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A High-Performance, Low Power Research Hearing Aid featuring a High-Level Programmable Custom 22nm FDSOI SoC*

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***Abstract*— With advances in algorithmic hearing aid research, the need for high-level programmable, behind-the-ear (BTE) wearable and low-power research platforms is emerging. These can be used to test new algorithms in real-world scenarios. Although various groups are developing different portable solutions, they are not in a BTE form factor. For this reason, the devices must be worn around the neck or somewhere on the body, which causes limited mobility and can lead to inaccurate research results. Therefore, this work presents a fully integrated and functional hearing aid research platform that weighs only 5 grams and can be worn behind the ear. The platform is high-level programmable, features wireless technologies such as near-field magnetic induction (NFMI) and Bluetooth Low Energy (BLE), and integrates two micro-electro-mechanical systems (MEMS) microphones and an external speaker. The audio processor of the system is based on a new custom, low-power 22nm mixed-signal system on chip (SoC). Different real-world use cases, like a dynamic compressor, are used to evaluate the platform. With a total power consumption of 47 mW, the rechargeable device achieves a run-time of six hours. When the wireless interfaces are turned off, the power consumption drops to 31 mW, and the run-time increases to nine hours.**

***Clinical relevance*—The proposed research hearing aid demonstration platform can be used portable and outside the clinical setting for algorithmic research. With its behind-the-ear form factor and rechargeable battery, studies can be conducted for several hours without restricting patient movement in real-world scenarios.**

I. INTRODUCTION AND RELATED WORK

With over 430 million individuals with disabling hearing loss and an increasing trend to over 700 million in 27 years [1], hearing aid research is becoming more and more relevant. In addition, evolving technologies and advances in architectural designs enable the devices to reduce their power consumption and achieve higher computational performance.

Research is being devoted to new and more advanced algorithms for hearing aids to make these enhancements beneficial to deaf and hard of hearing people. For example, one area of research is to improve the identification and localization of different speakers in complex and noisy environments, such as in [2]. In addition, neural networks are being explored to improve the signal-to-noise ratio or to denoise an input signal, e.g., in [3].

For clinical research, the new algorithms could be evaluated in a test setup in an audio laboratory, like presented in [4], using a computer. However, this test setup needs to be more portable and compact if the algorithms are supposed to be tested in a real-world setting with a wearable solution. At the time being, there are many commercial hearing aids on the market, but there are no publicly available research platforms or concepts in the size of an actual hearing aid.

For this reason, several research groups are working on programmable, wearable, and real-time capable platforms and frameworks like [4], [5], [6], [7], [8]. The platform presented in [4] is based on commercially available field-programmable gate arrays (FPGAs). Other systems use micro-controllers, like the BeagleBone Black wireless, for their platforms ([5], [6], [7]). Although the form factor of these devices is small compared to lab setup with a computer, they cannot be worn behind the ear. To use them, patients must at least wear a box around their neck, as depicted in [9]. Nevertheless, as stated in [6] ear-level devices in behind-the-ear (BTE) sizes are of particular interest. This design format is more convenient and does not require complex wiring on the body, making it easier to use in the field. Better and more accurate test results can be achieved without the cables and the restriction of the patients. It also reduces the stigmatization of subjects and test devices.

Therefore, this paper proposes a concept and demonstration device of a hearing aid research platform. It is a portable, low-power, high-level programmable, and rechargeable device in the size of a BTE hearing aid. The platform consists of all the necessary components to evaluate different real-world scenarios. It is based on a newly developed, programmable, 50 MHz Smart Hearing Aid Processor (SmartHeaP) system-on-chip (SoC) [10], two micro-electro-mechanical systems (MEMS) microphones, a speaker, and two different wireless communication technologies. Everything is embedded in a hearing aid case that is less than two 50-euro cent coins in size, so it fits easily behind the ear. With the proposed platform, research groups can evaluate the performance of novel hearing aid algorithms in real-world scenarios without the need for a clinical setup.

II. SYSTEM CONCEPT

To fulfill all the requirements of a hearing aid, the concept of the research platform is divided into four different subsystems, as illustrated in Fig. 1. These subsystems are an

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audio processing and system control unit, a wireless connectivity system, a power management system, and hearing aid peripherals.

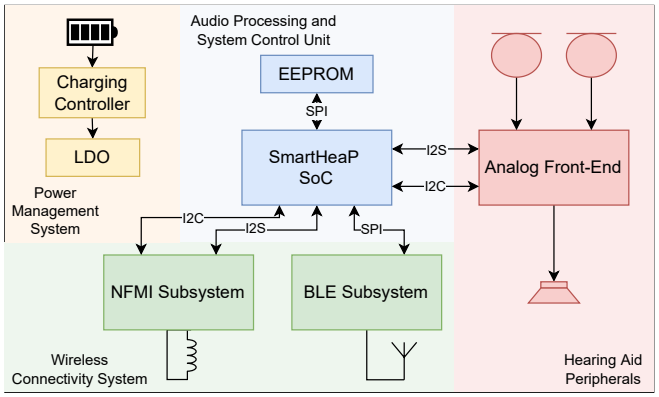


Fig. 1: Block diagram of the proposed research hearing aid showing the four subsystems: Audio processing and system control unit (blue), wireless connectivity system (green), power management system (yellow), and hearing aid peripherals (red).

All electronic components of the actual demonstration devices were selected to have a low noise profile and low power consumption. Communication between the different subsystems is implemented through various standard interfaces such as inter-integrated circuit (I2C), inter-IC sound (I2S), or serial peripheral interface (SPI).

The demonstration platform is implemented on a six-layer flex printed circuit board (PCB). The flexible interconnections are used to fold the PCB to fit into an actual hearing aid housing. The complete PCB and an enclosed hearing aid with the placement of all the components are shown in Fig. 2. In total, one hearing aid has a size of 4.6 x 2 cm and a weight of about 5 grams, including the battery and external speaker.

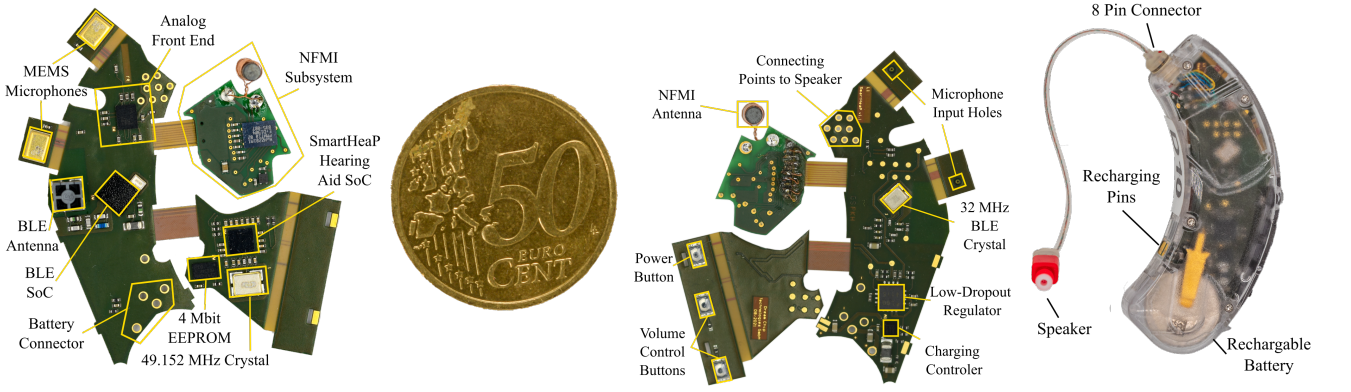
A. *Audio Processing and System Control Unit*

The audio processing and system control unit consists of an external 4 Mbit EEPROM and the Smart Hearing Aid Processor (SmartHeaP) SoC. The SoC is a novel application-specific integrated circuit (ASIC) fabricated in 22nm fully-depleted silicon-on-insulator (FD-SOI) and contains two application-specific instruction set processors (ASIPs). One core for wireless interfacing and a computational, more advanced core for audio processing. As shown in [10], the audio core of the SoC is capable of executing complex hearing aid algorithms without reaching the computational limits of the architecture. The essential features of the SmartHeaP SoC are listed in the table I.

TABLE I: SMARTHEAP SOC [10] FEATURE OVERVIEW

Analog Front-End	2 x 20 bit ADC & 1 x 20 bit DAC
Programmability	assembly, C, C++
Operating frequency	max. 50 MHz
Memory Audio Core	2 MB data + 256 kB instruction
Architecture	Cadence Tensilica Fusion G6 + Cadence Tensilica LX7 + Custom Instruction Set Extension
Technology	22nm FD-SOI
Size	7.365 mm^2
Native word Length	32 bit

As part of the Cadence Tensilica ecosystem, a comprehensive development environment, including a hardware-extensible C/C++ compiler toolchain (GCC, Clang), is included with the SmartHeaP SoC. In addition, the framework first presented in [11] has been modified through the use of hardware-extensible intrinsics to enable seamless porting of MATLAB fixed-point code to the SoC. Compared to other recently presented hearing aid processors without similar support, e.g., [12], these advances significantly reduce the development and implementation time of hearing aid algorithms.



(a) Front side of the PCB

(b) Back side of the PCB

(c) Fully integrated and folded PCB in the hearing aid case

Fig. 2: Integrated demonstration platform of the research hearing aid on a six-layer flex PCB with all the different electrical components.

After power-on, the audio core of the SmartHeaP SoC controls all necessary interfaces to the other systems and initializes the whole platform. The SoC itself boots from the external EEPROM. Reprogramming of the SoC can be done via a Bluetooth Low-Energy (BLE) update or a wired I2C connection integrated into the speaker connector. Reusing the connector eliminates the need for an additional programming port, e.g., USB-C, in the hearing aid case and keeps the size of the presented device smaller.

Via an individual reset line, the SmartHeaP SoC can switch the various subsystems on or off separately for different evaluation scenarios. For example, by turning off the wireless interfaces, the overall system's power consumption can be reduced, and a longer run-time can be achieved. In addition, the SmartHeaP SoC can control the audio samples' data path and choose to which subsystem they are forwarded.

B. Wireless Connectivity system

The proposed research device is equipped with a wireless subsystem that allows interaction with the platform without a wired connection and enables ear-to-ear communication. It consists of a near-field magnetic induction (NFMI) system and a BLE system.

The demonstration device presented uses an NXH2281UK SoC for the NFMI connection between two hearing aids. Due to the low carrier frequency of 10.679 MHz transmitted by a copper coil and the lower bandwidth compared to a BLE connection, the interface promises lower power consumption. To control the radio link and authenticate the devices, an ARM Cortex-M0, and an embedded 512 kbit EEPROM are included in the SoC, which has a package size of 10.38 mm². Via this subsystem, a real-time binaural streaming connection with two microphones per device can be established between two demonstration devices. This allows binaural algorithms, e.g., a minimum variance distortionless response (MVDR) beamformer [13], to be studied and explored on the research hearing aid.

A Goodix GR5515 BLE SoC is included for the BLE connections. The chip has 1 MB of built-in flash memory and a package size of 12.25 mm^2. It also has built-in power and reset management. The reset function is used to reset all components of the device at startup. In addition, the complete system can be updated via over-the-air updates.

With BLE technology, the hearing aid research platform may be used to investigate different self-fitting algorithms for the deaf and hard of hearing persons. With these algorithms, a hearing aid user can adjust the parameters of a dynamic compressor ([6], [14]) in real-world scenarios in real-time using a mobile phone without the need for lab setup. Furthermore, the wireless interface can also be used to control algorithms such as a beamformer manually or to adapt the parameters of other algorithms.

In addition, it can also be used for debugging and logging purposes. With a mobile phone connected to the hearing aid platform, it is possible to monitor settings or the outcome of an algorithm while wearing the hearing aid in a case study. Also, convenience functions such as volume can be controlled in this way.

C. Power Management System

The Power management system consists of a rechargeable Li-ion battery with a capacity of 74 mAh at 3.7V, the associated charging controller, and a Low DropOut linear regulator (LDO).

Zinc air batteries are primarily used in hearing aids because they are smaller and have a higher energy density ($\sim$ 650 mAh @ 1.4 V) compared to Li-ion batteries. However, the reaction is continuous once exposed to air, so the discharge can not be interrupted. A zinc air battery would be less efficient in scenarios with short power cycles, such as the development and deployment of algorithms. The battery would discharge, and unnecessary battery waste would be generated.

For this reason, a Li-ion battery is used in the demonstration device. These have a low self-discharge rate, and the discharge processes can be interrupted. Furthermore, due to the low-power components on the hearing aid platform, a run-time of several hours can still be achieved. If the run-time is still insufficient for a specific test setup, the battery of the research hearing aid can be replaced, similar to regular hearing aids. This ensures operation with minimal interruptions for extended periods while spare batteries can be charged externally.

An MPQ5480 charging controller is used to charge the battery inside the demonstration device and protect it from deep discharge. It is also used to generate a supply voltage of 1.8 V. In addition to powering all components on the hearing aid, the 1.8 V is also used as input to an LDO (ADP323) that provides a 1 V, 0.65 V, and 0.5 V supply voltage. The 1 V is used for the MEMS microphones and the NFMI SoC, while the 0.65 V and 0.5 V are used to power the SmartHeaP SoC.

D. Hearing Aid Peripherals

The demonstration device includes two low-power MEMS microphones, an external speaker, and an audio codec to operate as a fully functional and integrated hearing aid. Two MEMS microphones (P8AC03, from Sonion) were chosen instead of conventional microphones to reduce power consumption and system size. As with commercially available hearing aids, they are placed near the top of the case at a distance of about 1.5 cm.

Typically, a hearing aid's speaker is located near the microphones. The sound of the speaker is then transmitted into the ear with a sound tube. Due to this arrangement, this setup is more susceptible to feedback. To avoid this problem, the presented research hearing aid uses an external speaker (see Fig. 2c) placed directly in the ear canal. The distance between the components already reduces the system's feedback without requiring advanced algorithms. The loudspeaker is attached to the PCB via an eight-pin connector. This interface can also be used to program the research platform when the speaker is not attached.

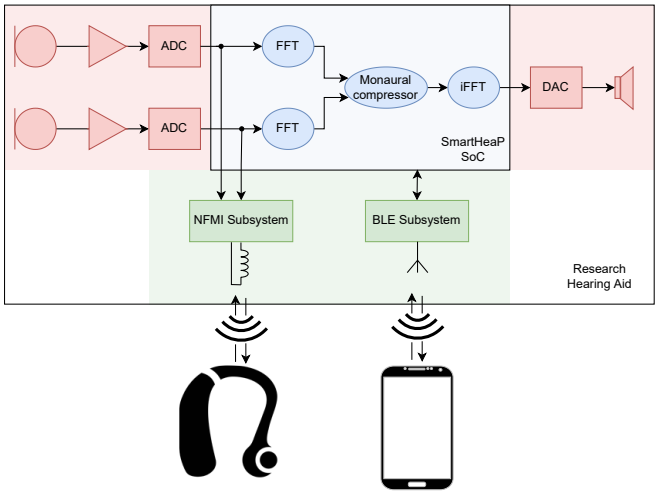


Fig. 3: Block diagram of an exemplary real-world use case for the evaluation setup. The squared boxes represent hardware systems, and the circles show the algorithmic implementation of the dynamic compressor on the SmartHeaP SoC.

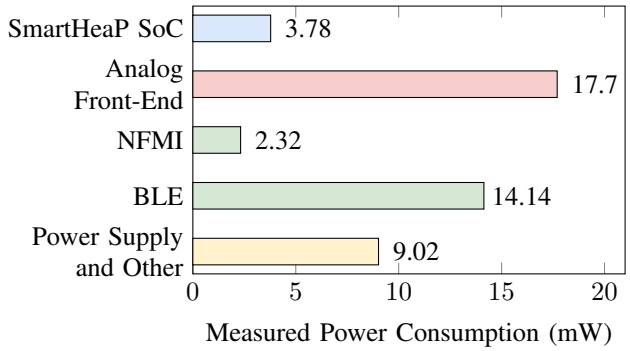


Fig. 4: Measured power consumption of the different subsystems of the research hearing aid during the operation of the dynamic compressor.

In addition to the integrated analog front-end of the SmartHeaP SoC, the shown demonstration device also features a commercially available low-power and low-noise analog front-end (MAX9867). The commercial front-end has a less precise bit length than the integrated one of the SmartHeaP SoC but has an analog amplifier and additional interfaces. With this complementary component, the research platform offers the possibility to investigate the effects of different bit lengths and gains of the analog input signals on the algorithmic results.

III. CASE STUDY: POWER CONSUMPTION ANALYSIS

Besides the system's processing power, the most critical aspect of the hearing aid is its flexibility and power consumption. Therefore, several hearing aid use cases were deployed on the research hearing aid to evaluate the actual power consumption. Firstly, calibration software is deployed to calibrate the corresponding demonstration device's input and output levels. In addition, common algorithms like noise reduction [15], adaptive feedback cancellation [16], a dynamic compressor [14], and an MVDR beamformer [13] were evaluated on the platform.

Figure 3 depicts a block diagram of an exemplary evaluation setup for a real-world use case. In this scenario, the dynamic compressor, which works in the frequency domain, is deployed on the SmartHeaP SoC as a primary audio program. The algorithm's parameters can be updated or adapted via a mobile phone through a BLE connection. The NFMI connection is also active to measure the system's maximum power consumption, even though this use case does not require the binaural link.

Furthermore, the outputs of the MEMS microphones are connected to the external analog front-end. The interface amplifies 16 dB to both analog signals before converting them to the digital domain. The signals are sampled at 16 kHz with 16 bits per sample. Afterward, the digital signals are transmitted sample by sample via I2S to the buffers of the SmartHeaP SoC.

The blue circles in Fig. 3 show the exemplary implementation of the dynamic compressor [14]. In this use case, the SmartHeaP SoC buffers 64 samples for each channel into internal queues. Therefore the maximum processing time for the algorithmic steps are 4 ms to meet real-time requirements. Otherwise, the buffers of the SoC will overflow. Applying overlap-add with the last frame and 50 % zero padding, a 256-point FFT is necessary to process one input frame per microphone channel. The complete use case occupies roughly 37 % of the computing resources of the SmartHeaP SoC while using semi-automatically generated C code without extensive hand optimizations.

During the processing of the audio algorithms, the SmartHeaP SoC also checks if new updates of the parameters are available from the BLE subsystem and updates the algorithm accordingly. Afterward, the processed samples are sent back to the external analog front-end via I2S. Subsequently, the converted analog signal is output to the speaker without amplification.

The power consumption is measured for the described use case to obtain information for the system's uptime. With all subsystems and peripherals active, the hearing aid can operate for up to six hours and has a mean power consumption of 47 mW. For the other evaluated algorithms, the results are similar. The energy consumption only deviates by up to two milliwatts on the SmartHeaP SoC, depending on the algorithm.

For a further breakdown, Fig. 4 shows the measured power consumption of the different sub-modules. These measurements could not be obtained by direct measurement at the components due to the highly integrated nature of the demonstration device. Instead, the power is measured at the battery, while the subsystems are disabled individually by software. The resulting power difference is used as an estimate for the power consumption of the subsystem. This

also includes losses in the power management subsystem and thus overestimates the actual power consumption of the component.

The figure shows that the hearing aid peripherals consume most of the power. This includes the analog front-end, which consumes roughly 38 % of the total power (17.7 mW). Like other portable hearing applications, the BLE Subsystem consumes around 14.4 mW while sending and receiving. This equals 30 % of the power of the proposed system. The power management system required for the use of rechargeable batteries, including the low noise LDO, consumes around 20 % of the power.

This evaluation shows that a significant portion of the power consumption from the demonstration device is due to wireless interfaces. As stated before, the NFMI interface consumes much less energy than the BLE interface. At about 2.3 mW, it is about 6x more power-efficient than the BLE interface, but it has a range of only 25 cm. Therefore, if these interfaces are not required in a test scenario, they can be turned off. An additional measurement for the dynamic compressor without wireless connectivity shows a power reduction down to 31 mW, increasing the system's run time to nine hours.

The SmartHeaP SoC, the central part of the proposed research listening device, has among the lowest power consumption, ranging from 1.8 mW to 5.5 mW depending on the processed algorithm. The lowest power consumption has the MVDR beamformer with 1.8 mW and the noise reduction algorithm the most with 5.5 mW.

IV. CONCLUSION

This paper presents a concept and implementation of a fully integrated hearing aid research platform. It is based on a new high-level programmable, mixed-signal chip produced in 22nm, the SmartHeaP SoC. It incorporates all required external components, like an external analog front-end and a BLE interface, into a BTE form factor case with a total weight of 5 grams. The device allows the evaluation of novel hearing aid applications without the need for external components. The platform's power characteristics are evaluated using several typical hearing aid algorithms, like a dynamic compressor or noise reduction. The measured results show that the demonstration device can achieve run times of up to nine hours while consuming 31 mW. This is more than sufficient for use as a research platform and also allows more extended studies, including real-world scenarios with deaf and hard of hearing people.

Furthermore, the performed case studies on the implemented demonstration device with the different use cases show that the high-level programmability of the SmartHeaP SoC enables quick deployment of new hearing aid algorithms onto the hearing aid platform. In addition, the wireless interfaces allow for quick testing and reconfiguration at the cost of increasing the system's power consumption.

Overall, the presented high-level programmable research hearing aid device enables hours of real-world case studies with deaf and hard-of-hearing people without the need for laboratory set-up or additional equipment.

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