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LETTER

Low-latency processing of IoT information in the IoT platform named “C-NAT”

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Abstract It seems to be reasonable that various IoT services are deployed over the IoT platforms with commonalities for these services. One of these platforms is CCN with Network Initiative And Traffic Control (C-NAT) which has been proposed by the authors. C-NAT intends to be operated over the Internet. However, this operation causes to increase in the processing delay at interworking points by multiple buffer copies. As the first step to solve this problem, this paper proposes that C-NAT is operated over the data link layer to reduce the processing delay. It indicates the advantages of this proposal by queuing analysis. It also describes operational sequences in this proposal.

Keywords: IoT platform, ICN, CCN, C-NAT, low latency communication, IoT DEP

Classification: Network management/operation

1. Introduction

Various IoT services have been deployed. In IoT mature stage, the IoT platforms with commonalities for these services should be required. Many articles have been discussed on these platforms. For example, the IoT reference models to specify these platforms are discussed in [1]. The platforms focused on information and communication technologies (ICT) are discussed in [2]. Authors also identify the IoT platform architecture for communication network technologies, named “Sandwich architecture” in [3].

Authors have indicated the data access platform with lightweight processing [3]. They have also proposed CCN with Network Initiative And Traffic Control (C-NAT) as one of the concreated protocols in this platform. C-NAT provides lightweight communication, which mitigates protocol overhead of the Internet by Information Centric Network (ICN) technology [4], particularly, Content Centric Network (CCN) technology [5].

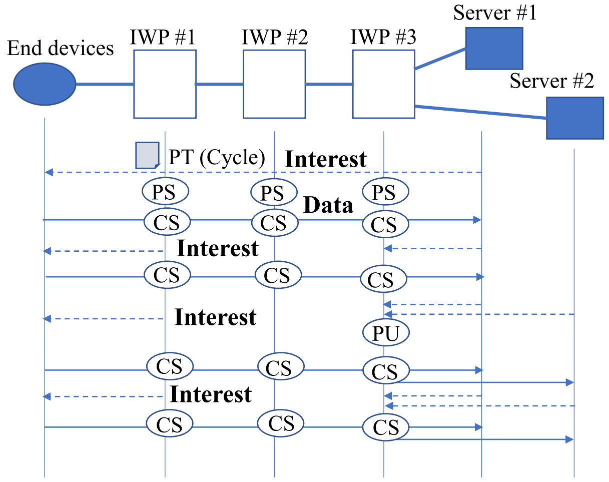
This paper intends to provide low-latency processing at communication facilities, i.e., Interworking Points (IWPs), endpoints, in C-NAT. This paper proposes low-latency processing by reduction of buffer copies in an IWP and endpoints, and provides the effectiveness of this approach through queuing analysis. Moreover, it also indicates operations of C-NAT based on this proposal.

This paper is extended from the authors’ articles published at IEICE General Conference [6].

2. Overview of C-NAT

This section summarizes C-NAT. For detail, C-NAT has been published in [7]. Its options have been published in some papers, e.g., [8].

C-NAT specifies two features, i.e., lightweight communication sequences for IoT services based on named base communication, and traffic control, including bandwidth assignment and priority control on cache at IWPs. This section indicates the former features in Fig. 1.



IWP: Interworking points, PT: Provisioning Table
Actions in each IWP
PS: Pending Interest Table (PIT) Set, PU: PIT update,
CS: Contents Store

Fig. 1 Overview of communication sequences in C-NAT

In C-NAT, the first **Interest** message is transferred from the Server to the End devices, e.g., Server #1 to End devices in Fig. 1. Then, the **Data** message corresponding to the first **Interest** message is transferred from the End devices to the Server. At that time, IWPs still maintain the state of “PIT set,” i.e., the state of the Pending Interest Table is activated for the **Interest** message, for the second or after **Data** messages. In the second or after rounds, when information is transferred from end devices, **Interest** messages are transferred according to the Provisioning Table (PT) at the IWP

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accommodating end devices. The detailed sequences are provided in [7].

When an additional server, e.g., Sever #2, intends to obtain information, information is transferred from the Contents Store (CS) in IWP by **Interest** messages from this server.

In CCN, it is a problem that information is stored in CS for a long period. To solve this problem, the additional function of the timed cash control has been published in [8].

3. A problem of implementation on C-NAT

C-NAT, as summarized in the previous section, seems to be one of the promising candidates for lightweight IoT platforms. Although C-NAT can be operated independently of IP flows by ICN technologies, it can be positioned as an application layer function in actual implementation. Therefore, it requires multiple buffer copies in the software proposing messages of C-NAT. For instance, Fig. 2 shows the layer structure for information processing at an IWP.

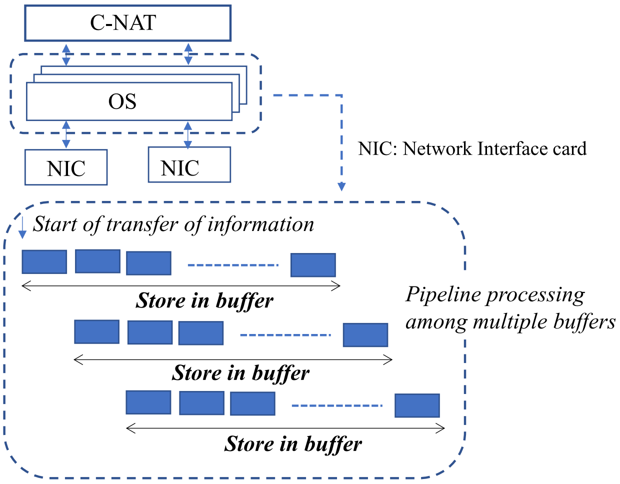

C-NAT
OS
NIC
NIC
NIC: Network Interface card
Start of transfer of information
Store in buffer
Store in buffer
Store in buffer
Pipeline processing among multiple buffers

Fig. 2 Layer structure and pipeline processing of information at an IWP

In actual implementation, an IWP can be decomposed into three parts, i.e., Network Interface Card (NIC) for processing on the physical and the data link layers, Operating Systems (OS) for the network and the transport layers, and protocol processing on C-NAT as the application layer as shown in Fig. 2. In this implementation, the OS part includes multiple buffers, e.g., socket, protocol processing, temporary, aliment of information, etc. Multiple copies of information among these buffers are invoked.

In the information processing in the OS part, pipeline processing [9] is applied as a legacy architecture. Information is divided into small blocks, and then, is transferred among buffers.

Therefore, processing delay is mitigated compared to complete store-and-forward processing.

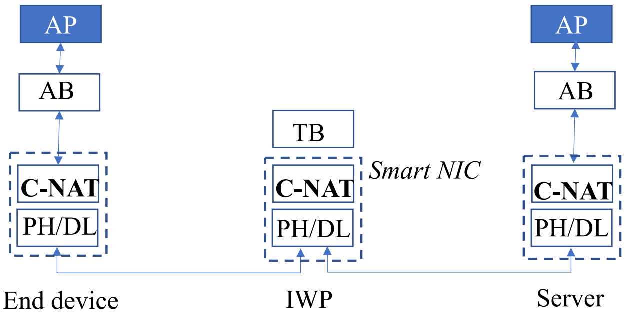
4. Proposed architecture for low-latency processing

In low latency and low delay variation IoT services, e.g., industry IoT services [10], this processing delay can have serious impacts. Therefore, this section proposes that C-NAT is operated over the lower layer, i.e., the data link layer.

4.1 Implementation in smart NIC

Recently, it is one of the attractive subjects that processing with intelligence is executed over NIC, i.e., the smart NIC architecture, e.g., [11]. In this architecture, the information transfer processing is accelerated by FPGA on the smart NIC [12] and embedded software in onboard dedicated processors [13]. According to these trends, an IWP, including C-NAT, can be implemented by hardware acceleration.

Therefore, the low-latency communication architecture based on C-NAT is proposed, as shown in Fig. 3. In Endpoints, i.e., End devices and Servers, and IWPs, because C-NAT is implemented over smart NICs, multiple buffer copies can be mitigated.



AP: Application AB: Application Buffer
TB: Temporary Buffer
PH/DL: Physical and Data link layers

Fig. 3 Communication flow based on the proposed architecture

In Fig. 3, information is transferred between Application Buffers (ABs). However, in an IWP, Temporary Buffer (TB) is implemented over smart NIC, because it corresponds to CS in CCN.

4.2 Effectiveness of the proposed architecture

Mitigation of buffer copies is evaluated by queueing models in this subsection. Fig. 4 shows the model of endpoints and IWPs for performance evaluation,

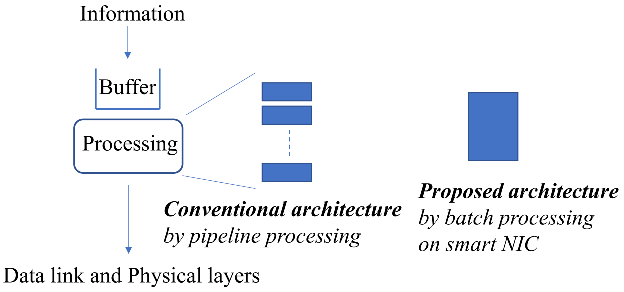

Information
Buffer
Processing
Conventional architecture by pipeline processing
Proposed architecture by batch processing on smart NIC
Data link and Physical layers

Fig. 4 Models for performance evaluation

In the conventional architecture, information is decomposed into several blocks, and is handled by pipeline processing. In the proposed architecture, information is not decomposed, and is handled by batch processing, i.e., processing of information whole. Information is transferred from the application buffer at end systems, and from the temporary buffer at IWPs. If information arrives in the C-NAT module in Fig. 3 randomly and its length is also random, the M/Ek/1 model for each point is applied to the conventional architecture. Ek denotes the Erlang distribution with k-phase. In this situation, the M/M/1 model is applied to the proposed architecture.

These models are explained as follows. The performance is normalized by the period of information transfer. The arrival rate of information is denoted by λ. In pipeline processing, when the number of processes is N, it is assumed that information is decomposed to k and overhead in each proposes is r. In this case, when the capabilities of information processing in both architectures are identical, the period of information transfer, h_k, is derived from Eq. (1).

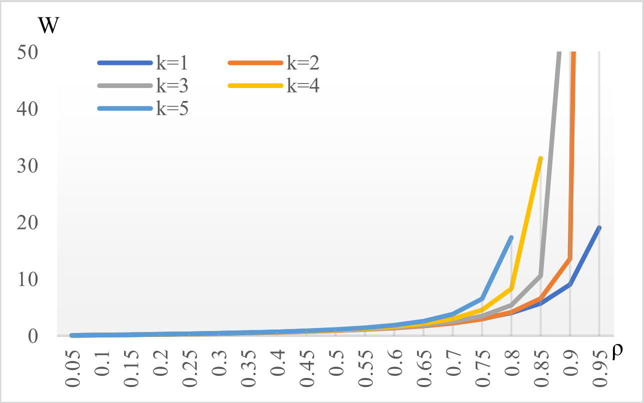


Fig. 5 Numerical solutions to compare between architectures (r=0.05)

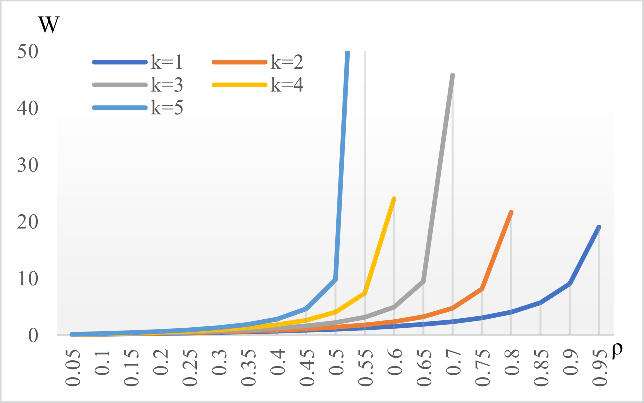


Fig. 6 Numerical solutions to compare between architectures (r=0.2)

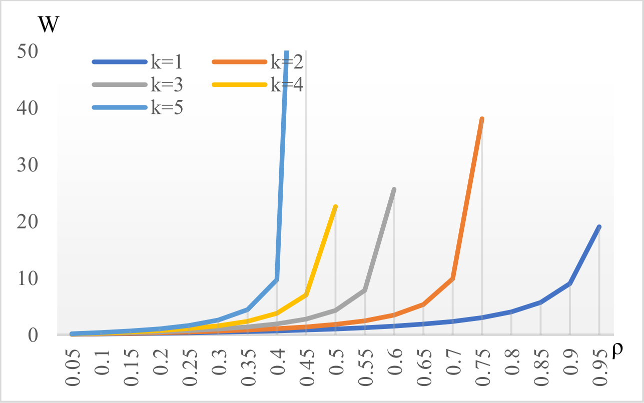


Fig. 7 Numerical solutions to compare between architectures (r=0.3)

$$h_k = \frac{1 + (k - 1)\, r}{k} \tag{1}$$

Generally, to derive the average proposing delay, W, Eq. (2) is applied to the M/G/1 model.

$$\mathrm{W} = \frac{\rho h \left(1 + C^2\right)}{2(1 - \rho)} \tag{2}$$

In these conditions, each parameter can be specified as follows.

$$\rho = \lambda h_k$$

$$h = h_k$$

$$C^2 = 1/k$$

Figures 5, 6, and 7 show examples of numerical solutions in these conditions.

In these figures, the case of "k=1" corresponds to the results of the proposed architecture. The other cases correspond to the results of the conventional architecture. These figures conclude that the proposed architecture can provide low-latency processing, particularly, notable differences among them in heavy load cases. In conventional architecture, the number of buffer copies is more, and latency is increased by increasing overhead. These characteristics indicate the case of a single point, i.e., an endpoint or an IWP. Therefore, in the end-to-end communication path, these differences will be more significant.

5. Operations of the proposed architecture

This section describes the operations of C-NAT in the proposed architecture. Because transferred information is identified by "name" in C-NAT, information can be identified by the Address of the AB shown in Fig. 3 and sequence numbers. Therefore, in this architecture, memory-to-memory communication is invoked among end devices and servers, as shown in Fig. 7.

In Fig. 8, the virtual memory consists of several areas. information of Application A is transferred to dedicated areas in Server across networks. Information of Application B is also transferred to that area. Areas for these applications are identified by the address in the virtual memory. When this communication is applied to C-NAT, communication sequences can be described in Fig. 8.

As shown in Fig. 9, the IWP accommodating end devices contains PT, including cycle and address in the AB.

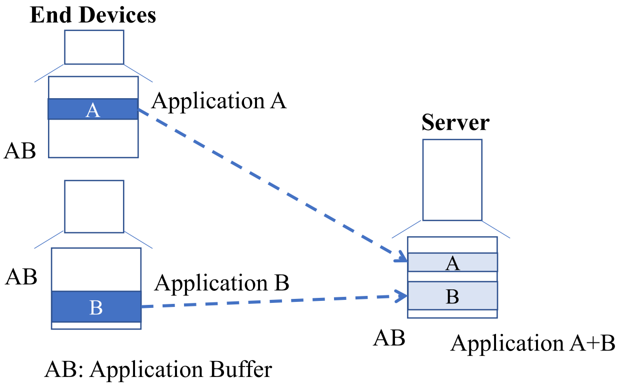


Fig. 8 Memory-to-memory communication among application buffers

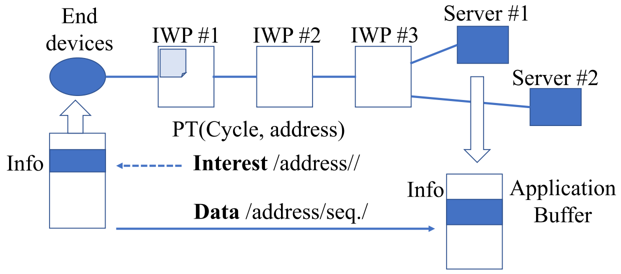


Fig. 9 Communication sequences on C-NAT in the proposed architecture

According to PT, **Interest** messages are transferred to end devices periodically in C-NAT. In the proposed architecture, these **Interest** messages indicate **Data** messages by identifying "/address//." After that, **Data** messages by identifying "/address/seq./." Other IWPs can identify **Data** messages by sequence number. Finally, the information contained in **Data** messages is stored in the AB of server.

6. Conclusions

This paper has described the enhancement of C-NAT for low-latency communication. This paper has invoked that C-NAT is operated over the data link layer, i.e., over the smart NIC. As the first step of this study, this paper has modelled the proposed architecture and has concluded its reasonability. Then, this paper has specified operations of C-NAT in the proposed architecture.

As the next step, this architecture will be implemented over the smart NIC and will be evaluated, by using real applications with requirements of low-latency communication.

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