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Discussion Group II – Circuit Reliability

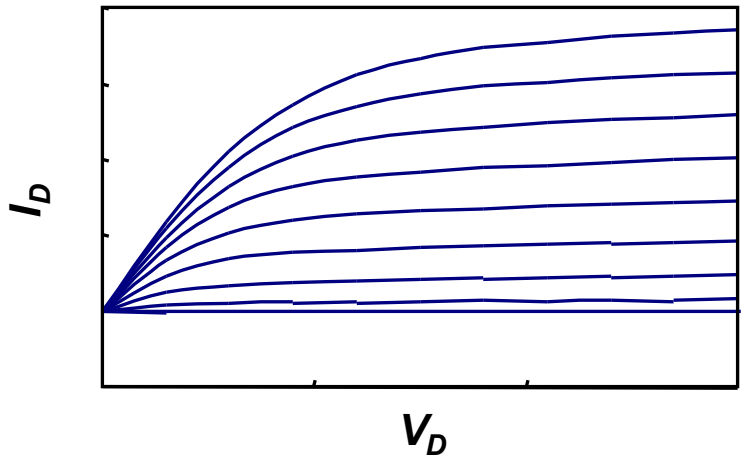
Moderator: Ben Kaczer, *imec*

Assumption

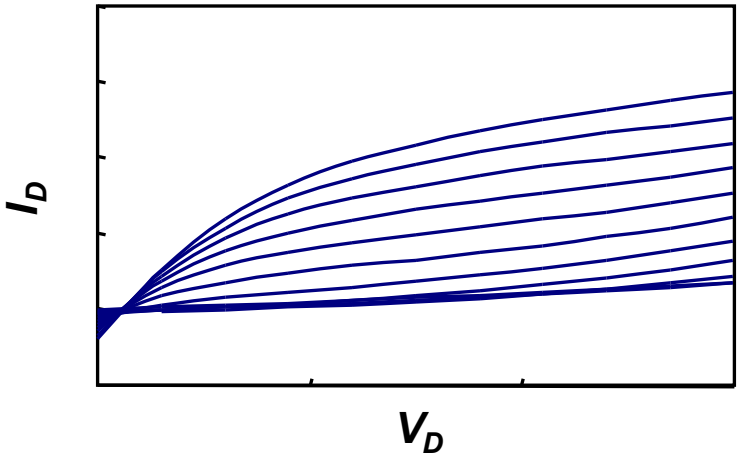
- We have here representatives of “both worlds”, i.e.,
  - Technology, reliability researchers and engineers
  - Circuit designers and EDA tool vendors

Why reliability is important

- Ex.: As fabricated: nominal PDK performance

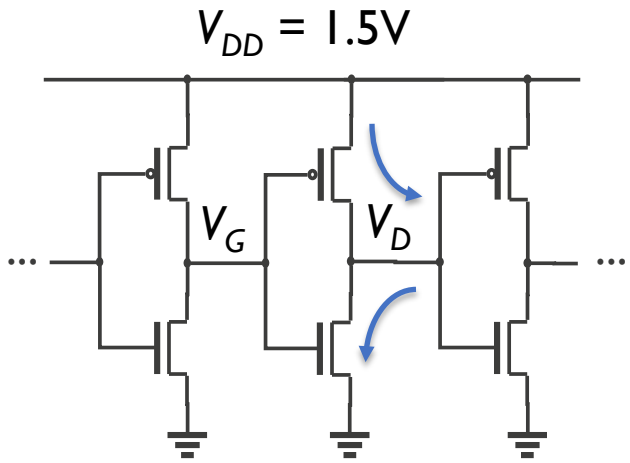


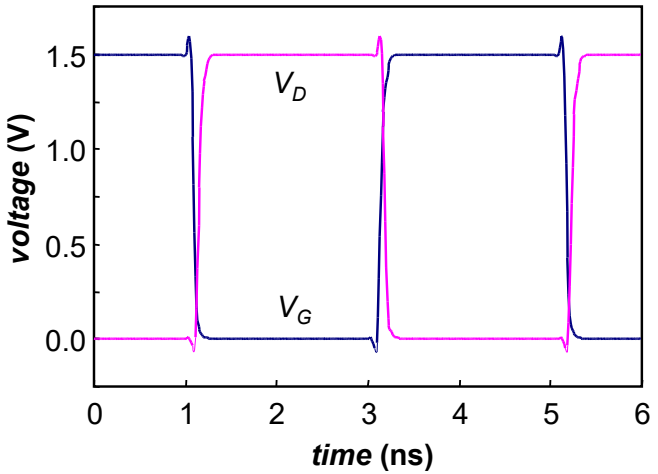
- E.g., a year later: degraded performance

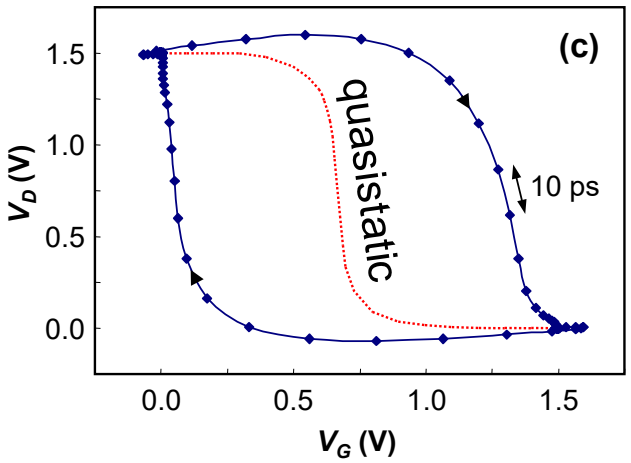


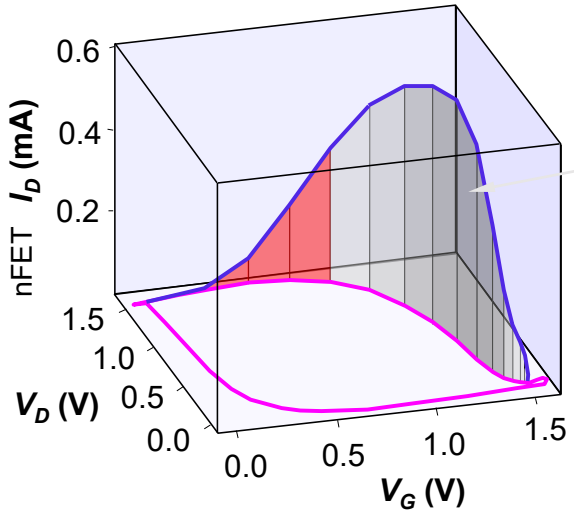
- Functionality needs to be guaranteed throughout the entire lifespan of the application
- Degradation mechanisms are complex and difficult to be accurately captured by empirical models, which may lead to
  - "Conservative" (worst-case) approach: lower performance, loss of profit margin, market share...
  - "Cavalier" (no-reliability) approach: field failures and returns, loss of profit, credibility, market share...

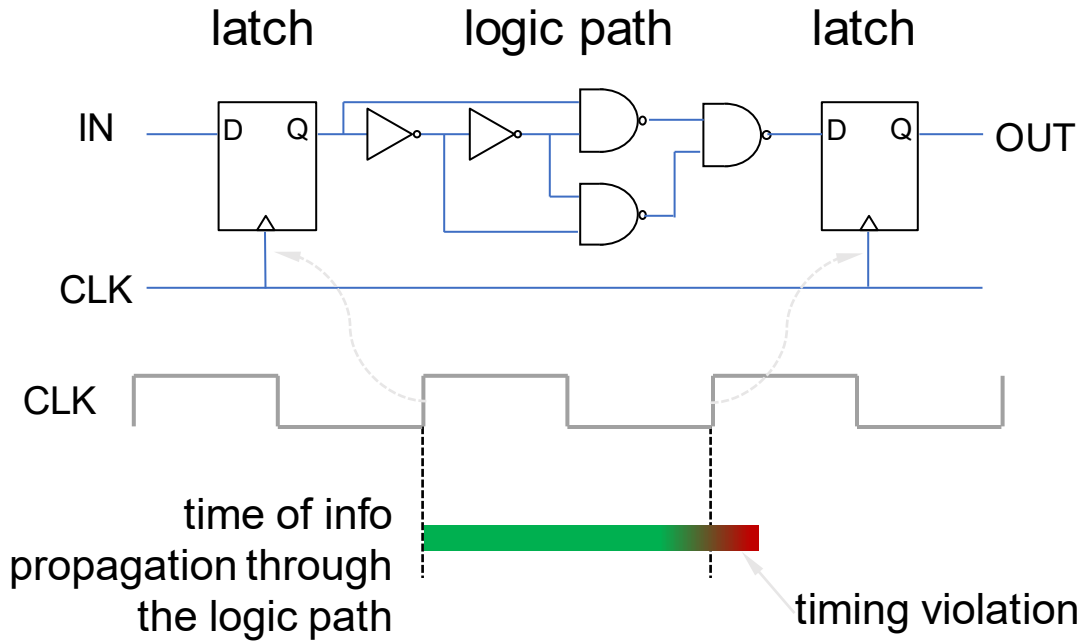
Quick (digital) circuits refresher: inverter (chain) and timing









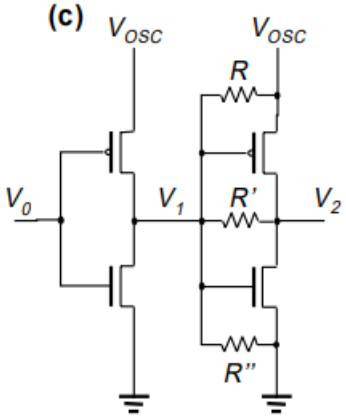


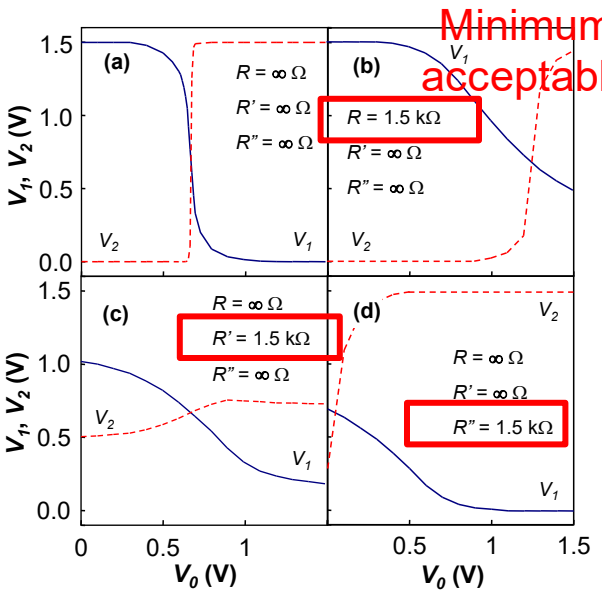
- Current needed to drive the next stage → dynamic power
- Current when FETs off → static power
- Adverse effects of degradation/aging:
  - lower *on* current → timing violation
  - leakage → higher power consumption, memory elements: faster charge loss...

B. Kaczer *et al.*, "Observation of hot-carrier-induced nFET gate-oxide breakdown in dynamically stressed CMOS circuits", IEDM 2002

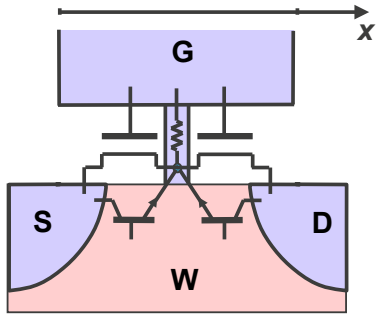
HBD and SBD Ex.: impact on RO and SRAM

- Worst-case effect of HBD on ring oscillator



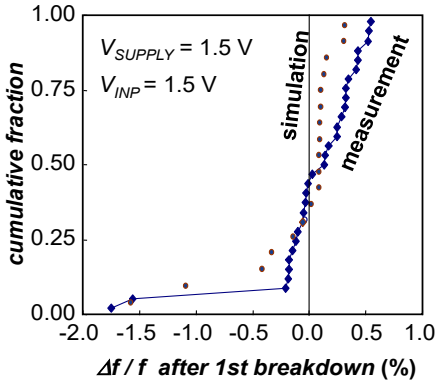


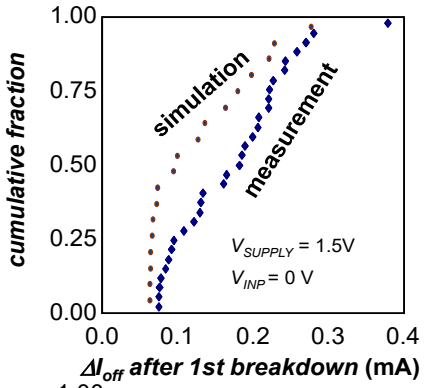
- More detailed lumped-element model for HBD explains distributions

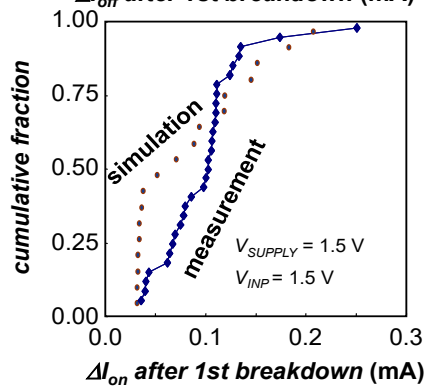


- Model reproduces FET behavior with BD at all positions *x* along the channel, in both inversion and accumulation

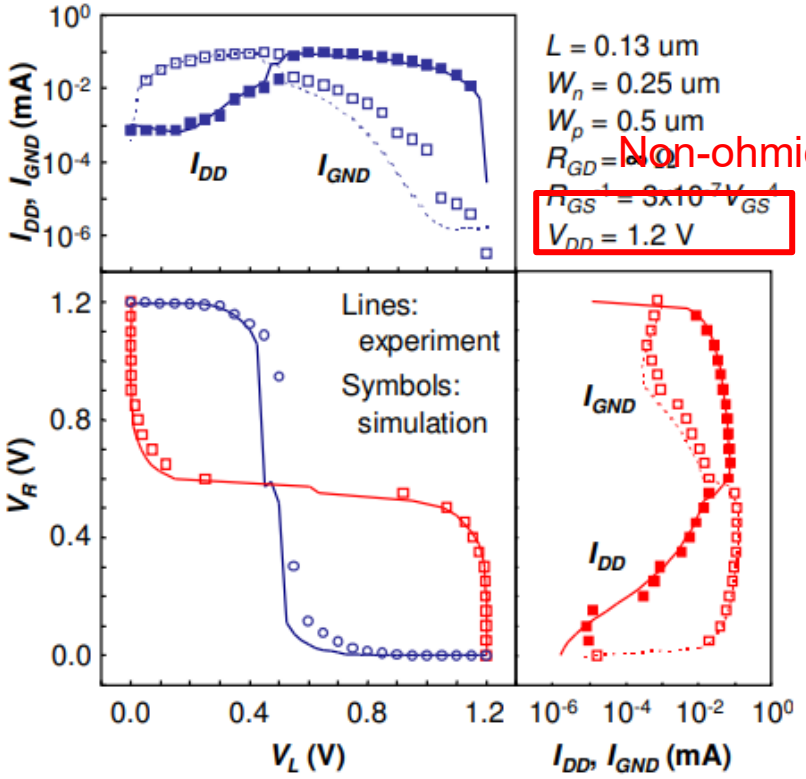
Ring Oscillator before and after breakdown







- Impact of SBD on static behavior of SRAM cell



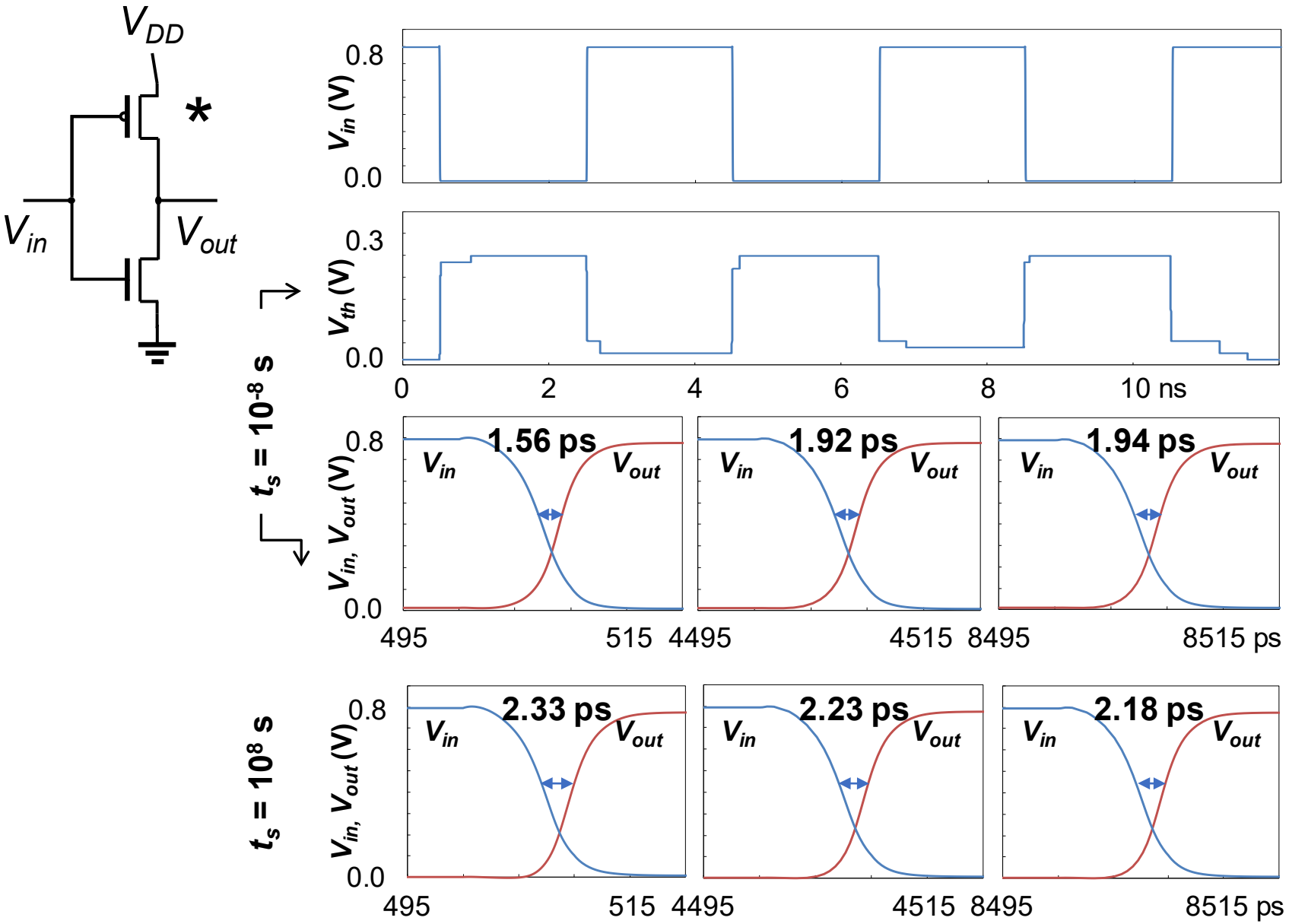
- Cell stable but consumes more power
- SBD may affect cell timings

B. Kaczer *et al.*, "Consistent Model for Short-Channel nMOSFET After Hard Gate Oxide Breakdown", TED 2001

B. Kaczer *et al.*, "Analysis and modeling of a digital CMOS circuit operation and reliability after gate oxide breakdown: a case study", Microel. Rel 2002

B. Kaczer *et al.*, "Experimental verification of SRAM cell functionality after hard and soft gate oxide breakdowns", ESSDERC 2003; R. Rodriguez *et al.*, "The Impact of Gate Oxide Breakdown on SRAM Stability", EDL 2002

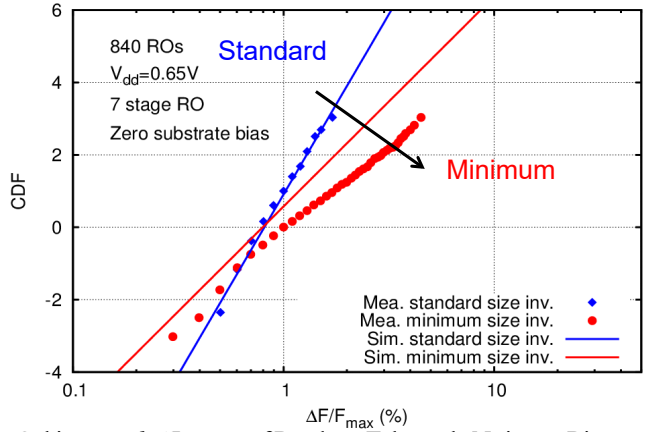
BTI ex.: delay intermittency and delay degradation with aging



- For simplicity, traps with randomized values of τ_c, τ_e, and ΔV_{th} "injected" only into the pFET* of an inverter
- At start: Intermittent and random delay (jitter)
- After aging: Delays degraded, still intermittent and random

B. Kaczer *et al.*, "Atomistic approach to variability of bias-temperature instability in circuit simulations", IRPS 2011

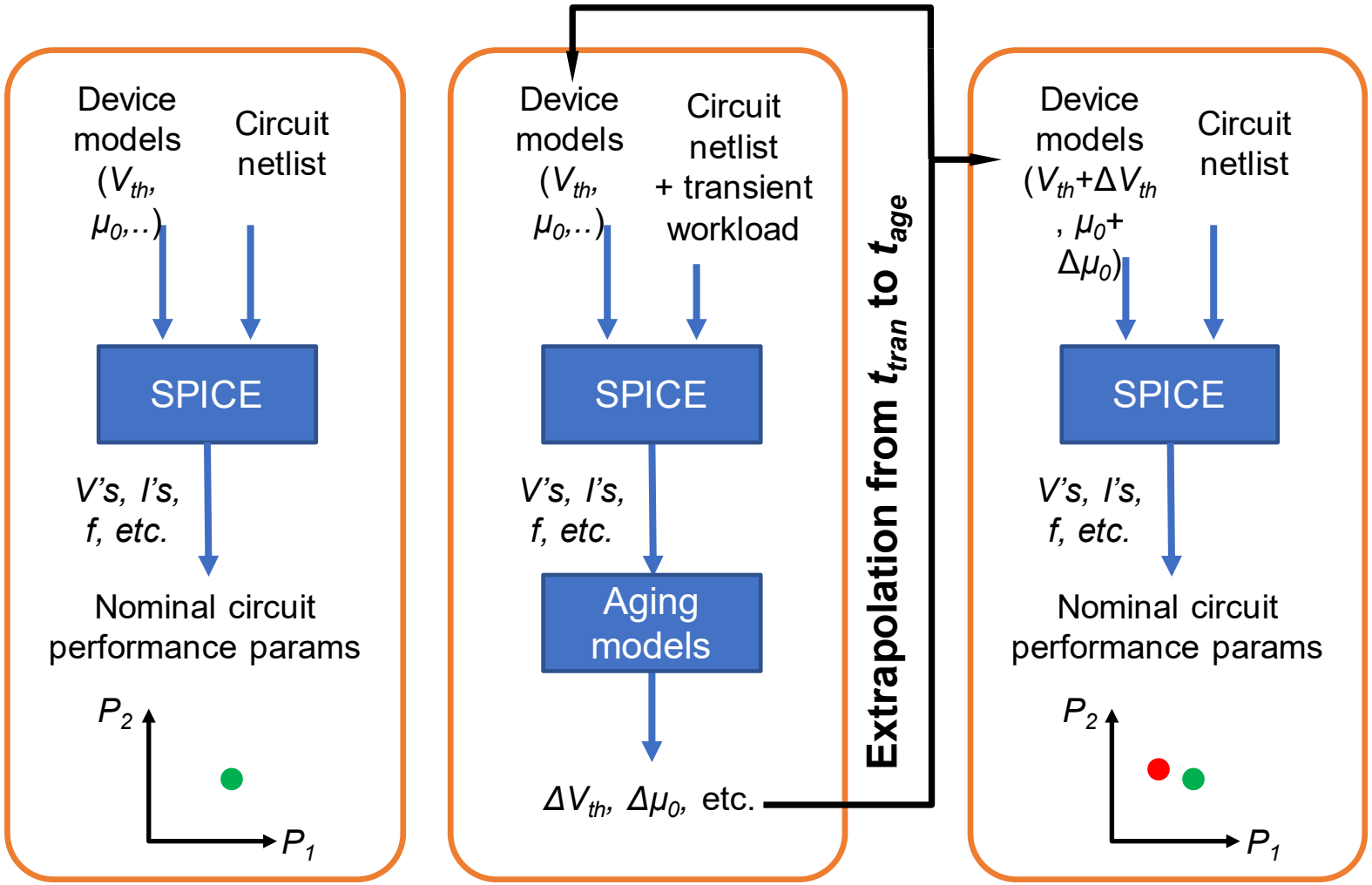
- Delay variability increases at lower V_{DD}, shorter paths, smaller devices



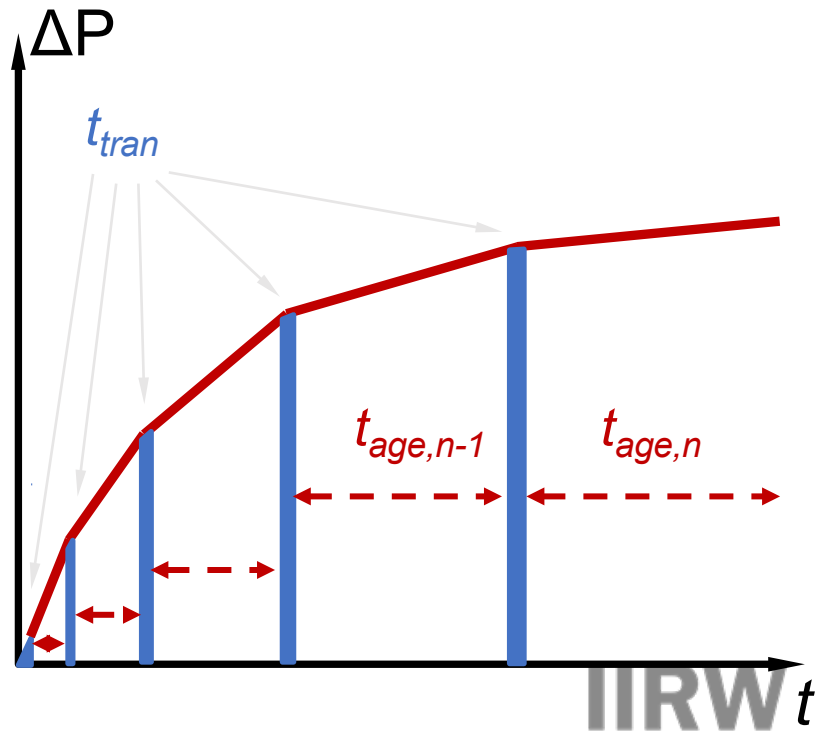
A. Oshima *et al.*, "Impact of Random Telegraph Noise on Ring Oscillators Evaluated by Circuit-level Simulations", ICICDT 2015

End-of-life simulation methodology

Nominal simulation → Stress simulation → Aged simulation



- Short "stress" transient simulation projected to degradation at certain "age" by aging models
- For more a precise reproduction of degradation, simulation can be divided into *n* steps and repeated piecewise over total life

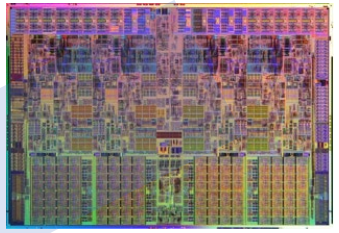


Source: D. Sangani

Compact model: intersection of worlds

Thorough understanding of the physics of degradation at individual defect level propagated to higher design abstraction levels

ESL



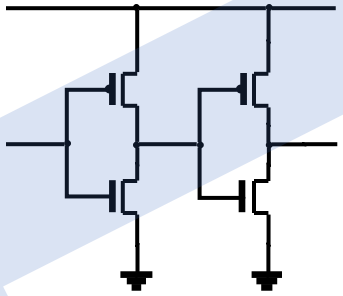
HDL/RTL

ALU

Gates

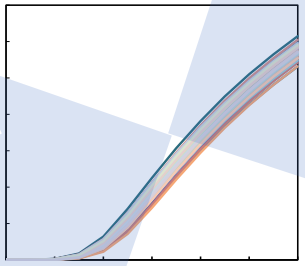
Workloads

Circuits

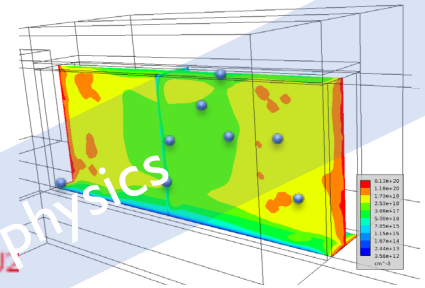


Reliability-Aware Compact models

Device transport

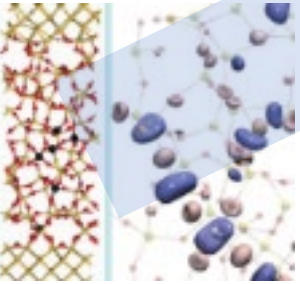


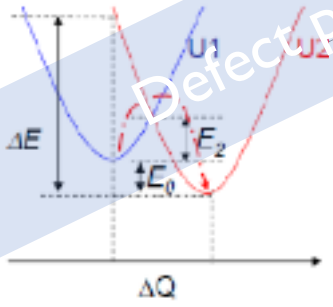
Trap kinetics



Defect physics

Atomic structure





Use and workload propagated to lower design abstraction layers

Standardized EDA + "Rel-aware" CM

Outline: Discussion topics

- Proprietary vs. Standard EDA circuit simulations?
- What should a «Reliability-aware» Compact model do?
  - Physical vs. Phenomenological?
  - Arbitrary VG, VD workload?
    - Include relaxation?
  - Mean degradation only vs. Distributions of parameter degradation?
  - Complexity vs. Accuracy vs. Speed?
  - Asymmetric HCD degradation?
    - «Playback» condition-dependencies of electrical degradation?
      - Operating V_{DD}, capacitive load, N/P balance in CMOS, ...
  - Output?
    - DVth, Dmu, D(SS)? DI-V? Noise figures? (How is noise currently simulated?)
  - Interface with Circuit Simulator
    - Wrapper circuit vs. Modify BSIM parameters vs. Proprietary vs...?

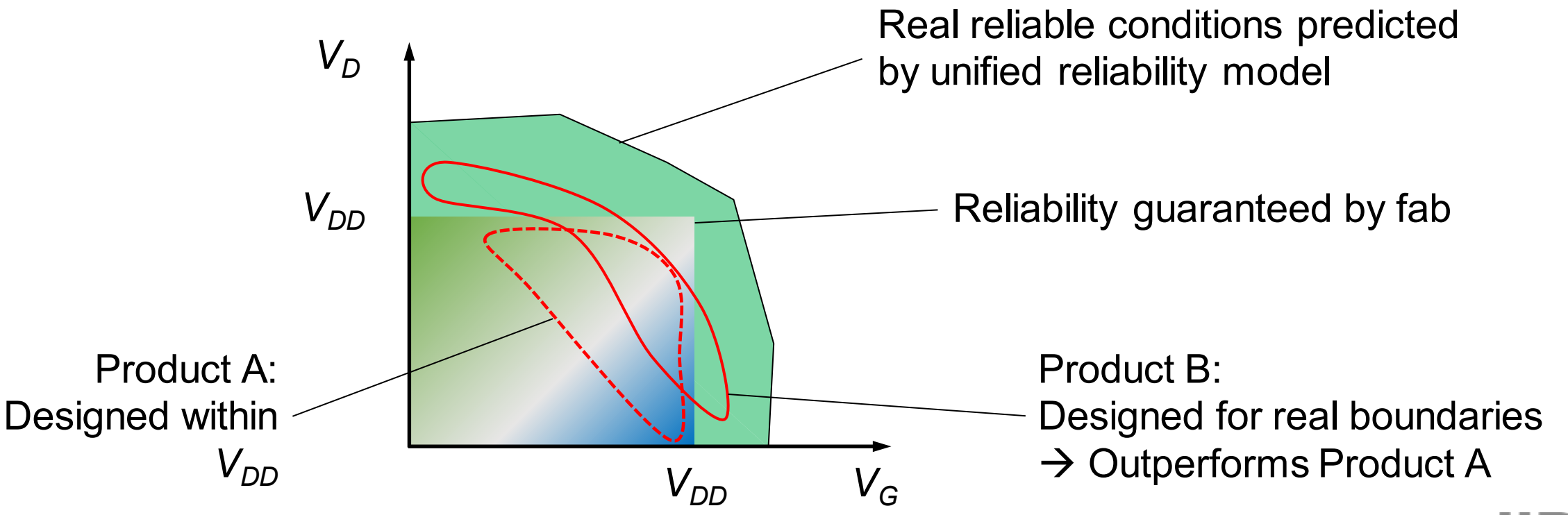
Outline: Discussion topics (2)

- Age vs. Defects
  - Individual defects with distributed properties vs. Continuous distributions of defects
- Reliability-aware circuit modeling «Ecosystem»
  - Foundries, EDA tool vendors, users, other parties: who does what?

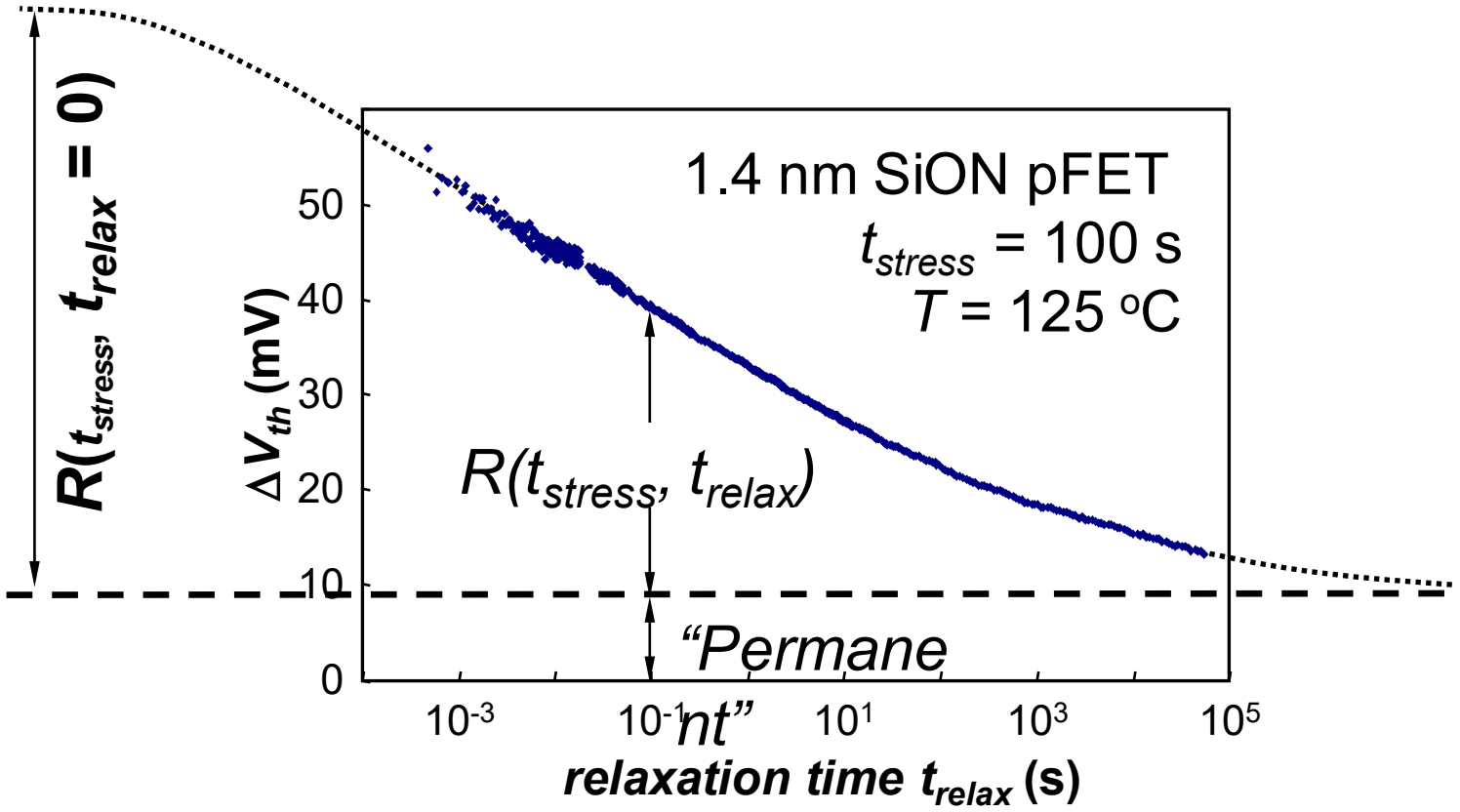
- What are “good” “standard” circuits to simulate in order to verify reliability aware compact models?
  - “Good” in the sense “relevant for applications”
  - “Good” in the sense “feasible to collect experimental data to compare with”
  - “Good” in the sense “feasible to simulate / not too complex”
- On which metrics (e.g. gain, frequency) should we focus when comparing reliability simulations of circuits with measurements?
- How representative is accelerated stress testing of circuits, of the real-life operating conditions?
- How do we verify long-term predictions of our models, typically used in EOL simulations?

CM should be covering entire (V_G, V_D) space

- Qualify and improve technology for reliability within V_{DD}
- Provide unified physics-based FEOL reliability model, based on deep understanding of underlying reliability phenomena



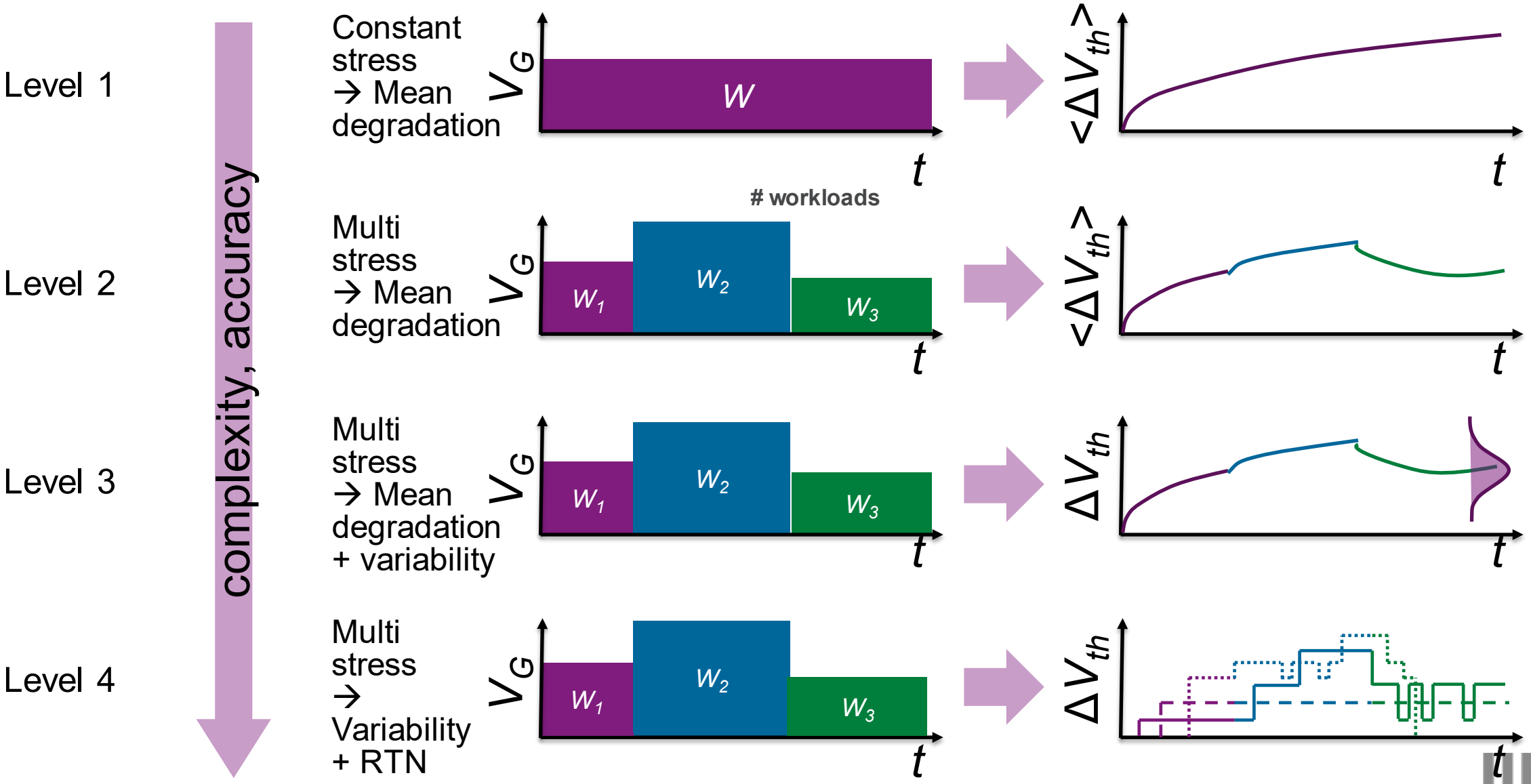
The curse and the blessing of BTI: relaxation



- Major issue for measurements, interpretation, and lifetime projection
  - Relaxation typically not complete → Permanent component
- \+ Contains information about the mechanism; increases device lifetime
  - Detrapping
  - Recovery/Anneal of interface states
- → Models must include relaxation to be fully physical

S. Rangan *et al.*, "Universal recovery behavior of negative bias temperature instability [PMOSFETs]", IEDM 2003; B. Kaczer *et al.*, "Ubiquitous relaxation in BTI stressing—New evaluation and insights", IRPS 2008; T. Grasser *et al.*, "NBTI in Nanoscale MOSFETs—The Ultimate Modeling Benchmark", TED 2014

Arbitrary-workload, mean and variability BTI circuit simulations



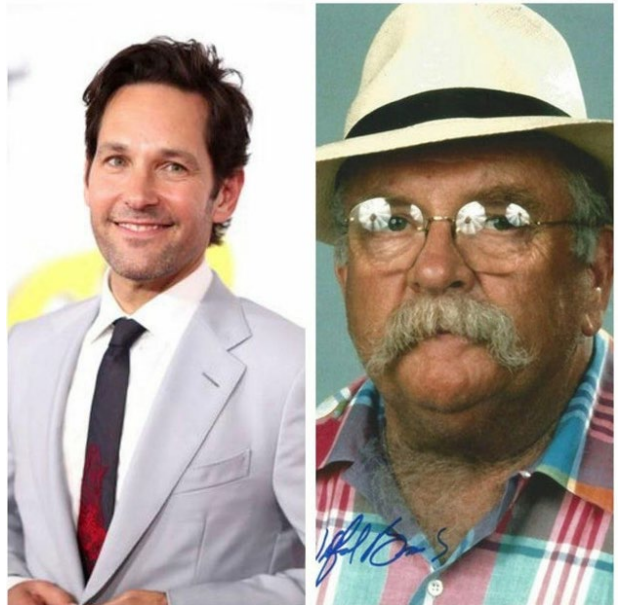
B. Kaczer *et al.*, SSE 2016

Gate oxide defects: the primary cause behind FET aging

- Example: physics-based Compact Models
  - Charge-based
  - Potential-based
  - ...

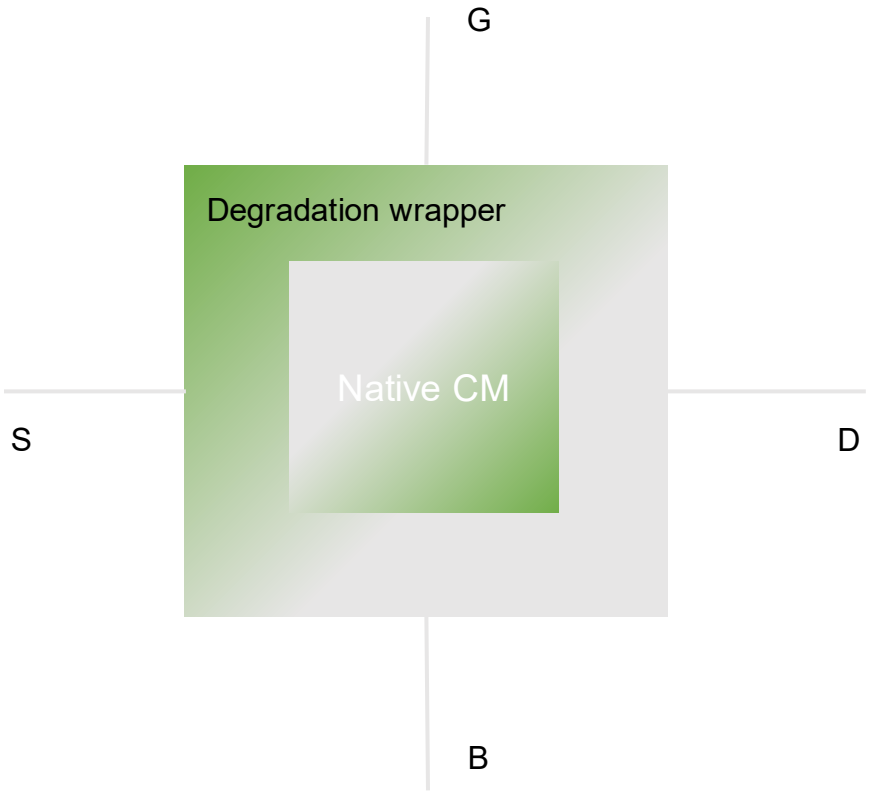
- Degradation models
  - "Age"-based
  - **"Defect"-based**

Same age, different "degradation"



Both 50 years old at the time photo taken

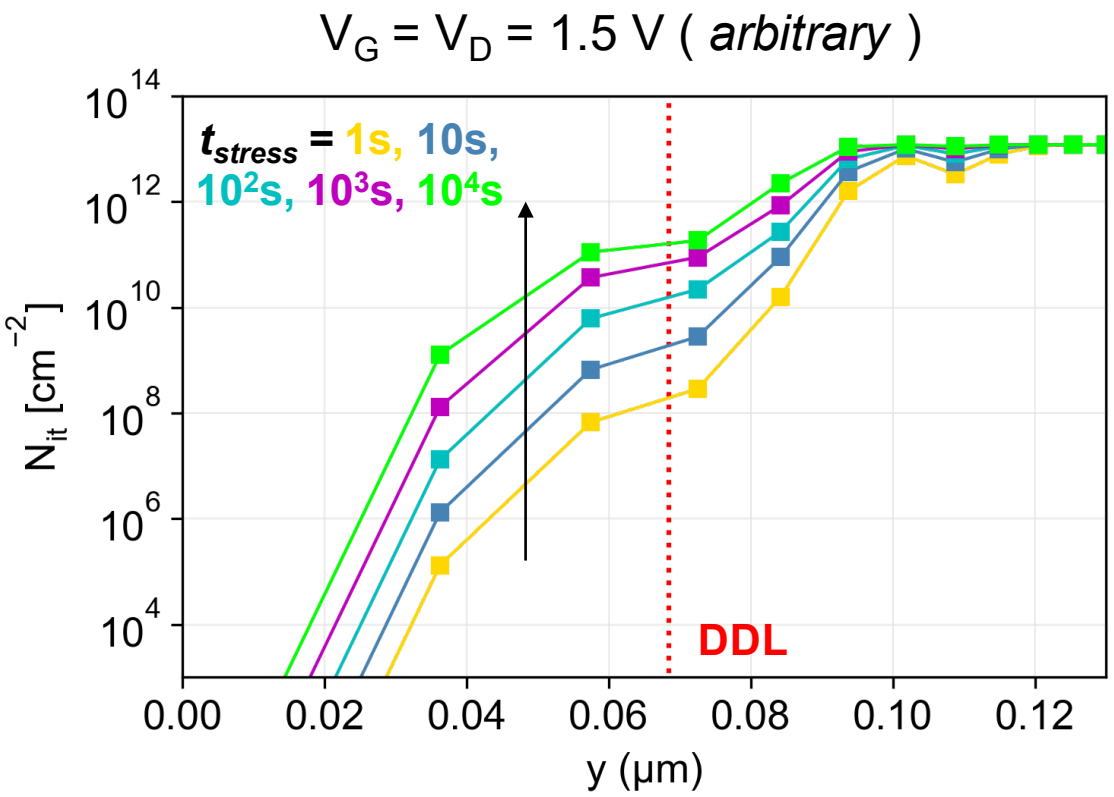
Wrapper

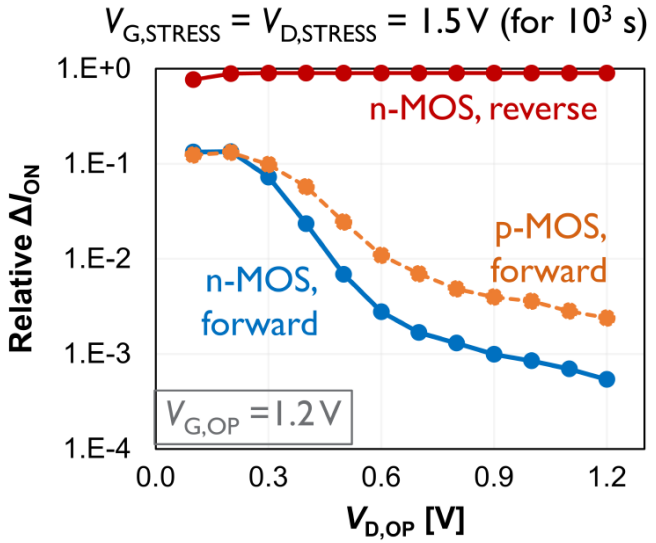


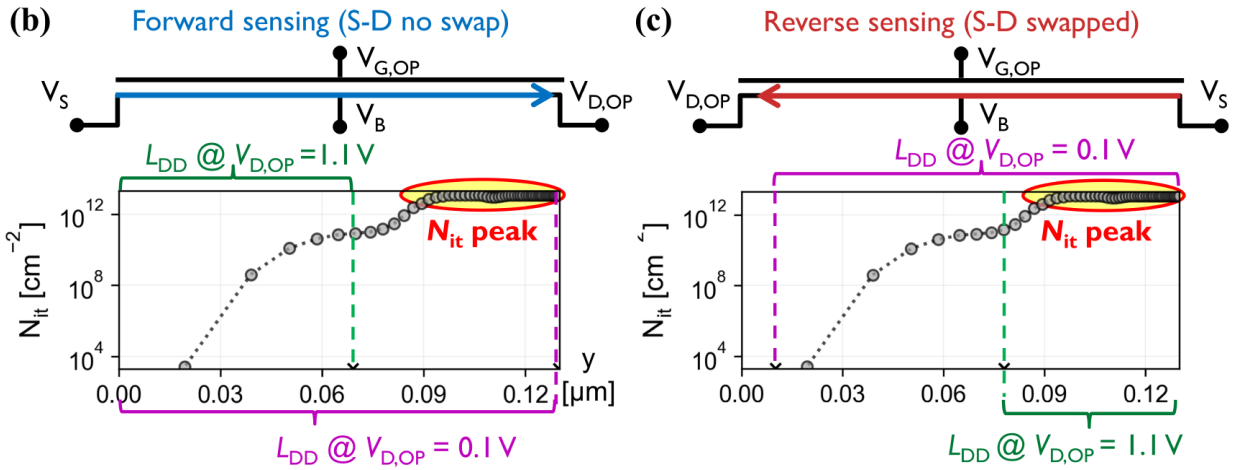
BSIM implementation: asymmetry of degradation reproduced

LCH = 130 NM, EOT = 1.9 NM (*UNCALIBRATED*)

Captures asymmetry of degradation







Y. Xiang *et al.*, IRPS 2021

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Channel slicing from Lin to Sat regimes: A DD FET from a series of ballistic FETs

Physics-Based Compact Model of Nanoscale MOSFETs—Part I: Transition From Drift-Diffusion to Ballistic Transport

Giorgio Mugnaini and Giuseppe Iannaccone, *Member, IEEE*

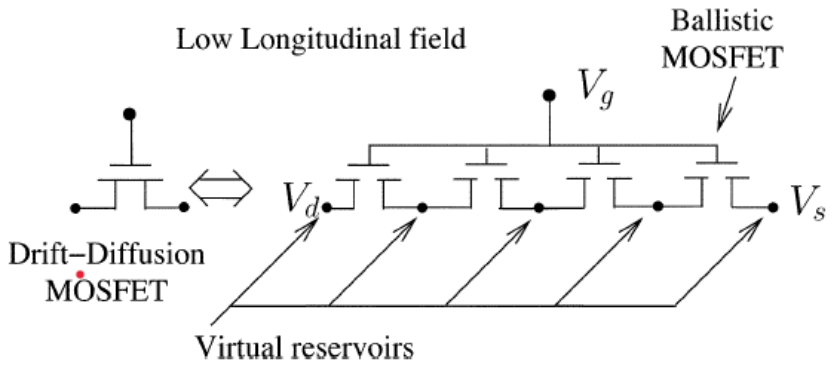

Fig. 2. Long chain of B MOSFETs. The contacts act as thermalizing reservoir. We also show the symbol we use for a B MOSFET in the following figures.

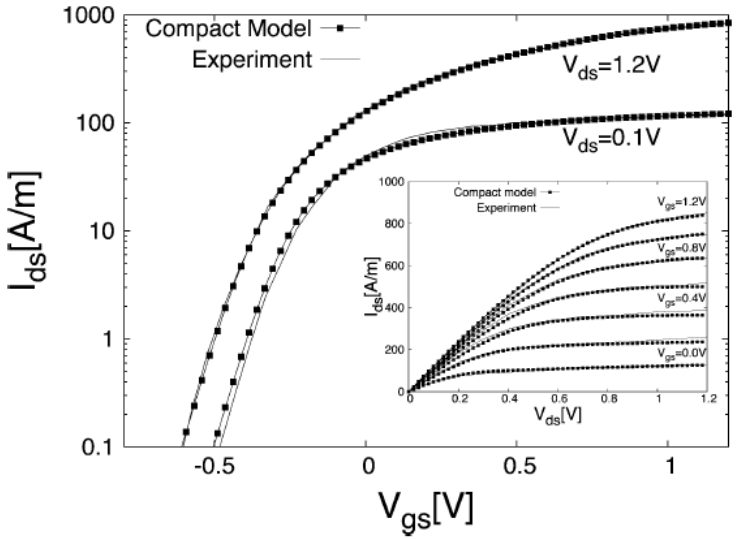

Fig. 9. Comparison between the transfer characteristics obtained from experiments on a FinFET with $L = 80$ nm reported in [33] and from a compact model fitted to the data. The comparison of output characteristics is illustrated in the inset.

Lambert-W function

$$I_{\rm ds} = \frac{\lambda}{2\phi_t} v_{\rm th} Q_n \mathcal{W}\left(e^{\frac{V_g - V_{Fn} - V_T}{\phi_t}}\right) \frac{dV_{Fn}}{dx}$$

$$Q_m = Q_n \mathcal{W}\left[e^{\frac{V_g - V_{Fn} - V_T}{\phi_t}}\right]$$

Potential slope (single value)

$$I_{\rm ds} L = \mu_{\rm no} \int_0^L Q_m \frac{dV_{Fn}}{dx} dx = \mu_n \int_{V_s}^{V_d} Q_m dV_{Fn}$$

$$\int \mathcal{W}(e^x) dx = \frac{\mathcal{W}^2(e^x)}{2} + \mathcal{W}(e^x)$$

$$I_{\rm ds} = \frac{\mu_{\rm no} Q_n \phi_t}{L} \left[\frac{Q_{\rm ms}^2 - Q_{\rm md}^2}{2Q_n^2} + \frac{Q_{\rm ms} - Q_{\rm md}}{Q_n}\right]$$

- The main requirement is the “local” potential continuity at each “virtual reservoir”

Z. Wu *et al.*, IRPS 2021

Minutes

- Log here a few key points that triggered lively discussion by the audience as perceived by you
- The goal is to have a short report at the end of the day

Participants

- Name, *Affiliation*
- Name, *Affiliation*
- Name, *Affiliation*
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Thanks for your participation!