Foreword
Microelectronics System Integration

IT IS A delight and honor to introduce this special issue of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY—PART B: ADVANCED PACKAGING. We feature six works, each of which was presented at ISIS'97, the 1997 IEEE International Conference on Innovative Systems in Silicon. As a showcase for microelectronics systems integration, the conference spans the spectrum from submicron device technology, through design techniques, and computer aided design, to systems architecture. The papers in this issue represent a peer-reviewed consensus of conference highlights, and reflect contemporary trends in applications, miniaturization, testing, and economics. Four of the contributions exemplify how to conceive, design, and implement a silicon system. The other two focus on effective application of technology and engineering resources in evaluating silicon systems.

Microelectromechanical systems (MEMS) continue to receive ever-increasing attention. This is largely a result of the range of the bulky, discrete-component systems that MEMS replace. Our first two articles provide excellent illustrations of extensions of the range of MEMS to the domains of environmental monitoring and process control. In "Silicon Micromachined Gas Chromatography System," E. Kolesar and R. Reston demonstrate how to design sensors by blending fundamentals of chemistry with knowledge of packaging and semiconductor processes. In "Microfluidic MEMS for Semiconductor Processing," A. Henning *et al.* show how micro-miniature valves and actuators can be used to control the concentrations of gases in semiconductor fabrication lines. These two papers point the way toward increased use of silicon systems for monitoring and controlling environments in which silicon systems themselves are manufactured.

Our third and fourth articles describe new developments in the design of switching circuits. In "Architecture, Defect Tolerance and Buffer Design for a New ATM Switch," V. Jain, L. Lin, and S. Horiguchi provide an implementation that supports the emerging network standard of asynchronous mode transmission. In "Programmable Neural Logic," V. Bohossian, P. Hasler, and J. Bruck develop a multi-input logic switch whose response threshold is dynamically adjustable. Both of these research efforts enhance our repertoire of modular building blocks for switching systems.

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Last, but certainly not least, we present two articles that melt traditional barriers between test and design. In "Possibilities and Limitations of IDDQ Testing in Submicron CMOS," J. Figueras and A. Ferré elucidate the impact of deep submicron processes on fault detection by measurements of quiescent device-to-device current. In "Economics Modeling of Multichip Systems Testing Strategies," M. Abadir relates an engineering manager's view of how to best spend test dollars. Spanning the spectrum from micro to macro, these two expositions give a sense of how communities of specialists in various aspects of integrated systems are themselves becoming more integrated.

We selected the papers above from a large number of very good contributions, and worked with the authors and referees to tailor each contribution to the readership of the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY—PART B: ADVANCED PACKAGING. We are excited about the result, and hope that you find this issue to be interesting, informative, and relevant.

In addition to the authors of the papers included in this issue, we would like to express our appreciation to everyone who submitted or reviewed a manuscript. The volunteer work performed by these people is critical to sustaining quality research, and we would like to recognize them by name, as shown at the top of the next page.

In particular, we would like to express our gratitude to ISIS Publications Chair J. Brewer, ISIS General Chairs D. Sciuto and S. Tewksbury, CPMT Publications Vice President P. Wesling, and CPMT General Editor J. P. Krusius. Thank you one and all.

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de Angel, E.
Delpiano, F.
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Franzon, P.
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Ghodsian, B.
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Judy, M.
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Lea, M.
Lombardi, F.
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Matsuzawa, T.
Meyer, F.
Modelli, A.
Omer, A.
Otterstedt, J.
Ozguz, V.
Page, K.
Pellegrino, P.
Pepe, A.
Pesando, L.
Prasanna, V.
Renovell, M.
Silvano, C.
Some, R.
Truzzi, C.
Wise, K.
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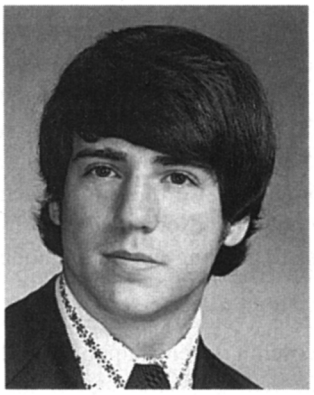

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