Guest Editorial
Special Issue on Low Power Electronics and Design

WITH the remarkable success of personal computing devices and wireless communication systems, there is an increased demand for high-speed computation and complex functionality. Complex and dense circuits are forcing integrated circuit fabrication technology into the deep submicron regime, and forcing the design specification into register-transfer and behavioral levels of abstraction. Simultaneously, constraints on power consumption have tightened because of the need for portable devices, circuit reliability requirements, and the costs associated with packaging and cooling.

The requirements of lower power consumption have already resulted in intense research activity. This has led to the formation of an annual symposium, the IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), at which much of this research has been reported.

This Special Issue features solicited papers expanding on presentations made at the 1996 ISLPED, held at Monterey, CA, August 12–14, 1996. The papers broadly fall into two categories: 1) low power electronics, which includes topics in device technology, and digital and analog circuits, and 2) low power design, which encompasses work in software and systems, synthesis, simulation, and power estimation. This issue contains the papers on low power electronics and most of the papers on low power design. The last two papers will appear in a Special Section of the March 1998 issue.

Low Power Electronics

The first three papers focus on device technology issues. The first describes an advanced CMOS process that utilizes a graded-channel implant to create the effect of a shorter channel length while controlling punchthrough and DIBL (drain-induced barrier lowering), to provide better speed at low supply voltages. The next paper quantifies, with simulations and experimental test structures, the variations in circuit speed that result from variations in device parameters such as channel doping concentration and gate length and width. At the 0.18 μm technology node, the variations can be up to 30%. However, for low values of V_{dd}, lowering V_t helps reduce variations in performance. The final technology paper presents the development of detailed analytical models for the fluctuations in V_t, subthreshold swing, drain current and subthreshold leakage caused by the random placement of channel dopant atoms. Those models are then used to predict variations in these parameters in the sub-0.1 μm regime. The authors predict that the variations will be unacceptably high, if current device structures are simply scaled according to the National Technology Roadmap for Semiconductors.

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The remaining papers cover a wide range of low power circuit techniques, primarily digital. The first describes a technique for achieving improved speed in SRAM's at low supply voltages, by boosting the voltage at critical circuit nodes. The key improvement made by the authors is their method of boosting these nodes while minimizing the charge that must be supplied by the on-chip charge pump circuits. The next paper presents analytical, simulation and experimental studies of a mixed voltage swing circuit methodology called "Mixed Swing QuadRail." An improvement in energy per operation of 2-3X is demonstrated, relative to conventional static CMOS. The following paper describes a monolithic temperature monitoring and recording circuit which can be powered from a miniature lithium cell for three years. A key feature is a timer circuit which operates at 10–20 kHz while dissipating only about 1 μW. A much higher and more precise frequency is achieved by the crystal oscillator circuit described in the next paper, with frequency digitally trimmable to sub-ppm accuracy. The authors have developed analytical expressions for estimating the oscillator amplitude, and therefore power, as a function of circuit parameters. The final paper for this section analyzes the power savings that can result from decoded instruction buffering in signal processing circuits. The authors show that a 25–30% power reduction is possible, while adding only about 2% to the area of a representative processor chip.

Low Power Design

The first two papers for this section will explore various techniques for reducing power by adaptively varying the power supply voltage. The first demonstrates that power can be reduced even further by buffering input data and averaging the processing rate over multiple periods of variable workload. The authors also show that while the quantization of power supply voltage levels can be quite coarse, they can still achieve nearly optimum power reduction. The second paper presents a dynamic programming technique for solving the multiple supply voltage scheduling problem in both pipelined and nonpipelined datapaths. An average energy savings of about 40% was realized on a set of standard benchmarks, using just four supply voltage levels.

The third paper presents a number of data encoding techniques for reducing the switching activity on the highly capacitive busses. These techniques include spatial and temporal redundancy addition and phase modulation. Average power reduction of 30–60% is reported. The next paper derives an information-theoretic lower bound on the average Hamming distance per transition which is valid for any state assignment of a given finite state machine (FSM). This bound

is useful in providing clues about the type of FSM structures which are likely to have low activity per transition and hence low-power dissipation. The next paper presents a gate-sizing approach that can take realistic gate delay and power models and obtain power optimization under delay constraints using a combination of local perturbations, multiple resizing moves, and relaxation techniques. Experimental results show that power savings between 5–30% are possible. The next paper describes a gate-level simulator for power and current evaluation in CMOS integrated circuits. The simulator speed is comparable to traditional gate-level simulators, but its accuracy is higher. This is mainly due to symbolic modeling of the CMOS cells which explicitly captures dependence on the input patterns and I/O conditions without actually using look-up tables.

Finally, two Transactions Briefs will appear in a Special Section of the March 1998 issue. The first brief presents a distribution-independent statistical sampling technique based on the properties of order statistics to estimate the average power dissipation of an integrated circuit. The main feature of this technique is its nonparametric stopping criterion which is more robust than the current parametric criteria based on the central limit theorem. Finally, the second brief describes two new designs for asynchronous sequencers which increase the throughput of the entire system. In addition, the paper shows how to modify the latches in the datapath to avoid data hazards when using these sequencers in dual-rail or single-rail datapaths. Results show that after voltage scaling, energy dissipation of the system may be reduced by a factor of 2.5 compared to a sequential design.

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The Guest Editors would like to thank the authors and the numerous reviewers for their excellent work in producing these high-quality papers, which represent a cross section of the papers presented at ISLPED'96. They would also like to thank Dr. D. Bouldin, former Editor-in-Chief, for his encouragement and support in providing this special issue forum for presentation of these papers.

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Dr. Barton was Co-Chairman of the Technical Program Committee for the 1996 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED'96), and is Co-General Chairman of ISLPED'97.

Massoud Pedram received the B.S. degree in electrical engineering from the California Institute of Technology, Pasadena, in 1986 and the M.S. and Ph.D. degrees in electrical engineering and computer sciences from the University of California, Berkeley, in 1989 and 1991, respectively.

He is an Associate Professor of Electrical Engineering–Systems at the University of Southern California, Los Angeles. He was the cofounder and General Chair of the International Symposium on Low Power Design in 1995 and the Technical Co-Chair and General Co-Chair of the International Symposium on Low Power Electronics and Design in 1996 and 1997. He has given several tutorials on low power design at major CAD conferences and forums including ICCAD and DAC. He has published more than 100 journal and conference papers and co-edited a book on low power design methodologies. His research interests span many aspects of design and synthesis of VLSI circuits, with particular emphasis on layout-driven synthesis and design for low power.

Dr. Pedram is a recipient of the National Science Foundation's Young Investigator Award in 1994 and the Presidential Early Career Award for Scientists and Engineers (a.k.a., the Presidential Faculty Fellows Award) in 1996. His research has received a number of awards including an ICCD Best Paper Award, a DAC Best Paper Award, and an IEEE TRANSACTIONS ON VERY LARGE SCALE (VLSI) SYSTEMS Best Paper Award. He has served on the technical program committee of a number of conferences and workshops, including the Design Automation Conference and the European Design Automation Conference. He is an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN and of the *ACM Transactions of Design Automation of Electronic Circuits*.