

# RF CMOS Low-Phase-Noise $LC$ Oscillator Through Memory Reduction Tail Transistor

C. C. Boon, M. A. Do, K. S. Yeo, J. G. Ma, and X. L. Zhang

**Abstract**—Based on the understanding of flicker noise generation in “silicon metal-oxide semiconductor field-effect transistors” (MOSFETs), a novel method for improving the phase noise performance of a CMOS  $LC$  oscillator is presented. Zhou *et al.* and Hoogee have suggested that the  $1/f$  noise can be reduced through a switched gate, and the flicker noise generated is inversely proportional to the gate switching frequency. The novel tail transistor topology is compared to the two popular tail transistor topologies, namely, the fixed biasing tail transistor and without tail transistor. Through this technique, a figure of merit of 193 dB is achieved using a fully integrated CMOS oscillator with a tank quality factor of about 9.

**Index Terms**—CMOS oscillator, oscillator, phase noise.

## I. INTRODUCTION

THE challenge in the design of a fully integrated CMOS  $LC$  voltage-controlled oscillator (VCO) is to achieve a low-phase noise while maintaining low-power consumption. However, the integrated inductor usually has a poor quality factor and this greatly affects the phase noise performance. While efforts have been made to improve the phase noise performance by increasing the quality factor of the  $LC$  tank through the implementation of the bondwire [3], [4] or a special layout technique [5], others have sought to improve the phase noise performance through improving the  $LC$  VCO circuit topology [6], [7]. Despite these endeavors, the design and optimization of integrated  $LC$  VCOs still pose many challenges to circuit designers as far as practicality and cost are concerned.

Recently, it was recognized [8], [9] that the tail transistor may be the largest contributor to the phase noise in a VCO, especially to the  $1/f^3$  shaped phase noise close to the oscillation frequency [10]. The noise sources from the tail transistor can be categorized into high-frequency noise source and low-frequency noise source. The high frequency up-converted flicker noise source of the tail transistor at twice the oscillation frequency is down-converted into phase noise by a hard-switching oscillator. On the other hand, the low-frequency flicker noise source of the tail transistor contributes to the phase noise through various mechanisms, such as AM-to-PM conversion in the nonlinearity of the varactor [11], modulation of the bias point [12], modulation of tail capacitance and Groszkowski effect [13].

In this paper, a CMOS  $LC$  VCO using a new tail transistor topology to reduce the intrinsic flicker noise is introduced.

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The authors are with the Division of Circuits and System, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798 (e-mail: PH318870@ntu.edu.sg).

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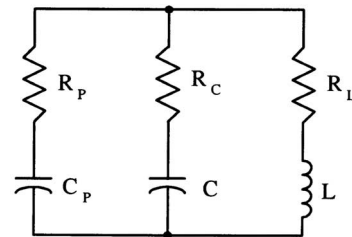


Fig. 1. Resonator tank.

In Section II, a new figure of merit (FOM) that takes into account the quality factor to better reflect the topology effect on the VCOs performance will be given. Sections III and IV discuss the topology of the novel VCO, and the comparison between the novel VCO and the VCO with a fixed biasing (FB) tail transistor topology as well as the VCO without tail (WT) transistor topology. Section V concludes the paper with an example of a VCO that meets the system specifications of the WCDMA/CDMA2000.

## II. FIGURE OF MERIT

Compared to [17], where the quality factor of the total parasitic capacitance  $Q_P$  is not taken into account, a more realistic oscillator's resonator is shown in Fig. 1. The quality factor of the inductor  $Q_L$  and the quality factor of the capacitor  $Q_C$  are modeled by series resistance  $R_L = \omega L/Q_L$  and  $R_C = 1/(Q_C \omega C)$ .  $C_P$  describes the loading capacitance due to the total parasitic capacitance of the cross-coupled transistors and the buffer, and the series resistance is given by  $R_P = 1/(Q_P \omega C)$ .  $C_P$  is mainly formed by  $C_{gs}$ ,  $C_{db}$ , and  $C_{gd}$  of the cross-coupled transistors and the buffer.

Then, the loaded quality factor  $Q$  of this resonator is obtained to be

$$\frac{1}{Q} = \frac{1}{Q_L} + \frac{1}{C + C_P} \left( \frac{C}{Q_C} + \frac{C_P}{Q_P} \right) \quad (1)$$

as compared to [14]

$$\frac{1}{Q} = \frac{1}{Q_L} + \frac{1}{C + C_P} \left( \frac{C}{Q_C} \right). \quad (2)$$

From the Leeson [18] heuristic expression for the phase noise ( $S_{SSB}$ ) of an  $LC$  VCO

$$S_{SSB} = F \frac{kT}{2P_{sig}} \frac{\omega_0^2}{Q^2 \Delta \omega^2} \quad (3)$$

where  $Q$  is the loaded quality factor of the resonator as defined in (1),  $\Delta \omega = 2\pi \Delta f$  is the angular frequency offset,  $P_{sig}$  is the

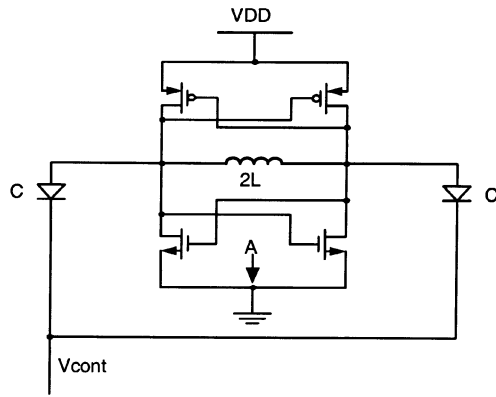


Fig. 2. WT transistor VCO.

average signal power (in watts) and  $F$  is the device noise excess factor. The equation was verified in [13].

A normalized phase noise has been defined as a FOM for oscillators [14]

$$\text{FOM} = \left( \frac{\omega_0}{\Delta\omega} \right)^2 \frac{1}{P_{\text{vco}} S_{\text{SSB}} [\text{mW}]} \quad (4)$$

where  $P_{\text{vco}}$  is the total power consumption of the VCO in milliwatts.

Therefore, from (3)

$$\text{FOM} = \frac{2}{F} \frac{P_{\text{sig}}}{P_{\text{vco}}} \frac{1}{kT} (Q^2) \quad (5)$$

which shows that the FOM is proportional to the squared quality factor of the resonator.

In order to compare between VCOs with different  $Q$  to reflect a change in performance that is independent of  $Q$ , for example, due to topological causes, (5) must be normalized. An arbitrary value of  $Q = 10$  is taken as the nominal value, the normalized FOM is

$$\text{FOM}_{\text{NORM}} = \text{FOM} \left\{ \frac{10}{Q} \right\}^2. \quad (6)$$

In this paper, both (5) and (6) will be used.

### III. VCO TOPOLOGIES

In this section, three VCO topologies, namely, VCO WT transistor, VCO with a FB tail transistor, and VCO with memory reduced tail transistor (novel topology) will be discussed.

#### A. WT Transistor Topology

The operation of the WT transistor topology shown in Fig. 2 is as follows. When the oscillation condition is satisfied, oscillation starts to develop. As the oscillation amplitude grows larger, it will reach a point where the negative resistance is not enough to support the positive resistance (loss) of the  $LC$  tank if the supply voltage and ground do not first clip the maximum swing. This is where the amplitude stops growing and a stable oscillation is reached.

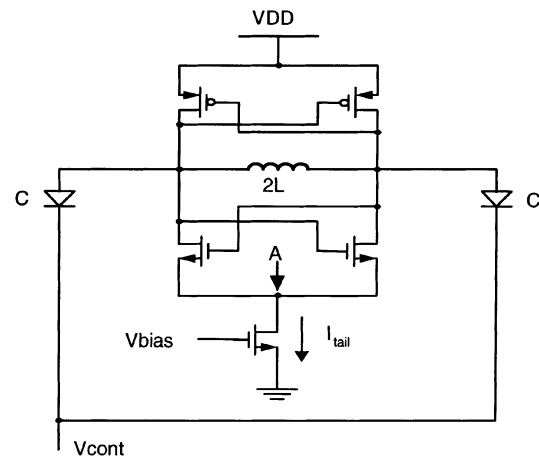


Fig. 3. FB tail transistor VCO.

#### B. FB Tail Transistor Topology

Fig. 3 shows a FB tail transistor VCO. The tail transistor is designed to operate in the saturation region as a current source. Consequently, the tail current determines the oscillation amplitude. At the resonance frequency, the admittances of  $L$  and  $C$  cancel, leaving  $R_{\text{EQ}}$ , the equivalent parallel resistance of the  $LC$  tank, where

$$R_{\text{EQ}} = QL\omega. \quad (7)$$

The differential voltage swing across the tank is given in first approximation by

$$V_{\text{tank}} = I_{\text{tail}} R_{\text{EQ}}. \quad (8)$$

Equation (8) is valid as long as the active devices work in the saturation region [25]. As the amplitude grows closer to the supply voltage, the active devices will be driven into the triode region. The cross-coupled transistors now act as resistors in parallel with  $R_{\text{EQ}}$  or it can be viewed as a reduction in the absolute value of the negative resistance that balances  $R_{\text{EQ}}$ . Hence, additional loss is introduced to the VCO, which leads to a lower VCO quality factor.

#### C. Memory-Reduced Tail Transistor (Novel) Topology

Close-in phase noise of a CMOS oscillator is largely determined by the flicker noise originated by the tail transistor. Flicker noise modeling generally is based on two major existing theories, namely, the carrier number fluctuation model and mobility fluctuation model [20]. The carrier-density fluctuation model predicts an input referred noise density which is independent of the gate-biasing voltage and is proportional to the square of oxide thickness, while the mobility fluctuation model predicts an input referred noise voltage increasing with gate-biasing voltage and proportional to oxide thickness. An often used model as the basis for circuit simulations is the unified model [16], [21] with a functional form resembling the carrier-density fluctuation model at the low bias and the mobility-fluctuation model at the high bias.

The flicker noise is known for its long correlation time and an associated physical process which has a ‘‘long-term memory’’ [22], [23]. The ‘‘carrier trapping in localized oxide states’’ is

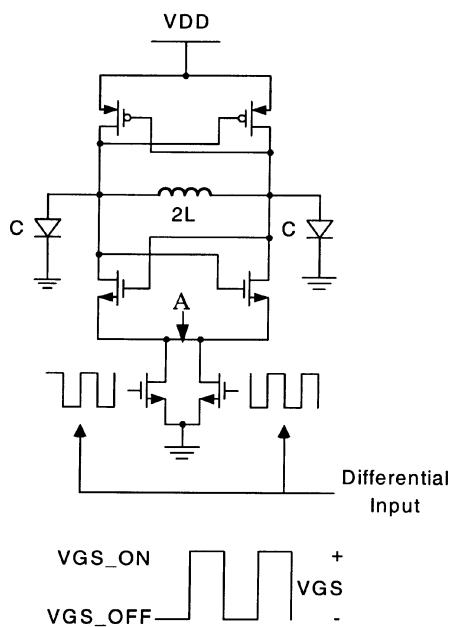


Fig. 4. Test setup for flicker noise.

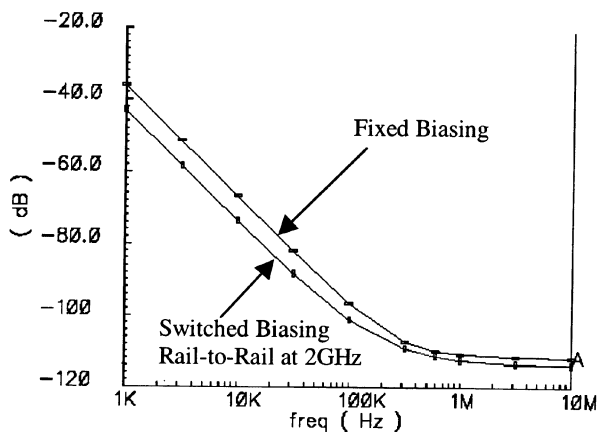


Fig. 5. Simulated baseband flicker noise for fixed and switched biasing conditions.

a process that plays a significant role in the generation of the flicker noise in a MOSFET. Moreover, the memory involved with the flicker noise is related to the long occupation time constants of the traps. As a switched transistor will force a trap to release its captured electron, rendering the transistor to be memory-less, the flicker noise will be reduced.

Fig. 4 shows the simulation setup to investigate the influence on the baseband power spectral density of the VCO tail transistor's flicker noise current due to the gate source voltage switching. For comparison, the gates of the two transistors are driven by a fixed biasing voltage and then by a switched biasing voltage from rail to rail at 2 GHz. As the supply current for both topologies are made the same, the difference in the phase noise at A is mainly due to the VCOs topology. The results are shown in Fig. 5. The amount of phase noise reduction using switched biasing compared to fixed biasing is about 8 dB at 1 kHz and 5 dB at 100 kHz, which agrees well with the measured results in [22] and [23].

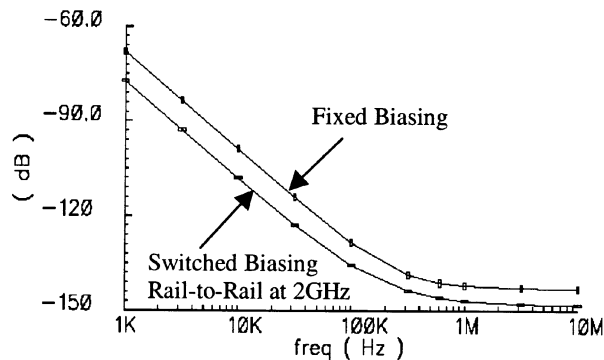


Fig. 6. Simulated second harmonic flicker noise for fixed and switched biasing conditions.

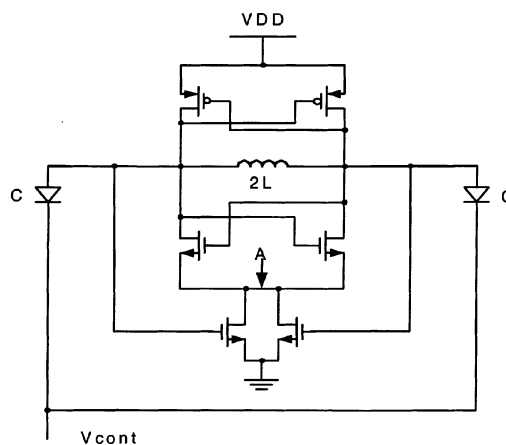


Fig. 7. Memory-reduced tail transistor VCO.

However, the low-frequency noise (baseband) does not directly produce phase noise, as discussed above. On the other hand, noise at the frequency around the second harmonic when down-converted, will become phase noise [24]. An examination on the second harmonic phase noise at A, is given in Fig. 6, which shows an improvement of phase noise of about 9 dB at 1 kHz and 6 dB at 100 kHz for the switched biasing topology over the fixed biasing topology. This is expected because less flicker noise is generated.

Fig. 7 shows the memory reduced tail transistor VCO. The operation of the novel oscillator is as follows. Initially, when the circuit is balanced, both the output voltage and current flowing in the two sides are set by the size of the tail transistors. The tail transistors will go into the saturation region first while the cross-coupled nMOS transistors are still in the cutoff region. When both the tail transistors and cross-coupled nMOS transistors are in the triode region, the tail transistors determine the current as the voltages at the source of the cross-coupled nMOS transistors are floating.

Since all the transistors in this VCO topology are switched biasing rather than fixed biasing, it is expected to have lower flicker noise [22], [23]. Moreover, as the transistors operate in the triode region for a large portion of the oscillation period, they exhibit lower current flicker noise than the transistors that operate in the saturation region, for example, the tail transistor in the FB topology [28].

#### IV. PERFORMANCE COMPARISON OF THE THREE VCO TOPOLOGIES

A comparison of the two conventional topologies with this novel topology will reveal the advantages and disadvantages of these VCOs.

The main advantage of the novel topology and WT topology over the FB topology is that without the tail transistor flicker noise source, the only flicker noise source now is the cross coupled transistors, which have an inherently lower flicker noise due to the switched biasing, resulting in better phase noise performance [22], [23].

Another disadvantage of the FB topology compared to the novel topology and WT topology, is that the tail transistor in the FB topology reduces the headroom available for oscillation by around 0.2 to 0.4 V in a CMOS 0.25 micron technology. The effect is not negligible for low voltage design. A smaller signal power  $P_{sig}$  has an adverse effect on the phase noise, as phase noise is essentially the noise to signal ratio of the VCO. The tail transistors of the novel topology mostly work in the triode region, the headroom requirement is negligible, while the WT topology can achieve the largest oscillation amplitude among the three topologies.

For the FB topology, extra circuitry is needed to provide biasing voltage to the tail transistor. This increases the power consumption and also introduces noise sources to the VCO. The noise current coming from the biasing network will be mirrored into the tail transistor. Both the novel topology and the WT topology do not encounter this problem.

The major obstacle in implementing the WT topology is the power consumption. This is especially true in the case of an over-designed loop gain. For the complementary LC oscillator, in order to maintain the oscillation, the loop gain condition is

$$(g_{mn} + g_{mp}) > \alpha_g(1/R_{EQ}) \quad (9)$$

where  $\alpha_g$  is the excess gain factor and typically from 2 to 3.  $g_{mn}$  and  $g_{mp}$  are the trans-conductances of the nMOS and pMOS cross-coupled transistors, respectively. The excess gain factor is a safety margin to guarantee oscillation. However, in the case of the WT topology, the VCO will consume a lot of “short-circuit current” that is useless to the functioning of the oscillator. For the same tank characteristics, which include the excess gain factor  $\alpha_g$  and the oscillation frequency, the WT topology has the highest power consumption while both the FB topology and the novel topology have the same power consumption.

Another disadvantage of the WT topology is its absence of the high tail transistor impedance in series with the cross coupled transistors to stop the transistors from loading the resonator in the triode region [24]. In a balanced circuit, the odd harmonics circulate in a differential path, while even harmonics flow in a common-mode path. The even harmonics that are usually dominated by the second harmonic components travel through the resonator capacitors and the cross-coupled transistors to ground. The high impedance acts to suppress the noise in the tail transistor by making it to appear noiseless to the VCO, thus improving the phase noise performance. Compared to the WT topology, the FB topology and the novel topology suppress

TABLE I  
SUMMARY OF THE PERFORMANCES OF THE THREE VCOs

	Without Tail Transistor (WT) Topology	Fixed Biasing Tail Transistor (FB) Topology	Memory Reduced Tail Transistor (novel) Topology
Power Consumption	1.7mA * 2V = 3.5 mW	1.4mA * 2V = 2.8mW	1.4mA * 2V = 2.8mW
Phase Noise	84dBc/Hz @10kHz Offset 126.6dBc/Hz @600kHz Offset	81dBc/Hz @10kHz Offset 126dBc/Hz @600kHz Offset	87dBc/Hz @10kHz Offset 127.6dBc/Hz @600kHz Offset
FOM @600kHz Offset	191.3dB	191.5dB	193dB

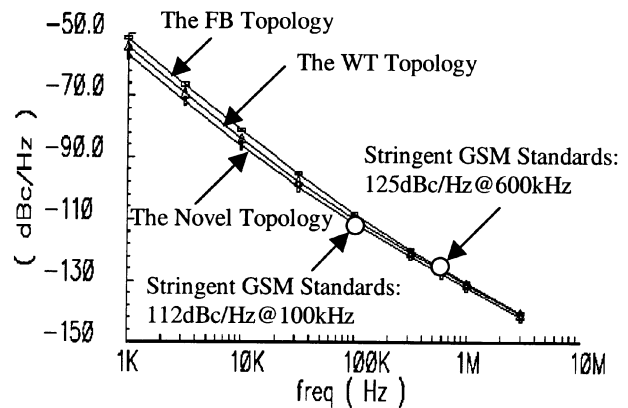


Fig. 8. Comparison of phase-noise performance for the three VCOs.

the second harmonic noise more and prevent the cross coupled transistors from loading the resonator. Thus, an improvement of phase noise in the  $1/f^3$  region is expected from the novel topology and the FB topology over the WT topology. However, the improvement on the FB topology is masked by the up-converted flicker noise of the tail transistor.

Finally, the FB topology is less susceptible to the frequency pushing effect, which is the frequency sensitivity to the voltage supply. Both the WT topology and the novel topology are affected by the frequency pushing effect.

For comparison, three VCOs with the same tank characteristics and oscillation frequency are designed and simulated using the three topologies. The excess gain factor  $\alpha_g$  is made to be 2.5 and the tank quality factor is about 9.

The oscillators are designed for GSM-1800 applications where the oscillation frequency is at 1.88 GHz and they are optimized for FOM. All the simulation models are extracted from the 0.25 micrometer IBM SiGe 6 HP process. However, only CMOS transistors are used in the simulation. The post-layout simulation performances of the VCOs for three topologies are summarized in Table I.

Fig. 8 shows the phase noise performances of the three VCOs, the stringent GSM specifications are given as circles in the figure. From Table I, it can be seen that the novel topology gives the maximum improvement of the phase noise of 6 dB from the FB topology and 3 dB from the WT topology while consuming lower power consumption than the WT topology.

TABLE II  
SPECIFICATIONS OF THE VCO

Tuning range	2.05GHz to 2.25GHz
Excess Gain Factor, $\alpha_g$	2.5
Estimated Tank Quality Factor	12
Phase Noise @ 600 kHz for 2.05GHz to 2.25 GHz	-129.2dBc/Hz to -129.3dBc/Hz
Phase Noise @ 8 MHz for 2.05GHz to 2.25 GHz	-152dBc/Hz to -152.5dBc/Hz
Power Consumption	4.2mA*2V = 8.4mW

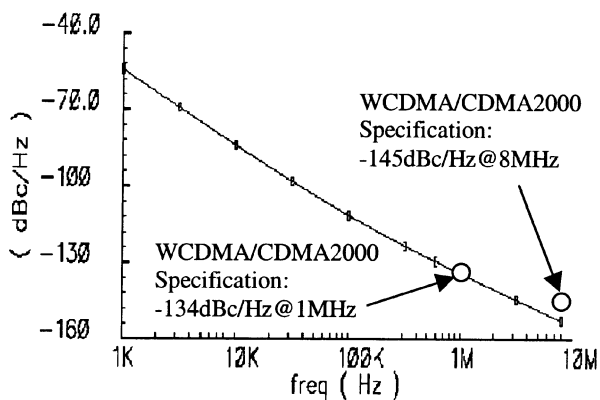


Fig. 9. WCDMA/CDMA2000 VCO using the novel circuitry.

The novel topology also shows the best FOM of 193 dB, which corresponds to a normalized FOM of 194 dB using (6).

In summary, the advantages of the novel topology are that it has a superior phase noise performance to that of the FB topology while it has lower power consumption than the WT topology, which gives this novel topology an edge over the other two topologies.

## V. CONCLUSION

To date, few VCOs have met the specifications of the WCDMA and CDMA2000 standards due to the stringent phase noise requirement. This is especially true for fully integrated VCOs due to the low inductor Q. Using the novel topology, a VCO optimized for phase noise performance is designed. The specifications of the VCO are shown in Table II.

Fig. 9 shows the phase noise performance of the VCO, and the WCDMA/CDMA2000 specifications are given as circles. It is shown that the VCO has exceeded the standard specifications with a low power consumption of 8.4 mW. The FOM for this VCO at 600 kHz offset is 191.5 dB. As a conclusion, the performance of the novel VCO and other state-of-the-art designs are compared in Table III.

From Table III, it can be seen that the novel VCO is one of the best in terms of FOM. [24] implementing a noise filtering technique has the best FOM. However, the noise filter requires a large inductor of 10 nH and a capacitor of 40 pF, thus limiting its practical uses due to cost. The next best VCO with FOM of 187 has a tank with a quality factor of 20 while the tank quality factor for the novel VCO is about 9.

TABLE III  
PERFORMANCE COMPARISON OF THIS WORK WITH OTHER  
STATE-OF-THE-ART OSCILLATORS

Ref.	Type	$f_0$ (Hz)	$\Delta f$ (Hz)	Phase Noise @ $\Delta f$ (dBc/Hz)	Power (mW)	FOM (dB)
[26]	FB	1.93G	600k	-122.2	27.6	177.9
[27]	FB	1.80G	3M	-130.0	6.0	177.8
[15]	FB	1.10G	600k	-126.0	12.7	180.2
[14]	WT	1.80G	3M	-143.0	20.0	185.5
[24]	FB	1.20G	3M	-153.0	9.2	196.0
[5]	FB	1.57G	600k	-133.5	30.0	187.0
<b>This-GSM</b>	<b>Novel</b>	<b>1.88G</b>	<b>600k</b>	<b>-127.6</b>	<b>2.8</b>	<b>193.0</b>
<b>This-GSM</b>	<b>FB</b>	<b>1.88G</b>	<b>600k</b>	<b>-126.0</b>	<b>2.8</b>	<b>191.5</b>
<b>This-GSM</b>	<b>WT</b>	<b>1.88G</b>	<b>600k</b>	<b>-126.6</b>	<b>3.5</b>	<b>191.3</b>
<b>This-WCDMA/CDMA2000</b>	<b>Novel</b>	<b>2.20G</b>	<b>600k</b>	<b>-129.5</b>	<b>8.4</b>	<b>191.5</b>

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