Continuous-Time Integrated FIR Filters at Microwave Frequencies

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***Abstract*—We discuss adaptive integrated finite-impulse response (FIR) filters operating in the continuous time domain. These filters become attractive to implement at microwave frequencies. An important topological property of the traveling wave FIR filter is presented, and its advantages when used as an adaptive equalizer are pointed out. Design considerations and modeling aspects of compact on-chip delay lines are given. Simulation results for an adaptive equalizer operating at a data rate of 10 Gb/s are presented.**

I. Introduction

RAPID SCALING of bandwidth in optical networks have resulted in deployment of optical time division multiplexed (OTDM) systems with bit rates as high as 10 and 40 Gb/s. At these data rates, there are significant link penalties associated with optical fiber impairments like chromatic dispersion and polarization mode dispersion (PMD). While techniques do exist to correct for impairments, they work in the optical domain. Further signal-to-noise ratio (SNR) penalties are incurred due to packaging parasitics and their variations during manufacturing. Electronic solutions to the problem are attractive due to their potential low cost. Since fiber impairments vary with environmental conditions, these solutions will necessarily have to be adaptive. It is in this context that adaptive electronic equalizers are used. By now, equalization as a technique is well known and equalizers of high complexity are routinely used in most channels, ranging from telephony to hard disk drives. While the optical channel is more "benign" when compared to some of the channels referred to above, the main challenge lies in being able to implement well known DSP techniques at speeds of several tens of gigabits per second [1]. It is in this context that adaptive filters are used in optical transceivers.

Fig. 1 shows a candidate receiver architecture employing an *all analog* adaptive finite-impulse response (FIR) filter followed by a decision device. In the filter, transmission lines are used to produce delayed replicas of the input. While such an approach would lead to physically large equalizers at low frequencies, it becomes attractive at very high speeds due its low power dissipation (compared to a digital implementation) even while operating a several tens of gigabits per second. These types of filters, referred to as continuous-time FIR filters are analyzed in this paper, where emphasis is placed on integrated circuit implementation. The reader is referred to [2] for a description of such filters built using discrete delay structures.

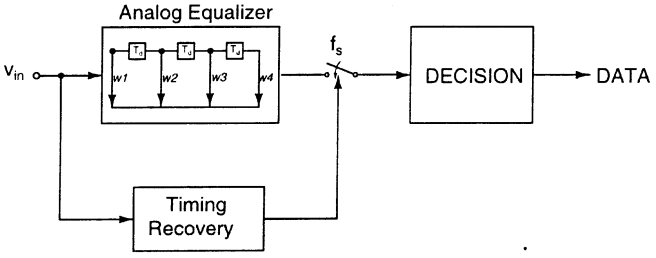

Fig. 1. An analog adaptive equalizer followed by a decision device.

The outline of this paper is as follows. In Section II, we consider a conventional tapped delay line structure, as inspired from DSP. The effects of impedance mismatch at the ends of the transmission line, and uniformly distributed series loss are analyzed. The traveling wave FIR filter, and its fundamental topological advantages relative to a conventional tapped delay line structure are shown in Section III. Delay line design and modeling are discussed in Section IV. Simulation results are presented in Section V and conclusions are given in Section VI.

II. Topological Considerations

A conventional tapped delay line filter, topologically inspired by discrete time FIR filter techniques is shown in Fig. 2, which, for illustrative purposes has three taps. The delays are implemented using transmission lines with a characteristic impedance of Z_o and length T seconds. A transconductor of value G is used to convert the input voltage to a current, which drives the delay line. Taps are implemented by transconductors with values w_1, w_2, and w_3 as shown. Summation of the tapped signals is done in the current domain, and the output voltage is developed across a load resistor of value $0.5R_T$ (this particular value is chosen in order to facilitate comparison with another topology, and will become clear shortly). The impulse response (Fig. 2) of the filter can be expressed as

$$h(t) = (R_T/2)(w_1 h_{v1}(t) + w_2 h_{v2}(t) + w_3 h_{v3}(t)) \qquad (1)$$

where $h_{v1}(t), h_{v2}(t)$, and $h_{v3}(t)$ are the impulse responses at nodes $v1, v2$, and $v3$, respectively. If $R_T = Z_o$

$$h(t) = G\left(\frac{Z_o}{2}\right)^2 (w_1\delta(t) + w_2\delta(t-T) + w_3\delta(t-2T)). \quad (2)$$

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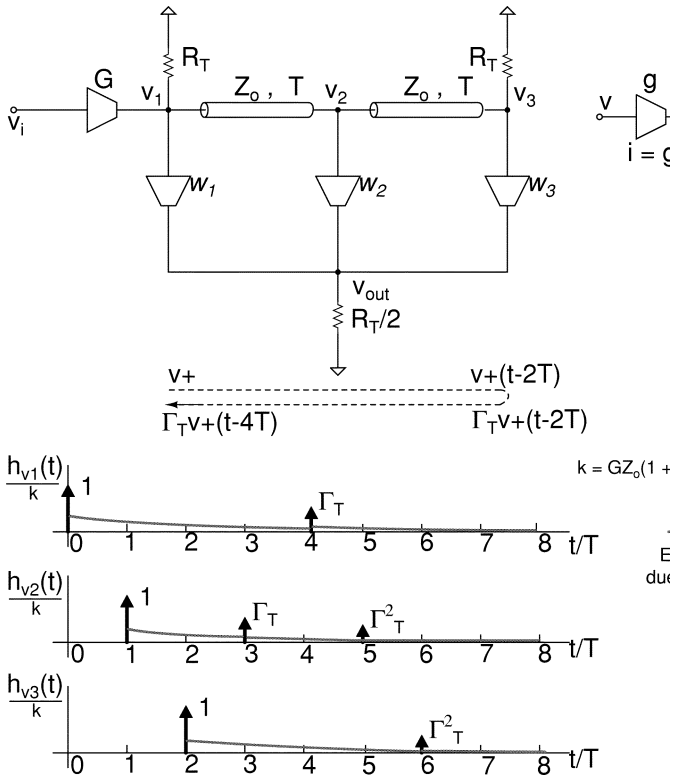

Fig. 2. $h_{v1}(t), h_{v2}(t)$, and $h_{v3}(t)$ in the presence of reflections for a tapped delay line structure.

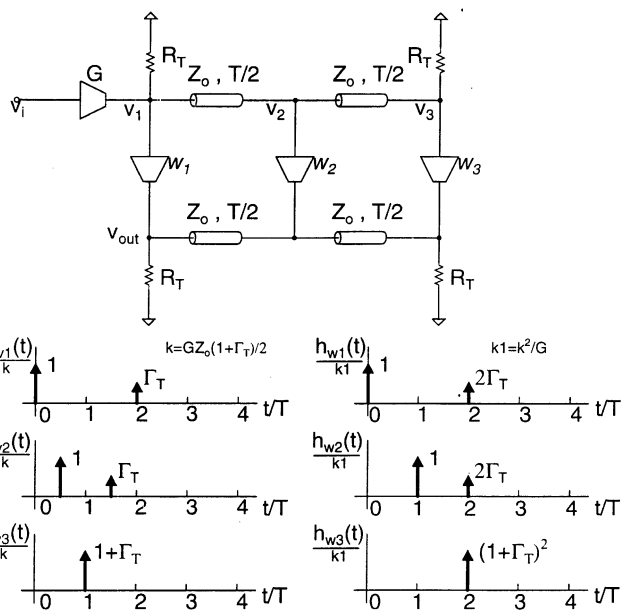

Fig. 3. The traveling Wave FIR structure and $h_{w1}(t), h_{w2}(t)$, and $h_{w3}(t)$ in the presence of reflections.

In practice, impedance mismatch at the ends of the delay line will cause reflections. We denote the reflection coefficient by Γ_T, which is given by $(R_T - Z_o)/(R_T + Z_o)$. $h_{v1}(t), h_{v2}(t)$, and $h_{v3}(t)$ are modified due to reflections as shown in Fig. 2. (For the time being, neglect the parts of the waveforms drawn in gray.) In cases of practical interest, $|\Gamma_T|$ will be of the order of 0.1, since this depends on mismatch between Z_o and R_T. Further, post equalization SNRs are of the order of 20 dB. Given this, one can safely neglect terms of the order of Γ_T^2 in comparison with Γ_T. Assuming that $R_T \approx Z_o(1 + 2\Gamma_T)$, the impulse response of the filter can be approximated as

$$h(t) \approx G\left(\frac{Z_o}{2}\right)^2 (1+3\Gamma_T)[(w_1\delta(t) + w_2\delta(t-T) + w_3\delta(t-2T) + w_2\Gamma_T\delta(t-3T) + w_1\Gamma_T\delta(t-4T))]. \quad (3)$$

It can be shown, that when there is uniform series loss series loss as well as mismatch at the terminations, $h_{v1}(t), h_{v2}(t)$, and $h_{v2}(t)$ would look like that shown in Fig. 2, with the exponentially decaying tails, drawn in gray. The amplitude of these tails is proportional to (R_s/Z_o), where R_s is the total series resistance per section of the line. In practice, this should be made small.

The key points to note from the discussion in this section are as follows.

1) Reflections at the ends of the delay line and series losses in the line cause the filter impulse response to "spill" over its ideal span (which for the three tap case considered above is $2T$). If the reflection coefficient and series loss is small, then the span of the impulse response with impedance mismatch is twice the span of the ideal impulse response.
2) It is not possible to constrain the impulse response of the filter to within the span of the ideal filter, by manipulating the tap weights w_1, w_2, and w_3. This is clear from (3).
3) From observation in (2), it is clear that if the filter is used in the context of adaptive equalization to compensate for channel intersymbol interference (ISI), this topology is more likely to worsen the problem than mitigate it.

III. Traveling Wave FIR Filters

Consider the filter structure shown in Fig. 3. Topologically, it is equivalent to a traveling wave amplifier, but with the output being taken at the "antisync" end [3]–[5]. While the possibility of using this structure as an FIR filter has been pointed out in the literature, its robustness, especially in the context of adaptive equalization, does not seem to have been adequately appreciated.

The filter has two sections of cascaded transmission lines, one on the input side and one on the output side. The impulse response of the filter is written as

$$h(t) = w_1 h_{w1}(t) + w_2 h_{w2}(t) + w_3 h_{w3}(t). \quad (4)$$

$h_{w1}(t)$ is the impulse response of the filter with $w1 = 1$ and $w2, w3 = 0$. $h_{w2}(t)$ and $h_{w3}(t)$ are similarly defined. These responses are shown in Fig. 3, where $h_{v1}(t), h_{v2}(t)$, and $h_{v3}(t)$ are shown on the left. In these plots, all terms of the order of Γ_T^2 and higher have been neglected. It is easily seen that $h_{w1}(t) = h_{v1}(t) * h_{v1}(t)/G$. Since $h_{v1}(t) \approx G((Z_o)/2)(1+\Gamma_T)(\delta(t) + \Gamma_T\delta(t-2T))$, we have

$$h_{w1}(t) \approx G\left(\frac{Z_o}{2}\right)^2 (1+\Gamma_T)^2[\delta(t) + 2\Gamma_T\delta(t-2T)]. \quad (5)$$

This is plotted on the right side of Fig. 3. Similarly, it can be shown that

$$h_{w2}(t) \approx G\left(\frac{Z_o}{2}\right)^2 (1+2\Gamma_T)[\delta(t-T)+2\Gamma_T\delta(t-2T)] \tag{6}$$

$$h_{w3}(t) \approx G\left(\frac{Z_o}{2}\right)^2 (1+\Gamma_T)^2\delta(t-2T). \tag{7}$$

Using (4), and the results shown, $h(t)$ is approximated as

$$h(t) \approx G\left(\frac{Z_o}{2}\right)^2 (1+\Gamma_T)^2[w_1\delta(t)+w_2\delta(t-T) +(w_3+2\Gamma_T w_1+2\Gamma_T w_2)\delta(t-2T)]. \tag{8}$$

We see the following.

1) If the reflection coefficient is small, then the span of the impulse response with impedance mismatch is *the same* as the span of the ideal impulse response.
2) Reflections cause tap weight "contamination." In the example discussed, we see that even if $w3$ is set to zero, there is a component of the impulse response at $t = 2T$. This can be corrected by using a modified value for $w3$, which is seen to be $w3' = w3 - 2\Gamma_T w_1 - 2\Gamma_T w_2$. In general, if $\mathbf{w_{ext}}$ is the externally applied $n \times 1$ tap weight vector, then the modified weights $\mathbf{w_{act}}$ due to reflections and series loss are a linear transformation of $\mathbf{w_{ext}}$ and are written as $\mathbf{w_{act}} = \mathbf{A}\mathbf{w_{ext}}$. In the three tap example, considered

$$\mathbf{w_{act}} = (1+\Gamma_T)^2 \begin{bmatrix} 1 & 0 & 2\Gamma_T \\ 0 & 1 & 2\Gamma_T \\ 0 & 0 & (1+\Gamma_T)^2 \end{bmatrix} \mathbf{w_{ext}}.$$

   From this equation, it is apparent that the traveling wave FIR filter can be made to look like an "ideal" FIR filter by predistorting the externally applied weights in the reverse fashion, i.e., by premultiplying the external tap weight vector $\mathbf{w_{ext}}$ by $\mathbf{A^{-1}}$.
3) Given that typical reflection coefficients achievable without using special trimming techniques are of the range $|\Gamma_T| < 0.05 - 0.1$, corresponding to resistor mismatch between 10%m–20%, it is seen that a traveling wave FIR structure is at least an order of magnitude improvement over the conventional structure shown in Fig. 2, as far as residual induced "ISI" terms outside the equalizer span are concerned.

A. Discussion and Simulation Results

Fig. 4(a) shows the simulation setup. A 10-Gb/s nonreturn-to-zero (NRZ) pseudo random bit stream, filtered with a 7.5-GHz fourth-order Bessel filter is the input to a six-tap FIR filter with a tap spacing of 50 ps. Fig. 4(b) shows the corrected first tap response of a tapped delay line type FIR filter. By "corrected response," we mean that the tap weights are so predistorted to cancel out effects of reflection and series loss as much as possible. From (3), it is clear that this is possible only to a certain extent for this topology, and residual "wander" is distinctly seen in the eye diagram.

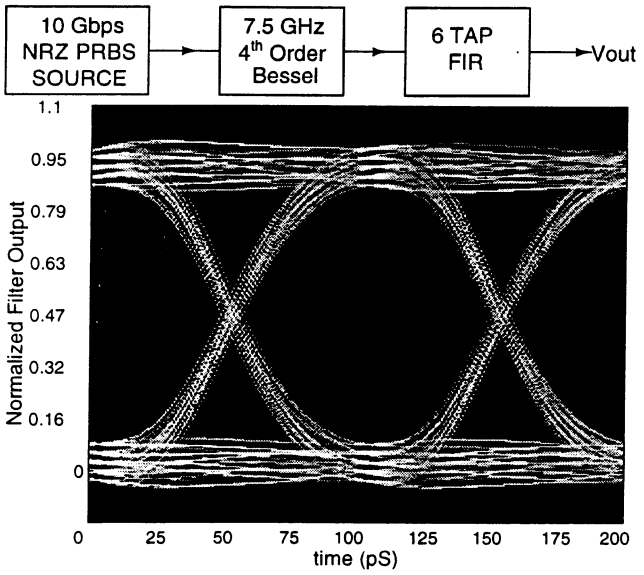

Fig. 4. (a) Simulation setup. (b) Corrected single tap eye for a tapped delay line filter—$\mathrm{R_T} = 60\ \Omega, \mathrm{R_s} = 4\ \Omega/\mathrm{tap}$, and $\mathrm{Z}_o = 50\ \Omega$.

Fig. 5 shows the raw and corrected first tap responses of a TWA-type FIR filter. Notice that the raw response has a lot of "wander," just like in the tapped delay line case. The magnitude of the wander is higher because of reflections on both input and output lines. However, most of this is confined to the equalizer span and can be corrected by appropriate predistortion of the tap weights. The result of this modification of tap weights is the eye diagram shown on the right in Fig. 5. From the discussion, it is seen that the *low-frequency* response of the equalizer plays a very important role in addition to its high-frequency bandwidth.

B. Choice of Tap Spacing, and Effect of High-Frequency Conductor and Dielectric Losses

The tap spacing can be made equal to one-half the symbol rate so that the equalizer implements a matched filter-symbol spaced equalizer cascade. Small variations in tap spacing around the nominal value are not critical, and unlike a digital implementation, where sampling rate has to be doubled, no particular penalty is incurred by reducing the tap spacing relative to a symbol interval. The frequency response of the filter with ideal transmission lines is periodic with period $1/T$, but high-frequency conductor and dielectric losses (presumably due to skin effect and dielectric losses) cause attenuation of the "image" responses. This might actually be to our benefit, as this filters out high-frequency noise prior to the sampling operation.

IV. Delay Element Design and Modeling

The physical size of the delay element determines the area occupied by the FIR filter. It is, therefore, important to be able to maximize the delay per unit area occupied by the delay element. A high bandwidth delay line (a transmission line) may be realized (approximately) on an integrated circuit (IC) by using structures such as microstrip lines, coplanar waveguides etc. In silicon technology, a dispersion less transmission line operating in the TEM mode has a phase velocity of about 150 μm/s. A 25 ps delay (as would be needed for a (T/2) spaced equalizer

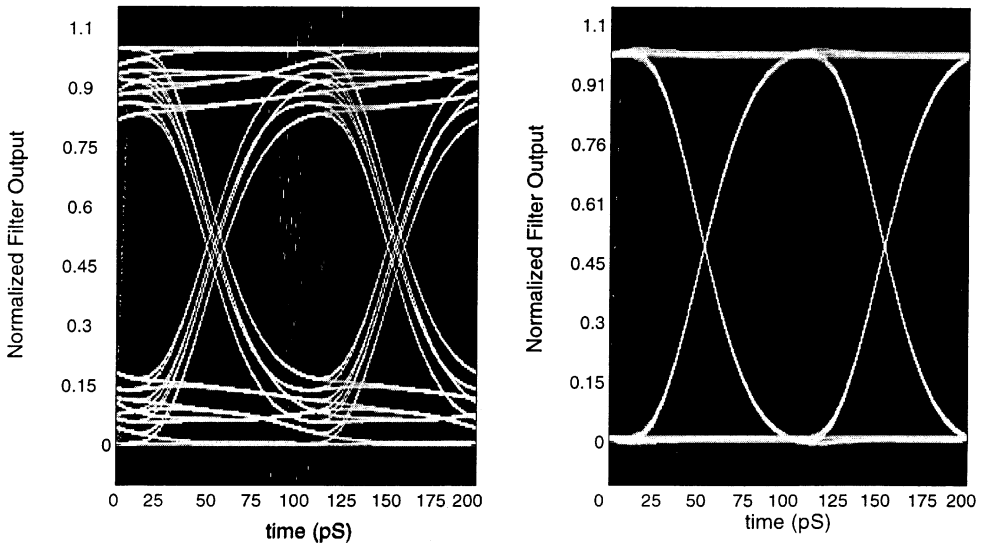

Fig. 5. Raw (left) and corrected (right) eye diagrams for a TWA FIR filter. $\mathrm{R_T} = 60\ \Omega, \mathrm{R_s} = 4\ \Omega/\mathrm{tap}$, and $\mathrm{Z}_o = 50\ \Omega$.

for a symbol rate of 10 Gb/s) would necessitate a line of about 3.75-mm long. This has two disadvantages—first, the series resistance of such a transmission line would be prohibitively high. Second, the aspect ratio of a filter designed using these delay elements would be very large and impractical. The aspect ratio can be made manageable by using meanders, but this does not solve the problem of high series resistance.

The key to reducing the size of the delay elements is to recognize that their bandwidth need not be significantly higher than the bandwidth of the input signal, so that lumped elements may be used to realize them. The frequency content of the input decides how much "lumpiness" we can tolerate for an *LC* based delay line. Further, a lumped *LC* section, with the inductor implemented as a planar spiral can be expected to realize a high delay per unit area since mutual inductance between successive turns can be exploited in order to reduce space occupied by the delay cell.

A. Patterned Ground Shield Delay Line

Based on the discussion, it is clear that one approach to reduce the size of the delay element, while obtaining a wide bandwidth, is the following strategy.

1) Design a spiral inductor with a sufficiently low series resistance. This is required so as to keep $|\Gamma_S|$ low.
2) Distribute the desired capacitance $C = (T_d^2)/L$ as uniformly as possible across the entire spiral. This can be done by placing a ground shield below the spiral. However, a fully conducting metal plate placed right below the inductor would largely cancel the effective inductance due to image currents induced in the shield. The solution to this problem is to pattern the ground shield so as to break the paths for the image current. For a given IC fabrication technology, the nominal spacing between metal layers is fixed. To get the highest delay, choose the metal layer closest to the spiral, as this maximizes the capacitance per unit area. Fig. 6(a) shows a patterned ground shield delay line.

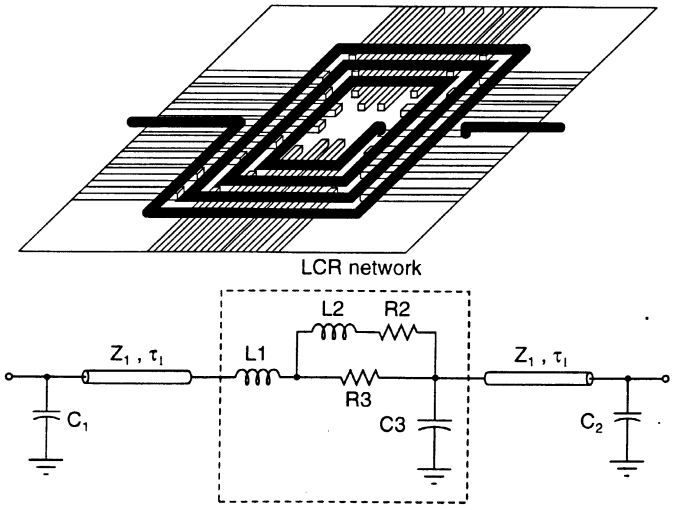

Fig. 6. A patterned ground shield delay line and broadband circuit model.

Patterned ground shield inductors have been proposed and used extensively in narrowband circuits [8], [9]. In these circuits, the ground shield is used to reduce inductor loss due to substrate effects. Further, the shield also reduces inductor signal coupling into the substrate. In narrowband circuits, the emphasis is on obtaining a high value of inductance with a small parasitic capacitance. Hence, the ground shield is implemented in a metal layer *far away* from the inductor. In the design of a delay line, however, notice that one would like a shield very close to the inductor in order to reduce the size of the delay line.

B. Delay Line Modeling for Circuit Simulation

Planar inductors are usually modeled using lumped elements. This is generally adequate for narrowband circuit design. In our case, however, it is necessary that the circuit model fit EM simulations (or measurements) accurately over the symbol rate and beyond. We also require that the model be amenable to transient simulation. This implies that frequency dependent inductances and resistances, which are commonly used in narrowband

models, should not be employed, as such elements are not part of most simulator libraries. Lossy transmission lines were not used as a part of the models in this work due to problems with inconsistency of ac and transient responses in the circuit simulator used in this work. Almost all SPICE-like simulators have ideal transmission lines as part of their library. One must therefore find a circuit model for the delay line structure that uses only resistors, inductors, capacitors and ideal transmission lines, and fits EM simulation or measurement data over a frequency band beyond the spectrum of the input signal. The FIR filter consists of many cascaded delay lines. So, even small errors between the model and data tend to accumulate when the entire filter is simulated. This underscores the importance of having an accurate fit to the data over the entire frequency band.

Intuitively, the delay line behaves like a transmission line at low frequencies. The characteristic impedance and delay are still unknown. It helps to have an estimate of these values, as they act as initial conditions for any optimization routine we might want to use to fit the simulation data to the circuit model. In this work, a free planar EM simulator (SONNET-LITE) was used. A spiral delay line was characterized in a 50-Ω environment. *Assuming* that the delay line behaves like an ideal lossless transmission line, its characteristic impedance Z_1 is calculated from [6] and [7]

$$Z_1 = 50\ \Omega\sqrt{\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}}. \tag{9}$$

Once Z_1 is approximately known, all S-parameter calculations are now performed with this as the reference impedance. Then, one can expect that within the bandwidth of the delay line, $|S_{21}|, |S_{12}| \approx 1$ and $|S_{11}|, |S_{22}| \ll 1$. The approximate delay of the spiral τ can be found from the group delay of S_{21}.

The circuit model used in this work is shown in Fig. 6(b). The motivation for using this topology is as follows. The feed lines to the inductor have a lower characteristic impedance compared to the spiral. Since they are electrically short, they are modeled as capacitors C_1 and C_2. The transmission lines have a characteristic impedance approximately equal to Z_1, determined from (9). The LCR network models the losses and "lumpiness" of the spiral. We found that running a circuit optimizer to fit Z_1, τ_1, C_1, C_2 and the elements inside the LCR network with bad initial conditions resulted in very poor agreement of data and model. So the following strategy was used. We know approximately the value of Z_1 and τ. Further, C_1 and C_2 can be expected to be small and so probably influence only S_{11} and S_{22}. If the LCR circuit in Fig. 6(b) is replaced by a thru, $|S_{21}|$ would be unity. Any deviation from this value is due to the LCR network. We, therefore, tried to fit a simple LCR network to the *magnitude* of S_{21}. For a well-designed delay line, this would be relatively flat in the desired "passband" and fall of with gentle slope beyond the useful frequency range of the line. A simple LCR network is therefore adequate to model this effect. The LCR circuit topology used in this paper is shown in the box in Fig. 6(b). Once a good fit is obtained for $|S_{21}|$, the group delay of the network τ_{LCR} can be obtained. τ_1 is calculated from $\tau = 2\tau_1 + \tau_{\mathrm{LCR}}$. We found that using these values for τ_1, Z_1, the LCR network elements and estimates for C_1 and C_2 as the initial conditions for the optimization results in a very good fit to the data over a very wide bandwidth.

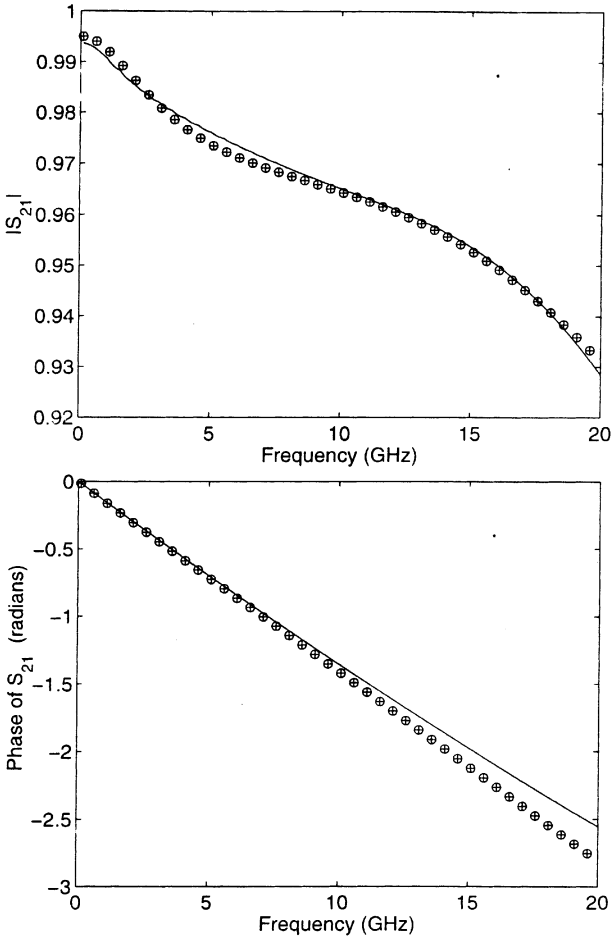

Fig. 7. Magnitude and phase of S_{21} reference impedance is 120 Ω (–model, $\bigoplus$ EM simulation).

A square spiral delay line with about 25-ps delay was designed in a modern SiGe IC process with six levels of metal and bipolar transistor $f_T's$ in excess of 120 GHz. The topmost metal layer in the process has low resistivity (about 10 m$\Omega/\square$). The spacing between this layer and the metal layer below it is about 4 μm. EM simulations were run in a 50-Ω environment and the characteristic impedance of the spiral, estimated from (9), was found to be approximately 120 Ω. The circuit model and EM simulations are compared in Fig. 7.

V. Simulation Results

In this section, we present simulation results of a traveling wave FIR equalizer, operating on a 10–Gb/s NRZ bit stream passing through a channel $0.5\delta(t) + 0.5\delta(t - 0.8T_b)$ (intended to model a first-order PMD channel over single-mode optical fiber), with $T_b = 100$ ps. The transconductors used for implementing the variable taps weights are simple differential pairs, buffered at the input by emitter followers. Weights are tuned by changing the tail currents. The bandwidth of these transconductors is much higher than the bit rate. In any case, their finite bandwidth is not a problem, as this is equivalent to a further impairment in the channel and can be compensated for by the adaptive filter.

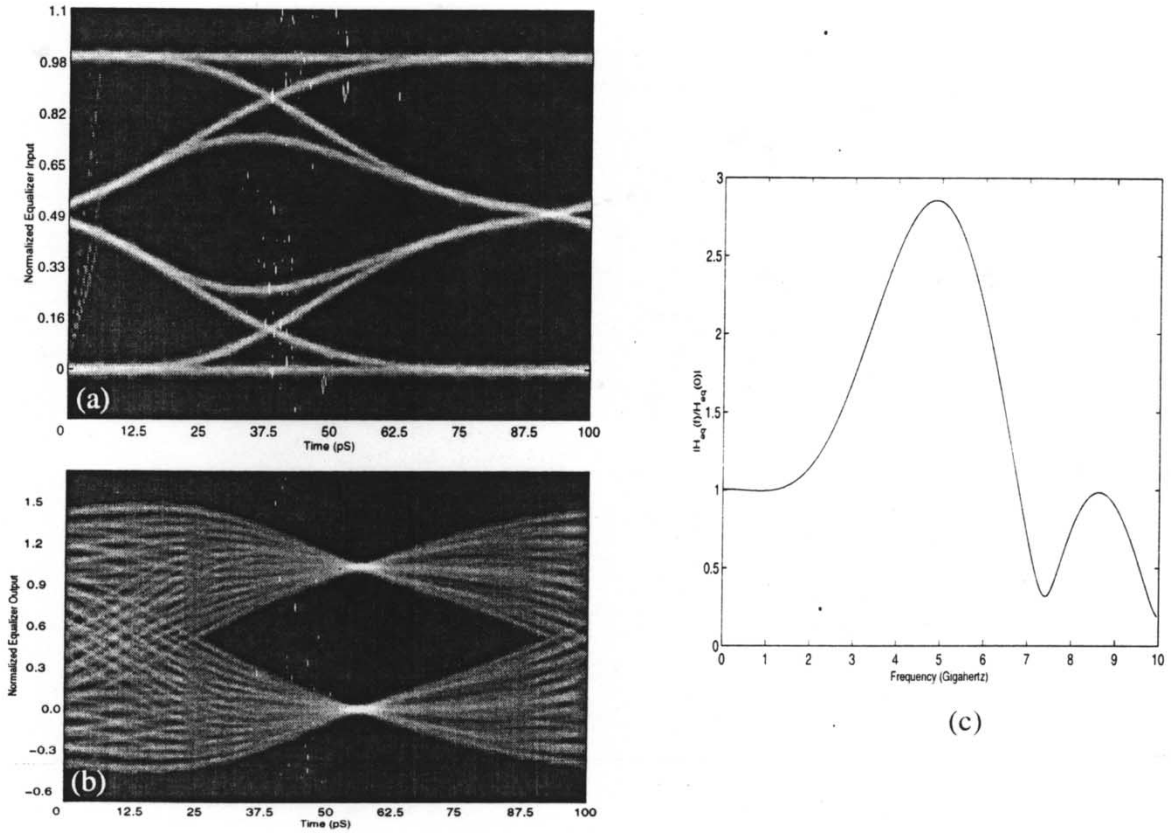

Fig. 8. Eye diagram. (a) Equalizer input. (b) Equalizer output. (c) Equalizer frequency response.

The block diagram of the simulated system is as shown in Fig. 4(a), except that a ten-tap equalizer is used, and the channel model is inserted between the equalizer and the transmit filter. The eye diagram at the input of the receiver is shown in Fig. 8(a). The equalizer is implemented using spiral delay lines of the type discussed in Section IV. The delay per line is approximately 24 ps, making the "tap spacing" 48 ps. R_s/Z_o is about 0.04, and Γ_T was deliberately made 0.05 at low frequencies. Since the impulse responses corresponding to each tap are known, the optimum tap weights were computed *a priori* using well-known techniques [10]. Here, the "optimum weights" mean that weight vector that result in the least ISI upon sampling the output of the equalizer at intervals of T_b seconds. Fig. 8(b) shows the equalized eye diagram, where the maximum eye opening corresponds to the times at which the output is sampled. The frequency response of the equalizer is shown in Fig. 8(c). Note the boost in the response around 5 GHz.

VI. Conclusion

We discussed the potential of analog FIR filters operating in the microwave frequency range. In the presence of practical nonidealities like impedance mismatch and series loss, it was shown that the traveling wave FIR filter topology is a big improvement over a conventional tapped delay-line filter. Simulation results for a ten-tap equalizer operating on a 10-Gb/s NRZ bit stream corrupted by ISI were given.

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