Using the Weak Inversion Region to Optimize Input Stage Design of CMOS Op Amps

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***Abstract*—Operation of MOS devices in the strong, moderate, and weak inversion regions is considered. The advantages of designing the input differential stage of a CMOS op amp to operate in the weak or moderate inversion region are presented. These advantages include higher voltage gain, less distortion, and ease of compensation. Specific design guidelines are presented to optimize amplifier performance. Simulations that demonstrate the expected improvements are given.**

***Index Terms*—Input stage, low-distortion, weak inversion.**

I. Introduction

THE GENERAL purpose bipolar junction transfer (BJT) op amp has traditionally been designed to have a high-voltage gain differential input stage, a moderately high-voltage gain second stage, and a low-voltage gain/high current gain third stage that acts as a buffer. The first two stages develop the high overall voltage gain needed for the op amp circuit. This configuration has continued in the design of MOS op amps, but as device channel length decreases, high-voltage gain in the first stage is harder to achieve. Although smaller channel lengths lead to higher frequency operation, a high upper corner frequency is unnecessary for the first stage in pole-splitting compensation designs. Consequently, longer channel length devices can be used in the first stage with shorter length devices used in succeeding stages. This work is directed toward longer channel devices although the general results apply to submicron devices also.

The use of longer channel devices for the first stage leads to higher voltage gains because of reduced channel-length modulation effects and higher output resistance. Additionally, longer lengths result in larger widths to achieve appropriate levels of channel inversion. The larger gate areas of the input devices will also reduce the threshold voltage and transconductance mismatch. The lower bandwidth of this stage, using larger devices, leads to a smaller value of compensating capacitor to properly place the dominant pole. The smaller length channel devices that follow create second and third poles that are widely separated from the dominant pole, thereby providing a better phase margin.

If the differential input stage uses wide channel devices, it is easy to bias these devices into the moderate or weak inversion region and achieve several additional advantages [1]–[5]. The first is the higher voltage gain that results from operation below the strong inversion region [1]–[4]. The second advantage is the low device power dissipation resulting from the low value of quiescent drain current. This feature has been used in several early low-power designs [6], [7]. Another advantage is the decrease in distortion over operation in the strong inversion region [4]. It is appropriate to minimize distortion introduced by input stages since succeeding stages will amplify any first stage distortion. Yet another advantage is the higher output resistance of the devices of the input stage resulting from the low drain currents that often lead to operation below the strong inversion region. This further limits the bandwidth and allows the compensating capacitor to have a smaller value. While the low bias current of the first stage decreases the slew rate of the amplifier, the smaller value of compensating capacitor offsets this effect.

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II. Operation of MOS Devices at Different Inversion Levels

MOS devices in amplifier stages typically operate in their active (saturation) regions. However, within the active region a device may be biased to the strong inversion region, the moderate inversion region, or the weak inversion region. In weak inversion, the number of free carriers in the channel is small enough to lead to negligible drift current, but diffusion current flows as the MOSFET operates more like a bipolar junction transistor [1]. The gate-to-source voltage is near the threshold voltage and very small channel current densities exist in this situation. As gate-to-source voltage increases, more carriers are induced in the channel and drift current becomes more significant. In the moderate inversion region, drift and diffusion components are comparable. Strong inversion is reached as the gate-to-source voltage increases to the point that drift current dominates the drain current.

A. Strong Inversion Region

The strong inversion region is perhaps the most commonly used among the three regions. Basic circuit design courses often confine discussion of MOS circuits to operation in this region since analytic equations are readily available. In the strong inversion region, variation of drain current with gate-to-source voltage is given by [8]

$$I_D = \frac{\mu C_{\rm ox}}{2}\frac{W}{L}[V_{\rm GS} - V_T]^2[1 + \lambda(V_{\rm DS} - V_{\rm DSP})] \quad (1)$$

where V_T is the nominal threshold voltage, λ is the channel-length modulation factor, and $V_{\rm DSP}$ is the drain-to-source pinchoff voltage.

B. Weak Inversion Region

Whereas the drain current has a near-square law variation in the strong inversion region, the approximate relation between drain current and gate-to-source voltage in the weak inversion region is given by [1]–[3], [5], and [9]

$$I_D = \frac{W}{L} I_{D0} e^{qV_{\rm GS}/nkT} \tag{2}$$

where n and I_{D0} can be extracted from experimental data. This exponential variation is also valid in the subthreshold region where $V_{\rm GS}$ is slightly less than V_T or $V_{\rm eff} = V_{\rm GS} - V_T < 0$, and a small but detectable drain current flows. The subthreshold region is considered to be included in the weak inversion region. The value of n ranges from approximately 1.6 in weak inversion to 1.3 in strong inversion for an nMOS device [10], [11].

C. Moderate Inversion Region

As $V_{\rm eff}$ increases, more carriers are induced in the channel and drift current becomes more significant. In this region, drift and diffusion currents are comparable. Increased gate-to-source voltage leads to the strong inversion region when drift current dominates the diffusion component.

Although an inversion coefficient can be defined to characterize the level of inversion [12], it can be approximately defined by the gate-to-source voltage. The lower end of the weak inversion region is the subthreshold region that exists for values of $V_{\rm GS}$ less than V_T when positive drain current flows. As $V_{\rm GS}$ ranges from subthreshold values up to about 20 mV above V_T, the device is in the weak inversion region. From a value of 20 mV above V_T to a $V_{\rm GS}$ of approximately 220 mV the device operates in the moderate inversion region [12]. Above this value of $V_{\rm GS}$, drift current dominates and the device is in the strong inversion region.

It is not always apparent in which region a device operates. Consider, an nMOS device with an aspect ratio of $W/L = 100$ and $((\mu C_{\rm ox})/2) = 60\ \mu$A/V^2. The drain current at the lower edge of the strong inversion region, assuming an applied voltage of 220 mV above the threshold voltage, is

$$I_D = 60 \times 100[0.22]^2 = 290\ \mu\text{A}.$$

If a designer sets the drain current for this stage to 100 μA, the device is operating below the strong inversion region. Larger aspect ratios result in even higher currents for weak/moderate inversion operation.

Fig. 1 shows the operation of this device in the various regions as a function of $V_{\rm eff}$. The current is plotted on a log scale and the voltage values of $V_{\rm eff}$ at each side of the moderate inversion region are only approximate. The graph of Fig. 2 shows the *V-I* characteristics for the device. The slope of a given curve in Fig. 2 is much less when the device operates at lower currents than the slope for curves at higher currents. This implies that $r_{\rm ds}$, the drain-to-source resistance, is considerably higher in the weak or moderate inversion region.

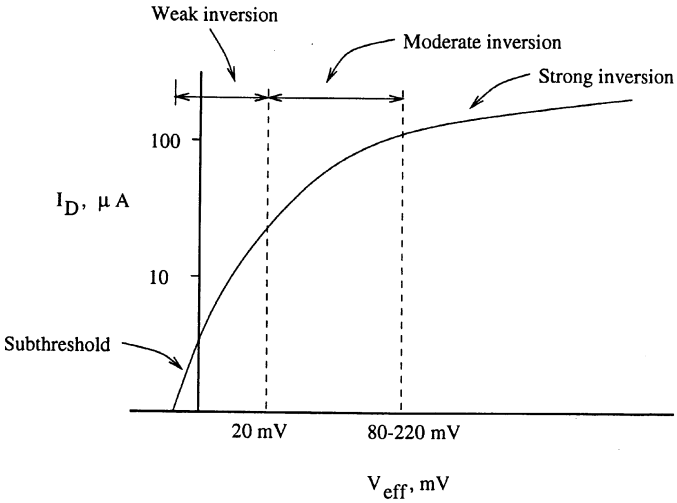

Fig. 1. Drain current as a function of effective voltage.

III. Effect of Operation Below Strong Inversion on Small-Signal Parameters

The channel-length modulation effect is essentially the same in a given device for weak inversion or strong inversion. The variation of $r_{\rm ds}$ with drain current is inverse in both regions, that is,

$$r_{\rm ds} = \frac{1}{\lambda I_{\rm DP}} \tag{3}$$

where $I_{\rm DP}$ is the drain pinchoff current. This pinchoff current is often approximated by I_D. The channel-length modulation factor, λ, equals the reciprocal of the Early voltage and is a strong function of channel length. For a given size device, the drain current decreases as operation moves from strong inversion to weak inversion, thus $r_{\rm ds}$ increases.

The transconductance in the two regions for a given device is quite different. In the strong inversion region, one equation used for this parameter is [8]

$$g_m = \frac{dI_D}{dV_{\rm GS}} = \sqrt{2\mu C_{\rm ox}(W/L)I_D}. \tag{4}$$

In the weak inversion region, the transconductance can be found by differentiating (2) with respect to $V_{\rm GS}$. This results in

$$g_m = \frac{dI_D}{dV_{\rm GS}} = I_{D0}\frac{W}{L}\frac{q}{nkT}e^{qV_{\rm GS}/nkT} = \frac{q}{nkT}I_D. \tag{5}$$

Thus, the transconductance varies directly with drain current in the weak inversion region.

When the simple common-source stage shown in Fig. 3 is driven by an ideal current source, the midband voltage gain is

$$A_{\rm MB} = -g_m r_{\rm ds}. \tag{6}$$

In the strong inversion region, the gain varies with I_D as

$$A_{\rm MB} = \frac{-K_1}{\sqrt{I_D}}. \tag{7}$$

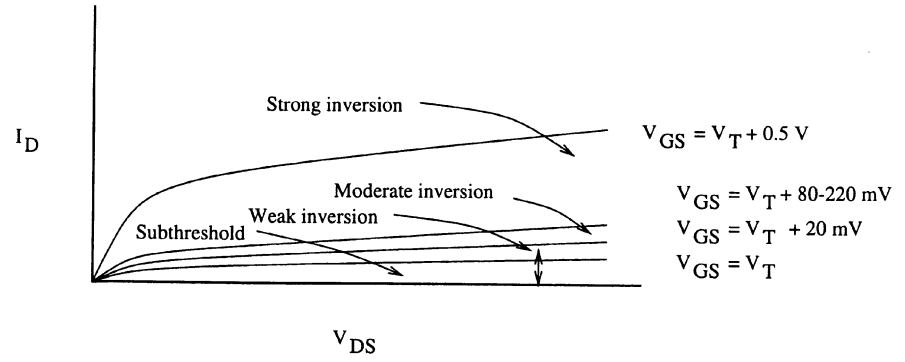

Fig. 2. *V-I* characteristics of an nMOS device.

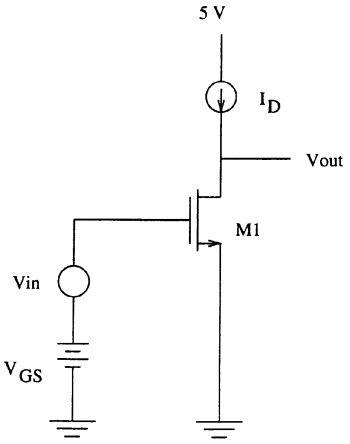

Fig. 3. A common-source stage with an ideal current source load.

In the weak inversion region, however, the voltage gain approaches a constant value or

$$A_{\rm MB} = -K_2. \tag{8}$$

Of course, the device does not move directly from the weak inversion region to the strong inversion region. The moderate inversion region represents a transition from the weak to the strong inversion region and the small-signal parameters vary differently than either of the two preceding equations predict. We can turn to simulation to find the variation of midband gain with drain current in all regions.

Two common-source stages with ideal current source loads are simulated using a BSIM3v3 model. The first has a W/L ratio of 4 μm/2 μm whereas the second stage has W/L = 400 μm/2 μm. The results of these simulations are shown in Figs. 4 and 5 as plots of midband voltage gain versus drain current.

In the strong inversion region, the voltage gain decreases with increasing drain current. Although this falloff approximates the theoretical relationship expressed by (8), the departure from this variation becomes greater as the moderate inversion region is approached from the direction of the strong inversion region. In Figs. 4 and 5, the moderate inversion region is entered near the point that $V_{\rm eff}$ is 200 mV. This region extends down to approximately 20 mV at which point the weak inversion region is entered. The voltage gain peaks near the upper edge of the moderate inversion region. As drain current decreases further, the weak inversion region is entered and the gain approaches a constant value. These plots of voltage gain as a function of drain current have shapes similar to plots of transconductance efficiency

$$\frac{g_m}{I_D}$$

reported in the literature [13]. Since $r_{\rm ds}$ can be related to the Early voltage by

$$r_{\rm ds} = \frac{V_A}{I_D} \tag{9}$$

the midband voltage gain of can also be written as

$$A_{\rm MB} = -\frac{g_m}{I_D} V_A. \tag{10}$$

If V_A is approximately constant for a given channel length, the midband voltage gain is proportionally related to g_m/I_D.

IV. Design Considerations in Amplifier Stages

When designing MOS stages for analog circuits, several considerations influence the choice of channel width, W, and the quiescent drain current, $I_{\rm DQ}$. The required values of upper corner frequency and midband voltage gain strongly influence W, whereas frequency response, midband voltage gain, and power dissipation requirements influence channel length, L, and $I_{\rm DQ}$.

Although operation below the strong inversion region leads to a lower bandwidth, there are several advantages when frequency is not a major consideration. In lower frequency amplifier stages, such as those used in op amps, operation below the strong inversion region leads to three advantages. These are:

1) midband voltage gain is maximum near the lower edge of the strong inversion region;
2) power dissipation is lower as $I_{\rm DQ}$ decreases;
3) distortion of the output signal is reduced when $I_{\rm DQ}$ is set at the point that maximizes voltage gain.

Distortion is reduced as a result of two factors: (1) the gain is more constant over a comparable percentage current swing in this region and (2) the symmetry of gain versus drain current leads to an output signal that approaches half-wave symmetry. This minimizes even harmonic distortion in the output signal.

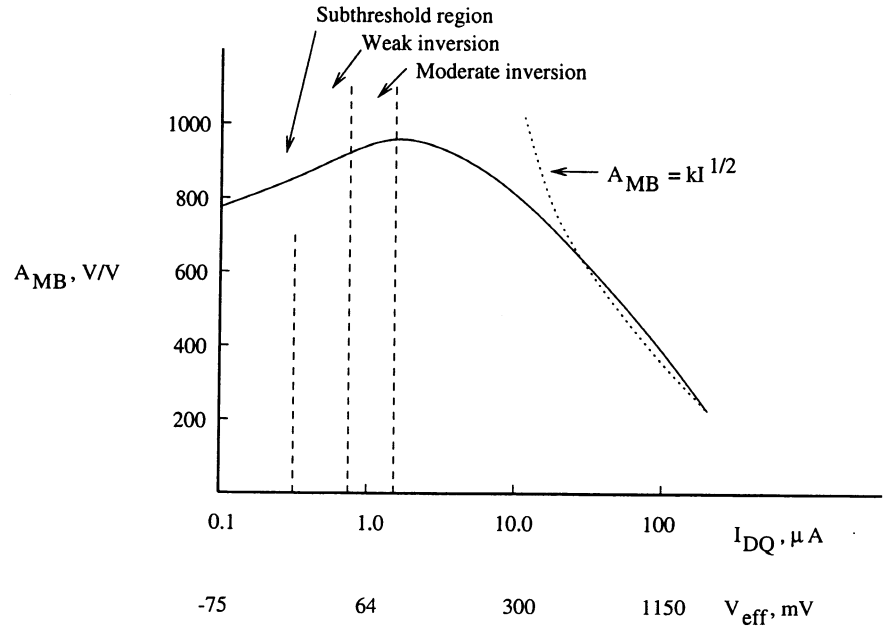

Fig. 4. Voltage gain as a function of drain current for aspect ratio of $4/2$.

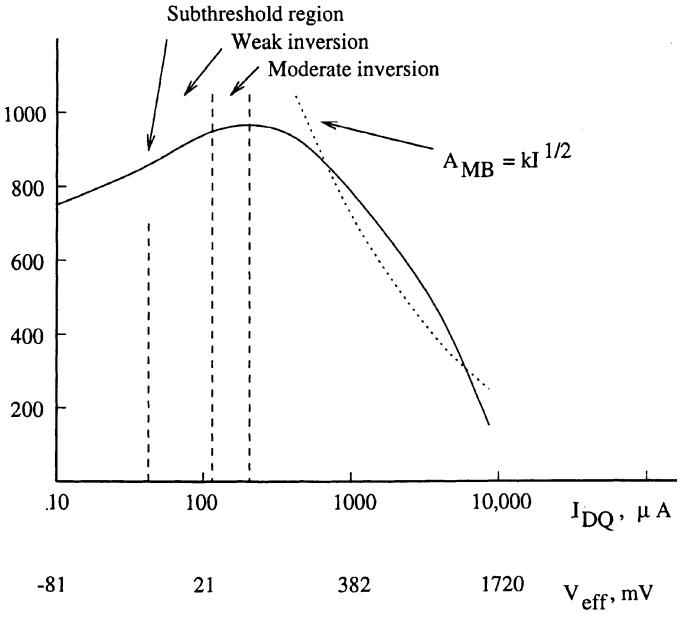

Fig. 5. Voltage gain as a function of drain current for aspect ratio of $400/2$.

In order to demonstrate these advantages, simulations using transient analysis of the common-source stage of Fig. 3 are done for several different situations with a sinusoidal input signal. The stage with $W/L = 4\ \mu\text{m}/2\ \mu\text{m}$ is biased to 2 μA and gain and distortion measurements are taken. From Fig. 4 this bias should result in maximum gain and minimum distortion. The stage is then biased to 100 μA to compare gain and distortion figures for this bias that is well into the strong inversion region. The same measurements are then repeated for the stage with $W/L = 400\ \mu\text{m}/2\ \mu\text{m}$. The maximum voltage gain and minimum distortion bias point in this case is found from Fig. 5 to be near 200 μA. Values at this bias are compared to corresponding values measured in the strong inversion region with $I_{\text{DQ}} = 4$ mA. The results of these measurements are shown in Table I.

TABLE I
SIMULATION RESULTS

W/L μ/μ	I_{DQ} μA	A_{MB} V/V	f_2 kHz	THD %	Even HD %	Output V_{p-p} V	V_p^+/V_p^- V/V
4/2	2	974	361	2.7	0.36	1.99	1.002
4/2	100	403	5950	9.9	9.6	2.00	1.533
400/2	200	961	430	2.7	0.40	1.97	1.004
400/2	4000	460	2370	10.6	10.2	1.81	1.563

A. Voltage Gain

The voltage gain for the stage with $W/L = 4\ \mu\text{m}/2\ \mu\text{m}$ is 974 V/V at the bias point of maximum gain. This occurs for a drain current of 2 μA. When biased into the strong inversion region with a drain current of 100 μA, the gain drops to 403 V/V. The maximum voltage gain is a factor of 2.4 times greater than that when biased well into the strong inversion region.

For the device with $W/L = 400\ \mu\text{m}/2\ \mu\text{m}$, the results are similar. The maximum voltage gain at a bias current of 200 μA is 961 V/V and the gain at a bias current of 4 mA is 460 V/V. The ratio of these gains is 2.1.

B. Harmonic Distortion

The total harmonic distortion (THD) in the strong inversion region for the device with $W/L = 4\ \mu\text{m}/2\ \mu\text{m}$ is 9.9% for a peak-to-peak output voltage of 2.00 V. This compares to a THD of only 2.7% when biased to the point of maximum voltage gain. As expected, the even harmonic distortion almost disappears, dropping from 9.6% in the strong inversion to 0.36% near the moderate inversion region.

A very obvious improvement is that of peak symmetry. For the higher bias current, the output signal, which ideally should exhibit peak symmetry, has a positive peak that is 53% larger than the negative peak. The lower current bias leads to a positive peak that is only 0.2% larger than the negative peak. Fig. 6 shows the output waveforms for the two bias values.

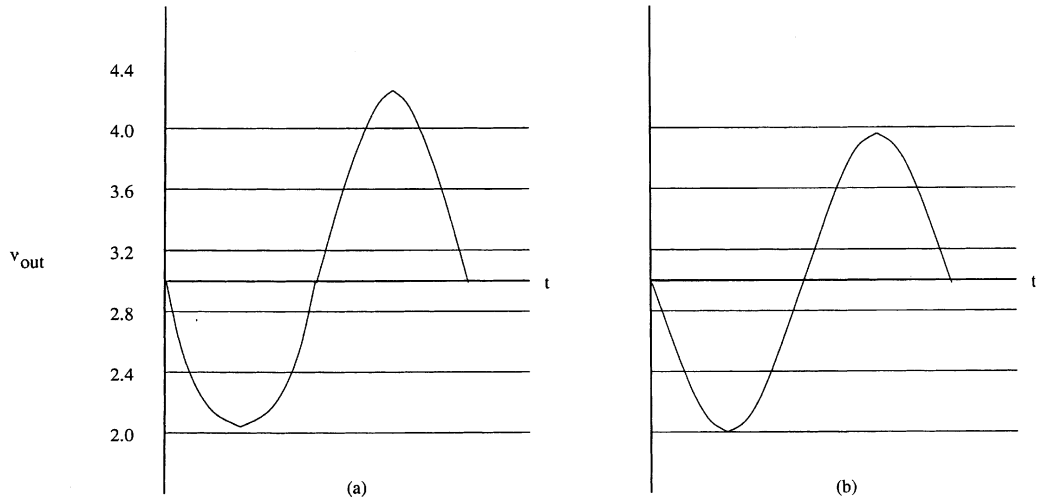

Fig. 6. Asymmetry of waveforms. (a) Strong inversion region. (b) Biased for maximum gain.

Improvements of these same orders of magnitude were also exhibited for the stage with $W/L = 400\ \mu\text{m}/2\ \mu\text{m}$. Distortion improved from 10.6% to 2.7% and the ratio of positive peak to negative peak dropped from 1.563 to 1.004 as bias current was lowered to the point of maximum gain.

Although this distortion comparison is valid to show THD figures for equal outputs when biased in the two regions, it is common to report distortion figures for equal inputs. Since the voltage gain is considerably higher for the lower bias point, the output signal will be larger for the low bias point compared to the strong inversion bias for equal input signals. Thus, THD will also be increased for the low bias point. A 1.5 mV peak signal is used for the input to the device with an aspect ratio of $4/2$. With a drain current of 2 μA (moderate inversion), the simulated THD is 2.8%. Increasing the drain current to 100 μA results in a THD of 7.1%. For the aspect ratio of $400/2$, similar results were obtained. An input of 2 mV peak value led to a THD of 4.6% for moderate inversion bias and 11.3% for strong inversion.

C. Device Dissipation

For all measurements, the value of V_{DSQ} was set near 3 V. The quiescent device dissipation then varies directly with drain current. The dissipation in the smaller device improved by a factor of 50 when biased to the point of maximum gain. The larger device decreased its dissipation by a factor of 20.

V. A Differential Input Stage

Fig. 7 shows a popular input stage used in MOS circuits, consisting of a differential pair with a Wilson current mirror load. The nMOS devices of the differential pair use $W/L = 10\ \mu\text{m}/4\ \mu\text{m}$ while the three pMOS devices use $W/L = 30\ \mu\text{m}/4\ \mu\text{m}$. It can be shown that the voltage gain of this stage is [8]

$$A_{\text{MB}} = g_{m2}R_{\text{out}} \tag{11}$$

where R_{out} is the output resistance presented by devices M2 and M5.

A plot of midband voltage gain as a function of tail current is shown in Fig. 8.

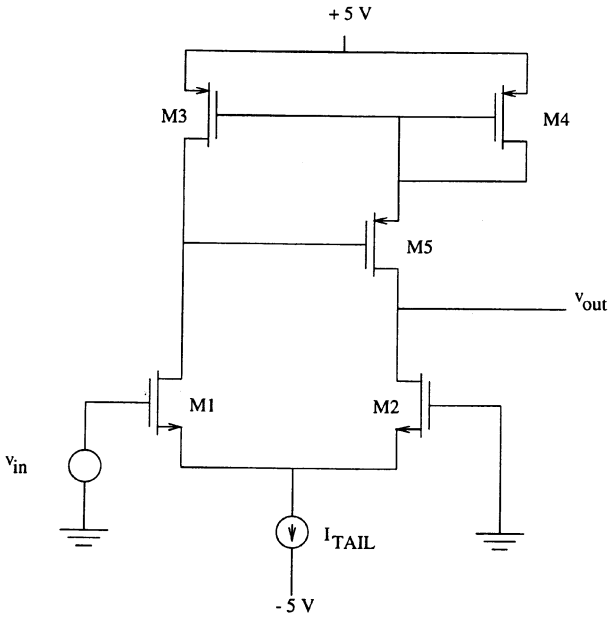

Fig. 7. Differential stage with Wilson current mirror load.

A. Voltage Gain

The voltage gain for the stage is 862 V/V at the bias point of maximum gain. This occurs at a tail current of about 0.5 μA, placing the differential devices near the edge of the weak inversion region. When biased into the strong inversion region with a tail current of 8 μA, the gain drops to 342 V/V. The maximum voltage gain is a factor of 2.5 times greater than that when biased well into the strong inversion region.

B. Harmonic Distortion

The THD in the strong inversion region for the stage is 25.7% for a peak-to-peak output voltage of 1.022 V. This compares to a THD of only 3.3% when biased to the point of maximum voltage gain with a similar peak-to-peak output voltage. As expected, the even harmonic distortion is greatly reduced, dropping from 25.4% in strong inversion to 2.5% at the lower current bias.

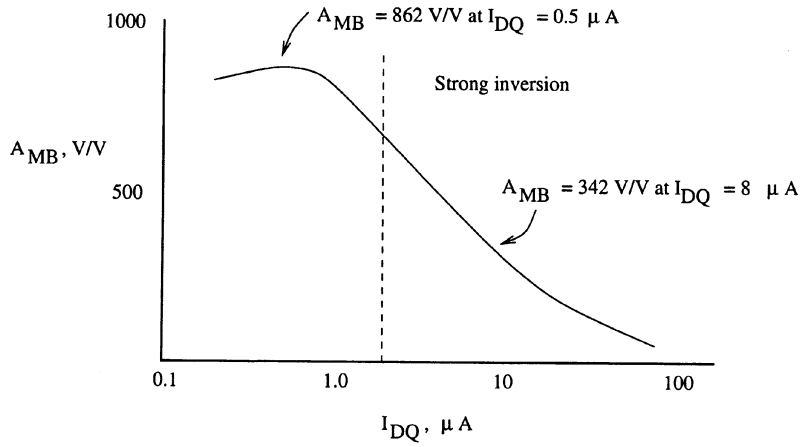

Fig. 8. Voltage gain of differential stage as a function of tail current.

Again, a significant improvement is that of peak symmetry. For the higher bias current, the output signal, which ideally should exhibit peak symmetry, has a positive peak that is a factor of 3.4 times larger than the negative peak. The lower current bias leads to a positive peak that is a factor of only 1.11 times larger than the negative peak.

The distortion is also measured for an input signal of 0.6 mV for the circuit biased with a tail current of 8 μA. The THD in this case is 13.6% compared to 3.3% for the same input signal, but a tail current of 0.5 μA. Again, the circuit biased to weak inversion shows only one-quarter as much THD as the strong inversion bias for equal input signals.

C. Compensating Capacitor

If an op amp is modeled as a three-pole network with P_1 as the first-stage pole, P_2 as the second-stage pole, and P_3 as the third-stage pole, stability in a unity voltage gain feedback configuration requires that [8]

$$P_1 < \frac{P_2 + P_3}{A_{\rm MB}} \tag{12}$$

This condition is generally achieved by adding a capacitor that bridges input and output nodes of the second stage, using the Miller effect to multiply the capacitive load on the first stage. The Miller effect is used to allow the actual capacitor value to be sufficiently small for IC realization. A typical value of voltage gain of the second stage is -300 V/V resulting in a capacitor multiplication factor of 301. The actual capacitor value may be around 20 pF for a general purpose op amp.

Addition of this capacitor also determines the slew rate of the circuit. This parameter is given by [8]

$$\text{Slew rate} = \frac{dv_{\rm out}}{dt}(\max) = \frac{I_{\rm TAIL}}{C} \tag{13}$$

where C is the actual value of the compensating capacitor and $I_{\rm TAIL}$ is the tail current of the differential stage.

For the differential stage of Fig. 7, it is obvious that operation at the point of maximum gain leads to a smaller value of P_1 from (12). Since the voltage gain for $I_{\rm TAIL} = 0.5\ \mu$A is a factor of 2.5 times higher that that for $I_{\rm TAIL} = 8\ \mu$A, the required value of P_1 for stable operation is a factor of 2.5 times lower. If the output resistance of the differential stage, $R_{\rm out}$, remained constant for both bias points, a larger capacitor would be required to stabilize the circuit when biased to the lower current. However, the output resistance for the lower tail current increases dramatically over the higher current case. The required capacitance is then much smaller for the low tail current case than for the high tail current case.

In order to demonstrate this effect, the upper corner frequency of the differential stage of Fig. 7 was dropped to 100 Hz by adding a capacitor from the output node to ground. With a tail current of 0.5 μA, the required capacitance was found by simulation to be 7.6 pF. For a tail current of 8 μA, the value of capacitance was found to be 168 pF. If these capacitors were created by the Miller effect of a second stage with a gain of -300 V/V, the two actual values of capacitance would be 25 fF and 558 fF for tail currents of 0.5 μA and 8 μA, respectively. Due to the higher gain of the low-current stage, the upper corner frequency may need to be a factor of 2.5 times lower than that for the high-current case. This would lead to a capacitor that is 2.5 times greater than the 25 fF value calculated or 62.5 fF.

Although the compensating capacitance is much smaller for the low-current case, the slew rate is not correspondingly improved. In fact, it may show a slight decrease. From (12), the slew rate for the low tail current circuit is

$$\frac{dv_{\rm out}}{dt}(\max) = \frac{5 \times 10^{-7}}{62.5 \times 10^{-15}} = 8 \times 10^6\ \text{V/s}$$

This compares to a slew rate for the case of high tail current of

$$\frac{dv_{\rm out}}{dt}(\max) = \frac{8 \times 10^{-6}}{558 \times 10^{-15}} = 14.3 \times 10^6\ \text{V/s}$$

While it is beyond the scope of this paper, work has been done on current matching and offset voltage matching for weak inversion biasing [14]. Weak inversion bias tends to minimize voltage differences or offsets, but is poorer for current mirror matching compared to strong inversion bias.

VI. Conclusion

Operation of amplifier stages in the weak or moderate inversion region leads to several advantages for high-gain/low-frequency stages such as input stages for an op amp. Higher gain, less dissipation, less distortion, and a smaller value of compensating capacitance are four advantages derived from biasing below the strong inversion region rather than in this region. The slew rate may decrease slightly for operation in the weak/moderate inversion region.

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