Editorial

THIS issue marks the completion of four years of this TRANSACTIONS. This TRANSACTIONS has reached several milestones in its short lifespan. It is now an established avenue for interdisciplinary publication in the many areas of nanotechnology of IEEE's mainstream. A journal is at its best when it provides outstanding, well-reasoned, novel and carefully written papers that foster creative insights and new directions for technical exploration. This TRANSACTIONS has been successful in its goals, is amongst the top ten IEEE publications for impact, has a growing circulation, and is now published six times a year. Our appeal to the community is also reinforced by the standards that the journal has maintained while providing rapid publication through the use of electronic submission and processing.

In this era of proliferation of publications, particularly by profit-making organizations, professional societies and their technically focused journals are a critical element in a profession maintaining its independence and integrity. The success of a publication such as this TRANSACTIONS is only possible because of the volunteers who edit and review the publications. Rapid dissemination of scientific and technical information would not be possible without this selfless service, and this publication is enormously indebted to both the reviewers and the editors.

Four years is also a significant stretch of time, and changes help bring new ideas and new enthusiasm. Prof. Akira Toriumi, Prof. Wolfgang Porod, and Prof. Sakhrat Khizroev are relinquishing their responsibilities. We owe them enormous gratitude for countless hours of work. Prof. Toshio Hiramoto is joining as an Associate Editor. His areas of interest span materials, devices, and circuits at nanoscale.

Four years is also a sufficiently long time period for an Editor-in-Chief. I thank the IEEE for giving me this enormous opportunity to serve the profession and to explore and develop a responsible interdisciplinary publication. This task has been a source of satisfaction. It is my pleasure to welcome Prof. Philip Wong as the new Editor-in-Chief of this TRANSACTIONS. I wish him and this publication continuing success.

SANDIP TIWARI, *Former Editor-in-Chief*
School of Electrical and Computer Engineering
Cornell University
Ithaca, NY 14853 USA

Digital Object Identifier 10.1109/TNANO.2005.861407

Toshiro Hiramoto (M'93) received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1984, 1986, and 1989, respectively.

In 1989, he joined the Device Development Center, Hitachi Ltd., Ome, Japan, where he was engaged in the device and circuit design of ultrafast BiCMOS SRAMs. In 1994, he joined the Institute of Industrial Science, University of Tokyo, as an Associate Professor. From 1996 to 2002, he was also an Associate Professor with the Very Large Scale Integration (VLSI) Design and Education Center, University of Tokyo. Since 2002, he has been a Professor with the Institute of Industrial Science, University of Tokyo. His research interests include low-power and low-voltage design of advanced CMOS devices, silicon-on-insulator (SOI) MOSFETs, device/circuit cooperation scheme for low-power VLSI, quantum effects in nanoscale MOSFETs, and silicon single-electron transistors.

Dr. Hiramoto is a member of the Institute of Electrical, Information and Communication Engineers (IEICE), Japan, and the Japan Society of Applied Physics. He has been an Elected Administrative Committee (AdCom) member of the IEEE Electron Devices Society since 2001. He served as the general chair of the Silicon Nanoelectronics Workshop in 2003 and as the program chair in 1997, 1999, and 2001. He also served on the Program Subcommittee on Integrated Circuits of the IEEE International Electron Devices Meeting (IEDM) in 1993 and 1994 and on the Program Subcommittee on CMOS Devices of the IEDM in 2003 and has served on the Program Committee of the Symposium on VLSI Technology since 2001.

H.-S. Philip Wong (S'81–M'82–SM'95–F'01) received the B.Sc. (Hons.) degree from the University of Hong Kong, Hong Kong, in 1982, the M.S. degree from the State University of New York at Stony Brook, in 1983, and the Ph.D. degree from Lehigh University, Bethlehem, PA, in 1988, all in electrical engineering.

In 1988, he joined the IBM T. J. Watson Research Center, Yorktown Heights, NY. In September 2004, he joined Stanford University, Stanford, CA, as a Professor of electrical engineering. While with IBM, he was involved with CCD and CMOS image sensors, double-gate/multigate MOSFETs, device simulations for advanced/novel MOSFETs, strained silicon, wafer bonding, ultrathin body SOI, extremely short-gate field-effect transistors (FETs), germanium MOSFETs, carbon-nanotube FETs, and phase change memory. He has held various positions from Research Staff Member to Manager to Senior Manager. While he was a Senior Manager, he had the responsibility of shaping and executing IBM's strategy on nanoscale science and technology, as well as exploratory silicon devices and semiconductor technology. His research interests are in nanoscale science and technology, semiconductor technology, solid-state devices, and electronic imaging. He is interested in exploring new materials, novel fabrication techniques, and novel device concepts for future nanoelectronics systems. Novel devices often require new concepts in circuit and system designs. His research also includes explorations into circuits and systems that are device driven. His current research covers a broad range of topics including carbon nanotubes, semiconductor nanowires, self-assembly, exploratory logic devices, and novel memory devices.

Prof. Wong serves the IEEE Electron Devices Society (EDS) as an elected Administrative Committee (AdCom) member. He serves on the International Electron Devices Meeting (IEDM) committee (1998–2006), was the Technical Program vice-chair in 2005, and will be the Technical Program chair in 2006. From 1998 to 2004, he served on the International Solid-State Circuits Conference (ISSCC) Program Committee. From 2003 to 2004, he was the chair of the Image Sensors, Displays, and Microelectromechanical Systems (MEMS) Subcommittee. He is a Distinguished Lecturer of the IEEE EDS. He has taught several short courses at the IEDM, ISSCC, Symposium on VLSI Technology, SOI, ESSDERC, and SPIE conferences. He is a member of the Emerging Research Devices Working Group of the International Technology Roadmap for Semiconductors (ITRS).