

Proceedings  
International Test Conference  
2001

---

---

The papers in this publication comprise the proceedings of International Test Conference 2001. They reflect the authors' opinions and are reproduced as presented and without change. Their inclusion in this publication does not necessarily constitute endorsement by International Test Conference, the sponsors, or the Institute of Electrical and Electronic Engineers, Inc.

Published by

**International Test Conference**  
**2000 L Street, N.W., Suite 710**  
**Washington, D.C. 20036**  
**(202) 973-8665**  
**E-mail: [itc@courtesyassoc.com](mailto:itc@courtesyassoc.com)**  
**<http://www.itctestweek.org>**

Copyright© 2001 by the Institute of Electrical and Electronic Engineers, Inc.

Printed in United States of America.

**Copyright and Reprint Permissions:** Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923. For other copying, reprint or republication permission, write to **IEEE Copyrights Manager, IEEE Operations Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331**. All rights reserved.

IEEE Catalog Number 01CH37260  
ISBN 0-7803-7169-0  
ISBN 0-7803-7170-4 (Microfiche Edition)  
ISSN 1089-3539

Order additional copies from:

IEEE Service Center  
445 Hoes Lane, P.O. Box 1331  
Piscataway, NJ 08855-1331

IEEE Computer Society Press  
Customer Service Center  
10662 Los Vaqueros Circle  
P.O. Box 3014  
Los Alamitos, CA 90720-1264

# Table of Contents

<b>INTRODUCTORY SECTION</b>	
Welcoming Message .....	1
Steering Committee and Subcommittees .....	2
Technical Program Committee .....	4
ITC Technical Paper Evaluation and Selection Process .....	8
2000 Paper Awards .....	9
2002 Call for Papers .....	11
TTTC: Test Technology Technical Council .....	14
Technical Paper Reviewers .....	17
Author Index .....	1200
<b>SPECIAL PANEL: CHANGING ECONOMICS OF SOC TESTING: WHO OWNS THE MARKET?</b>	
Moderator and Organizer: B. Kaminska .....	23
<i>SP1.1 Adding Value to SOC Testing While Lowering Costs</i>	
R. Blethen .....	24
<i>SP1.2 Changing Economics of SOC Testing: Who Owns the Market?</i>	
J. Harris .....	25
<i>SP1.3 SOC Test Challenges for the New Millennium</i>	
T. Newsom .....	26
<i>SP1.4 Bridging the Gap</i>	
L. Watrous-deVersterre .....	27
<b>SPECIAL PANEL: STRUCTURED TEST: THEN AND NOW</b>	
Moderator and Organizer: R. Aitken .....	28
<i>SP2.1 Structured Test, Then and Now</i>	
E. Eichelberger, N. Shahriari .....	29
<b>SESSION 1: PLENARY</b>	
ITC General Chair: William Lowd	
<b>Keynote Address</b>	
<i>Test Trade-offs: The View from Wall Street</i>	
S. Billat .....	12
<b>Invited Address</b>	
<i>Today's Test Choices: Anticipate, Adapt, Partner or Perish</i>	
P. Nigh .....	13
<b>SESSION 2: IEE 1149—BEYOND DC TESTING AT BOARD TEST</b>	
Session Chair: J. Webster, Coordinator: B. Sutton	
<i>2.1 AC-JTAG: Empowering JTAG beyond Testing DC Nets</i>	
S. Chung*, S. Baeg .....	30
<i>2.2 A General Purpose 1149.4 IC with HF Analog Test Capabilities</i>	
S. Sunter*, K. Filliter, J. Woo, P. McHugh .....	38
<i>2.3 Frequency Detection-based Boundary-Scan Testing of AC Coupled Nets</i>	
Y. Kim, B. Lai, K. Parker*, J. Rearick .....	46

**ITC Office**  
 2000 L Street, N.W.  
 Suite 710  
 Washington, D.C. 20036 USA  
 Tel: (202) 973-8665

**SESSION 3: BIST MEDLEY**

Session Chair: X. Sun, Coordinator: B. Nadeau-Dostie

- 3.1 *Design of Compactors for Signature-Analyzers in Built-In Self-Test*  
P. Wohl\*, J. Waicukauski, T.W. Williams ..... 54
- 3.2 *At-Speed Logic BIST Using a Frozen Clock Testing Strategy*  
J. Shin, X. Yu, E. Rudnick\*, M. Abramovici ..... 64
- 3.3 *Tackling Test Trade-offs for BIST RTL Data Paths: BIST  
Area Overhead, Test Application Time and Power Dissipation*  
N. Nicolici\*, B. Al-Hashimi ..... 72

**SESSION 4: HOW CAN WE IMPROVE  $I_{DDQ}$  TESTING FOR DSM/VDSM?**

Session Chair: P. Maxwell, Coordinator: C. Metra

- 4.1 *Improved Wafer-level Spatial Analysis for  $I_{DDQ}$  Limit Setting*  
S. Sabade\*, D. Walker ..... 82
- 4.2 *Neighbor Selection for Variance Reduction in  $I_{DDQ}$  and Other  
Parametric Data*  
W. Daasch\*, K. Cota, J. McNames, R. Madge ..... 92
- 4.3 *The Future of Delta  $I_{DDQ}$  Testing*  
B. Kruseman\*, R. van Veen, K. van Kaam ..... 101

**SESSION 5: PRACTICAL EXPERIENCE WITH SOC TESTING**

Session Chair: Y. Zorian, Coordinator: N. Touba

- 5.1 *A Building Block BIST Methodology for SOC Designs:  
A Case Study*  
V. Chickermane, P. Gallagher\*, S. Gregor, T. St. Pierre ..... 111
- 5.2 *Test and Debug Strategy of the PNX8525 Nexperia™  
Digital Video Platform System Chip*  
B. Vermeulen\*, S. Oostdijk, F. Bouwman ..... 121
- 5.3 *CTL the Language for Describing Core-based Test*  
R. Kapur\*, M. Lousberg, T. Taylor, B. Keller,  
P. Reuter, D. Kay ..... 131

**SESSION 6: SOME THORNY PROBLEMS FOR ATE SOFTWARE**

Session Chair: R. Huston, Coordinator: A. Downey

- 6.1 *Split Timing Mode (STM) – Answer To Dual-Frequency-  
Domain Testing*  
A. Sivaram ..... 140
- 6.2 *Automated Translation of Legacy Code for ATE*  
A. Moran\*, J. Teisher, A. Gill, E. Pasalic, J. Veneruso ..... 148
- 6.3 *Remote Access To Engineering Test – A Case Study In  
Providing Engineering/Diagnostic IC Test Services to  
Canadian Universities*  
R. Stevenson\*, M. Jarosz, C. Verver ..... 157

**SESSION 7: LECTURE SERIES—TEST AND REPAIR OF LARGE  
EMBEDDED DRAMS**

Session Chair: G. Fleeman, Coordinator: R. Rajsuman

- 7.1 *Test and Repair of Large Embedded DRAMs: Part 1*  
R. McConnell\*, R. Rajsuman, E. Nelson, J. Dreibelbis ..... 163
- 7.2 *Test and Repair of Large Embedded DRAMs: Part 2*  
E. Nelson\*, J. Dreibelbis, R. McConnell ..... 177

# Table of Contents

7.3	<i>Test Cost Reduction by At-Speed BISR for Embedded DRAMs</i> Y. Nagura*, M. Mullins, A. Sauvageau, Y. Fujiwara, K. Furue, R. Ohmura, T. Komoike, T. Okitaka, T. Tanizaki, K. Dosaka, K. Arimito, Y. Koda, T. Tada, .....	182
<b>SESSION 8: DFT INNOVATIONS</b>		
Session Chair: M. Flottes, Coordinator: C. Landrault		
8.1	<i>DPDAT: Data Path Direct Access Testing</i> K. Kim*, R. Jayabharathi, C. Carstens, P. Vishakantaiah, D. Feltham, A. Carbine .....	188
8.2	<i>A Method to Enhance the Fault Coverage Obtained by Output Response Comparison of Identical Circuits</i> I. Pomeranz*, S. Reddy .....	196
8.3	<i>Contactless Digital Testing of IC Pin Leakage Currents</i> S. Sunter*, C. McDonald, G. Danialy .....	204
8.4	<i>On Improving the Stuck-at-Fault Coverage of Functional Test Sequences by Using Limited-Scan Operations</i> I. Pomeranz, S. Reddy* .....	211
<b>SESSION 9: ON-LINE TEST</b>		
Session Chair: L. Bouzaida, Coordinator: M. Nicolaidis		
9.1	<i>Algorithm-level Re-Computing with Allocation Diversity: A Register Transfer Level Concurrent Error Detection Technique</i> K. Wu*, R. Karri .....	221
9.2	<i>A Highly Efficient Transparent Online Memory Test</i> K. Thaller .....	230
9.3	<i>On-line Testing and Recovery in TMR Systems for Real-Time Applications</i> S.-Y. Yu*, E. McCluskey .....	240
9.4	<i>GRAAL: A Tool for Highly Dependable SRAMs Generation</i> S. Chiusano*, G. DiNatale, P. Prinetto, F. Bigongiari .....	250
<b>SESSION 10: NOVEL TECHNIQUES FOR FAULT DIAGNOSIS</b>		
Session Chair: D. Feltham, Coordinator: A. Gattiker		
10.1	<i>Test Response Compression and Bitmap Encoding for Embedded Memories in Manufacturing Process Monitoring</i> J. Chen*, J. Khare, K. Walker, S. Shaikh, J. Rajski, W. Maly ...	258
10.2	<i>A Technique for Fault Diagnosis of Defects in Scan Chains</i> R. Guo*, S. Venkataraman .....	268
10.3	<i>Making Cause-Effect Cost Effective: Low-Resolution Fault Dictionaries</i> D. Lavo*, T. Larrabee .....	278
10.4	<i>Diagnosing Combinational Logic Designs Using the Single Location At-a-Time (SLAT) Paradigm</i> T. Bartenstein, D. Heaberlin, L. Huisman*, D. Sliwinski .....	287
<b>SESSION 11: TESTING ABOVE A GIGAHERTZ</b>		
Session Chair: M. Barber, Coordinator: D. Keezer		
11.1	<i>Testing Gigabit Multilane SerDes Interfaces with Passive Jitter Injection Filters</i> B. Laquai, Y. Cai* .....	297

11.2	<i>Testing Interconnects for Noise and Skew in Gigahertz SOCs</i> A. Attarha*, M. Nourani .....	305
11.3	<i>A Built-in Timing Parametric Measurement Unit</i> M.-J. Hsiao, J.-R. Huang, S.-J. Yang, T.-Y. Chang* .....	315
11.4	<i>Testing Clock Distribution Circuits Using an Analytic Signal Method</i> T. Yamaguchi*, M. Soma, J. Nissen, D. Halter, R. Raina, M. Ishida .....	323

**SESSION 12: TEST METHODS FOR HIGH-DENSITY MODULES**

Session Chair: B. Kim, Coordinator: D. Keezer

12.1	<i>Rapid Prototyping of Time-based PDIT for Substrate Networks</i> A. Venkataratnam, K. Newman* .....	332
12.2	<i>Estimating Burn-In Fail-out for Redundant Memory</i> T. Barnett*, A. Singh, V. Nelson .....	340
12.3	<i>Extreme-Voltage Stress Vector Generation of Analog CMOS ICs for Gate-Oxide Reliability Enhancement</i> M. Khalil, C.-L. Wey* .....	348

**SESSION 13: HIGH-QUALITY TEST**

Session Chair: W. Cheng, Coordinator: K. Panetta

13.1	<i>Multiple-Output Propagation Transition Fault Test</i> C.-W. Tseng*, E. McCluskey .....	358
13.2	<i>Switch-level Delay Test of Domino Logic Circuits</i> S. Natarajan*, S. Gupta, M. Breuer .....	367
13.3	<i>Implicit Functionality and Multiple Branch Coverage (IFMB): A Testability Metric for RT-Level</i> M. Santos*, F. Goncalves, I. Teixeira, J. Teixeira .....	377

**SESSION 14: NEW IDDX AND ENERGY TEST TECHNIQUES**

Session Chair: J. Segura, Coordinator: J. Soden

14.1	<i>Practical Application of Energy Consumption Ratio Test</i> E. Peterson*, W. Jiang .....	386
14.2	<i>Detecting Delay Faults Using Power Supply Transient Signal Analysis</i> A. Singh*, C. Patel, S. Liao, J. Plusquellic, A. Gattiker .....	395
14.3	<i>A Practical Built-in Current Sensor for <math>I_{DDQ}</math> Testing</i> H. Kim, D. Walker*, D. Colby .....	405

**SESSION 15: ATE HARDWARE: IMPROVING YOUR TEST RESULTS**

Session Chair: L. Song, Coordinator: B. Brown

15.1	<i>Test Path Simulation and Characterisation</i> K. Helmreich .....	415
15.2	<i>Testing Beyond EPA: TDF Methodology Solutions Matrix</i> S. Jain*, G. Chema .....	424
15.3	<i>Practical, Non-invasive Optical Probing for Flip-Chip Devices</i> G. Dajee*, N. Goldblatt, T. Lundquist, S. Kasapi, K. Wilsher .....	433

# Table of Contents

## SESSION 16: ADVANCED MICROPROCESSOR TEST METHODOLOGIES

Session Chair: C. Pyron, Coordinator: S. Fetherston

- 16.1 *Scan vs. Functional Testing – A Comparative Effectiveness Study on Motorola's MMC2107™*  
K. Tumin\*, C. Vargas, R. Patterson, C. Nappi ..... 443
- 16.2 *Debug Methodology for the McKinley Processor*  
D. Josephson\*, S. Poehlman, V. Govan ..... 451
- 16.3 *Using a Hierarchical DFT Methodology in High-Frequency Processor Designs for Improved Delay Fault Testability*  
M. Kessler, G. Kiefer, J. Leenstra, K. Schunemann,  
T. Schwarz\*, H. Wunderlich ..... 461

## SESSION 17: LECTURE SERIES—SOLVING BOARD TEST AND IN-SYSTEM PROBLEMS

Session Chair: J. Webster, Coordinator: B. Sutton

- 17.1 *Testing and Programming Flash Memories on Assemblies During High-Volume Production*  
F. deJong\*, A. Biewenga, D. van Geest, T. Waayers ..... 470
- 17.2 *Hierarchical Boundary-Scan: A Scan Chip-Set Solution*  
S. Harrison, G. Noeninckx, P. Horwood, P. Collins\* ..... 480
- 17.3 *A Practical Guide to Combining ICT and Boundary-Scan Testing*  
A. Albee ..... 487

## SESSION 18: MIXED-SIGNAL TESTING TECHNIQUES

Session Chair: B. Kaminska, Coordinator: S. Sunter

- 18.1 *Ramp Testing of ADC Transition Levels Using Finite Resolution Ramps*  
S. Max ..... 495
- 18.2 *Test Challenges for SONET/SDH Physical Layer OC3 Devices and Beyond*  
U. Natarajan ..... 502
- 18.3 *A Method to Improve SFDR with Random Interleaved Sampling Method*  
M. Tamba\*, A. Shimizu, H. Munakata, T. Komuro ..... 512

## SESSION 19: ADVANCED TECHNIQUES FOR EMBEDDED CORE TESTING

Session Chair: B. Pouya, Coordinator: N. Touba

- 19.1 *Space and Time Compaction Schemes for Embedded Cores*  
O. Sinanoglu\*, A. Orailoglu ..... 521
- 19.2 *Tailoring ATPG for Embedded Testing*  
R. Dorsch\*, H.-J. Wunderlich ..... 530
- 19.3 *A Case Study on the Implementation of the Illinois Scan Architecture*  
F. Hsu\*, K. Butler, J. Patel ..... 538

## SESSION 20: TEST GENERATION FOR CROSSTALK FAULTS

Session Chair: A. Majumdar, Coordinator: S. Davidson

- 20.1 *Crosstalk Test Generation on Pseudo Industrial Circuits: A Case Study*  
L.-C. Chen\*, T. Mak, M. Breuer, S. Gupta ..... 548

20.2	<i>Delay Testing Considering Crosstalk-induced Effects</i> A. Krstic*, J.-J. Liou, Y.-M. Jiang, K.-T. Cheng .....	558
20.3	<i>On Reducing the Target Fault List of Crosstalk-induced Delay Faults in Synchronous Sequential Circuits</i> K. Keller, H. Takahashi*, K. Saluja, Y. Takamatsu .....	568
<b>SESSION 21: MICROPROCESSOR TESTING</b>		
Session Chair: M. Abadir, Coordinator: C. Pyron		
21.1	<i>Test Methodology for the McKinley Processor</i> D. Josephson, S. Poehlman*, V. Govan, C. Mumford .....	578
21.2	<i>99 % AC Test Coverage Using Only LBIST on the 1-GHz IBM S/390 zSeries 900 Microprocessor</i> M. Kusko*, B. Robbins, T. Koprowski, W. Huott .....	586
21.3	<i>Modeling and Testing the Gekko Microprocessor, An IBM PowerPC Derivative for Nintendo</i> G. Vandling .....	593
<b>SESSION 22: STANDARDS AND TECHNIQUES—BOARD TEST DEVELOPMENT</b>		
Session Chair: J. Webster, Coordinator: B. Sutton		
22.1	<i>Towards a Unified Test Process: From UML to End-of-Line Functional Test</i> A. Baldini, A. Benso, P. Prinetto*, S. Mo, A. Taddei .....	600
22.2	<i>Dynamic Tests in Complex Systems</i> R. Tappe*, D. Ehrhardt .....	609
22.3	<i>Unsafe Board States During PC-based Boundary-Scan Testing</i> B. Eklow, R. Sedmak*, D. Singletary, T. Vo .....	615
<b>SESSION 23: DELAY TEST</b>		
Session Chair: J. Tyszer, Coordinator: J. Rajski		
23.1	<i>Too Much Delay-Fault Coverage Is a Bad Thing</i> J. Rearick .....	624
23.2	<i>Testing of Critical Paths for Delay Faults</i> M. Sharma*, J. Patel .....	634
23.3	<i>Exact Path-Delay Grading with Fundamental BDD Operations</i> S. Padmanaban, M. Michael*, S. Tragoudas .....	642
<b>SESSION 24: IDEAS FOR LOW-POWER SCAN OPERATION</b>		
Session Chair: B. Stewart, Coordinator: A. Meixner		
24.1	<i>Scan Array Solution for Testing Power and Testing Time</i> L. Xu*, Y. Sun, H. Chen .....	652
24.2	<i>A Token Scan Architecture for Low-Power Testing</i> T.-C. Huang*, K.-J. Lee .....	660
24.3	<i>An Analysis of Power Reduction Techniques in Scan Testing</i> J. Saxena*, K. Butler, L. Whetsel .....	670
<b>SESSION 25: UNCOVERING AND UNDERSTANDING WHY CIRCUITS FAIL</b>		
Session Chair: I. Hartanto, Coordinator: A. Gattiker		
25.1	<i>On Efficient Error Diagnosis of Digital Circuits</i> N. Sridhar, M. Hsiao* .....	67



# Table of Contents

25.2	<i>A Study of Bridging Defect Probabilities on a Pentium™ 4 CPU</i> V. Krishnaswamy*, A. Ma, P. Vishakantaiah .....	688
25.3	<i>Fed Ex™ – A Fast Bridging Fault Extractor</i> Z. Stanojevic*, D. Walker .....	696
<b>SESSION 26: ATE HW: CONQUERING THOSE STUBBORN TEST PROBLEMS</b>		
Session Chair: S. Cohen, Coordinator: B. Brown		
26.1	<i>Power Supply Transient Signal Integration Circuit</i> C. Patel*, F. Muradali, J. Plusquellic .....	704
26.2	<i>Scan Test Sequencing for Structural Test</i> J. Cullen .....	713
<b>SESSION 27: ADVANCES IN SCAN TESTING</b>		
Session Chair: S. Menon, Coordinator: R. Raina		
27.1	<i>Tester Retargetable Patterns</i> R. Kapur, T.W. Williams* .....	721
27.2	<i>On RTL Scan Design</i> Y. Huang*, C.-C. Tsai, N. Mukherjee, O. Samman, D. Devries, W.-T. Cheng, S. Reddy .....	728
27.3	<i>Enhanced Reduced Pin-Count Test for Full-Scan Design</i> H. Vranken, T. Waayers*, H. Fleury, D. Lelouvier .....	738
27.4	<i>OPMISR: The Foundation for Compressed ATPG Vectors</i> B. Keller*, C. Barnhart, V. Brunkhorst, F. Distler, A. Ferko, O. Farnsworth, B. Koenemann .....	748
<b>SESSION 28: MEMORY TESTING</b>		
Session Chair: N. Otsuka, Coordinator: R. Rajsuman		
28.1	<i>March-based RAM Diagnosis Algorithms for Stuck-at and Coupling Faults</i> J.-T. Li*, K.-L. Cheng, C.-T. Huang, C.-W. Wu .....	758
28.2	<i>Pseudo Fail Bit Map Generation for RAMs during Component Test and Burn-in in a Manufacturing Environment</i> J. Vollrath*, R. Rooney .....	768
28.3	<i>Bitline Contacts in High Density SRAMS: Design for Testability and Stressability</i> H. Pilo*, R. Adams, R. Busch, E. Nelson, G. Rudgers .....	776
28.4	<i>Simulation-based Analysis of Temperature Effect on the Faulty Behavior of Embedded DRAMs</i> Z. Al-Ars, A. van de Goor*, J. Braun, D. Richter .....	783
<b>SESSION 29: INCREASING DESIGN VALIDATION COVERAGE</b>		
Session Chair: S. Dey, Coordinator: P. Varma		
29.1	<i>Cost Evaluation of Coverage-directed Test Generation for the IBM Mainframe</i> G. Nativ, S. Mittermaier*, S. Ur, A. Ziv .....	793
29.2	<i>Identifying Redundant Gate Replacements in Verification by Error Modeling</i> K. Radecka, Z. Zilic* .....	803

\* = presenter

29.3	<i>A Validation Fault Model for Timing-induced Functional Errors</i> Q. Zhang*, I. Harris .....	813
29.4	<i>AMLETO: A Multi-Language Environment for Functional Test Generation</i> A. Fin, F. Fummi*, G. Pravadelli .....	821

**SESSION 30: PLL AND JITTER TESTING**

Session Chair: S. Kumar, Coordinator: G. Roberts

30.1	<i>Test Evaluation and Data on Defect-oriented BIST Architecture for High-Speed PLL</i> S. Kim*, M. Soma .....	830
30.2	<i>A High-Resolution Jitter Measurement Technique Using ADC Sampling</i> S. Cherubal*, A. Chatterjee .....	838
30.3	<i>An Approach to Consistent Jitter Modeling for Various Jitter Aspects and Measurement Methods</i> M. Shimanouchi .....	848
30.4	<i>A Synthesizeable, Fast and High-Resolution Timing Measurement Device using a Component-invariant Vernier Delay Line</i> A. Chan*, G. Roberts .....	858

**SESSION 31: NEW IDEAS FOR BIST TPG**

Session Chair: A. Crouch, Coordinator: K. Hatayama

31.1	<i>Low-Hardware-Overhead Scan-based 3-Weight Weighted Random BIST</i> S. Wang .....	868
31.2	<i>A New Multiple Weight Set Calculation Algorithm</i> H.-S. Kim*, J.-K. Lee, S. Kang .....	878
31.3	<i>Test Vector Encoding Using Partial LFSR Reseeding</i> C. Krishna*, A. Jas, N. Touba .....	885
31.4	<i>Two-dimensional Test Data Compression for Scan-based Deterministic BIST</i> H.-G. Liang*, S. Hellebrand, H.-J. Wunderlich .....	894

**SESSION 32: TEST AUTOMATION, IMPROVING IC TEST EFFICIENCY**

Session Chair: M. Abadir, Coordinator: B. Sutton

32.1	<i>Rapid-Response Temperature Control Provides New Defect Screening Opportunities</i> M. Malinoski*, B. West .....	903
32.2	<i>Optimal Production Test Times through Adaptive Test Programming</i> S. Benner*, O. Boroffice .....	908
32.3	<i>A New Methodology for Improved Tester Utilization</i> A. Khoche*, R. Kapur, D. Armstrong, T.W. Williams, M. Tegethoff, J. Rivoir .....	916

**SESSION 33: FPGA TESTING**

Session Chair: A. Benso, Coordinator: P. Prinetto

33.1	<i>IS-FPGA : A New Symmetric FPGA Architecture with Implicit SCAN</i> M. Renovell*, P. Faure, J. Portal, J. Figueras, Y. Zorian .....	924
------	--	-----

# Table of Contents

33.2	<i>BIST-based Delay-Path Testing in FPGA Architectures</i> I. Harris*, P. Menon, R. Tessier .....	932
33.3	<i>On-line Testing of Transient and Crosstalk Faults Affecting Interconnections of FPGA-implemented Systems</i> C. Metra*, A. Pagano, B. Ricco .....	939
<b>SESSION 34: RF TESTING</b>		
Session Chair: J. Sylla, Coordinator: J. Kasten		
34.1	<i>Moving from Mixed-Signal to RF Test Hardware Development</i> M. Slamani*, J. Ferrario, R. Wolf, H. Ding .....	948
34.2	<i>A Phase Noise Spectrum Test Solution for High-Volume Mixed-Signal/Wireless Automatic Test Equipments</i> H. Nam*, B. Cuddy, D. Luecking .....	957
34.3	<i>Testability Implications in Low-Cost Integrated Radio Transceivers: A Bluetooth Case Study</i> S. Ozev*, C. Olgaard, A. Orailoglu .....	965
<b>SESSION 35: EMBEDDED MEMORIES TEST AND REPAIR</b>		
Session Chair: H. Hidaka, Coordinator: R. Rajsuman		
35.1	<i>Embedded DRAM Built-in Self-Test and Methodology for Test Insertion</i> P. Jakobsen*, J. Dreibelbis, G. Pomichter, D. Anand, J. Barth, M. Nelms, J. Leach, G. Belansek .....	975
35.2	<i>Shadow Write and Read For At-Speed BIST of TDM SRAMs</i> Y. Wu*, L. Calin .....	985
35.3	<i>Memory Built-in Self-Repair Using Redundant Words</i> V. Schoeber*, S. Paul, O. Picot .....	995
<b>SESSION 36: LECTURE SERIES—LOGIC BIST CASE STUDIES</b>		
Session Chair and Coordinator: S. Davidson		
36.1	<i>An Effort-minimized Logic BIST Implementation Method</i> X. Gu*, S.-S. Chung, F. Tsang, J. Tofte, H. Rahmanian .....	1002
36.2	<i>BIST and Fault Insertion Re-use in Telecom Systems</i> G. Carlsson*, S. Dikic, L.-J. Fritz, D. Dell'Aquila .....	1011
36.3	<i>Use of BIST in Sun Fire™ Servers</i> J. Braden*, Q. Lin, B. Smith .....	1017
<b>SESSION 37: ADVANCED METHODS IN EMBEDDED CORE TEST</b>		
Session Chair: F. Muradali, Coordinator: A. Orailoglu		
37.1	<i>Test Wrapper and Test Access Mechanism Co-Optimization for System-on-a-Chip</i> V. Iyengar*, K. Chakrabarty, E. Marinissen .....	1023
37.2	<i>Configuration-free SOC Interconnect BIST Methodology</i> C. Su*, W. Tseng .....	1033
<b>SESSION 38: HOW COULD WE MODEL AND TEST VDSM DEFECTS</b>		
Session Chair: T. Storey, Coordinator: C. Metra		
38.1	<i>Boolean and Current Detection of MOS Transistor with Gate Oxide Short</i> M. Renovell*, J. Galliere, F. Azais, Y. Bertrand .....	1039
38.2	<i>Testing for Resistive Opens and Stuck Opens</i> J. Li*, C.-W. Tseng, E. McCluskey .....	1049

= presenter

- 38.3 *An Evaluation of Defect-oriented Test: WELL-controlled Low-Voltage Test*  
Y. Sato\*, M. Kohno, T. Ikeda, I. Yamazaki, M. Hamamoto ..... 1059

**SESSION 39: PRACTICAL TEST GENERATION TECHNIQUES**

Session Chair: M. Hsiao, Coordinator: E. Rudnick

- 39.1 *Fast Test Generation for Circuits with RTL and Gate-level Views*  
S. Ravi, N. Jha\* ..... 1068
- 39.2 *Combinational Test Generation for Various Classes of Acyclic Sequential Circuits*  
Y. Kim\*, V. Agrawal, K. Saluja ..... 1078
- 39.3 *On Static Test Compaction and Test Pattern Ordering for Scan Designs*  
X. Lin\*, J. Rajski, I. Pomeranz, S. Reddy ..... 1088

**SESSION 40: DELVING INTO FACTORS AFFECTING MANUFACTURING COST**

Session Chair: K. Butler, Coordinator: A. Kinra

- 40.1 *Tackling Test Trade-offs from Design, Manufacturing to Market Using Economic Modeling*  
E. Volkerink\*, A. Khoche, L. Kamas, J. Rivoir, H. Kerkhoff ..... 1098
- 40.2 *A New Test/Diagnosis/Rework Model for Use in Technical Cost Modeling of Electronic Systems Assembly*  
T. Trichy, P. Sandborn\*, R. Raghavan, S. Sahasrabudhe ..... 1108
- 40.3 *Unit-level Predicted Yield: A Method of Identifying High-Defect Density-Die at Wafer Sort*  
R. Miller\*, W. Riordan ..... 1118

**SESSION 41: ATE HARDWARE: FROM GIGAHERTZ TO TERAHERTZ**

Session Chair: J. Larsen, Coordinator: B. Brown

- 41.1 *Pin Electronics IC for High-Speed Differential Devices*  
A. Oshima\*, J. Poniatowski, T. Nomura ..... 1128
- 41.2 *When Zero Picoseconds Edge Placement Accuracy is Not Enough*  
J. Cheng ..... 1134
- 41.3 *Terabit-per-Second Automated Digital Testing*  
D. Keezer\*, Q. Zhou, C. Bair, J. Kuan, B. Poole ..... 1143

**PANEL 1: SEARCHING FOR COMMON GROUND BETWEEN LOW-COST AND HIGH-PERFORMANCE ATE SYSTEMS**

Moderator: B. Bennetts, Organizer: A. Kinra ..... 1152

- P1.1 *Arriving at a Common Ground between Lower-Cost and Higher-Performance ATE Systems*  
S. Lomaro ..... 1153
- P1.2 *e-Diagnostics – Can ATE Vendors Step Up to the Challenge?*  
R. Madge ..... 1154
- P1.3 *A Common Ground Between DFT-based and Performance Testers*  
K. Posse ..... 1155

# Table of Contents

<i>P1.4 Common Grounds for Varied Testers</i>	
G. Robinson .....	1156
<i>P1.5 What Are the Right Criteria for ATE?</i>	
A. Kinra .....	1157
<b>PANEL 2: OPEN MICROPHONE – WANTED: NEW TEST DIRECTIONS AND PRACTICAL TEST BOTTLENECKS</b>	
Moderator: P. Nigh, Organizer: F. Muradali .....	1158
<b>PANEL 3: CAN ANYONE STILL AFFORD SYSTEM TEST?</b>	
Moderator: P. Sridhar, Organizer: B. Sutton .....	1159
<b>PANEL 4: THE CHALLENGES OF MANAGING TEST</b>	
Moderator: B. Stewart, Organizers: T. Barbour, C. Stolicny .....	1160
<i>P4.1 The Challenges of Managing Test</i>	
A. Goel .....	1161
<i>P4.2 Challenges of Managing Test</i>	
J. Harris .....	1162
<i>P4.3 The Challenges of Managing Test: Standardization</i>	
H.-T. Luh .....	1163
<b>PANEL 5: IS STRIP TESTING THE NEXT ADVANCE FOR SEMICONDUCTOR TEST?</b>	
Moderator and Organizer: R. Keus .....	1164
<i>P5.1 Is Panel Testing the Next Advance for Semiconductor Test?</i>	
J. Dawdy .....	1165
<b>PANEL 6: SYSTEM-IN-A-PACKAGE IS COMING TO CONSUMER PRODUCTS—IS TEST READY?</b>	
Moderator: D. Keezer, Organizer: A. Koche .....	1166
<i>P6.1 System-in-Package Testing Using Existing IEEE Test Standards</i>	
L. Whetsel .....	1167
<i>P6.2 SIP Moves Test Emphasis from Final to Probe</i>	
P. O'Neill .....	1168
<i>P6.3 The SIP Alternative</i>	
L. Gilg .....	1169
<b>PANEL 7: AC SCAN: MICROPROCESSORS ARE READY...BUT WHERE IS THE INFRASTRUCTURE?</b>	
Moderator: M. Mercer, Organizer: R. Raina .....	1170
<i>P7.1 AC-Scan: Microprocessors Are Ready . . . But Where Is the Infrastructure?</i>	
G. Aldrich .....	1171
<i>P7.2 Scan is Good Enough for Stuck Fault, Why Not AC Scan for Delay Faults?</i>	
K. McCauley .....	1172
<i>P7.3 AC-Scan: Microprocessors Are Ready . . . But Where is the Infrastructure?</i>	
R. Raina .....	1173
<i>P7.4 AC-Scan: Microprocessors Are Ready . . . But Where Is the Infrastructure?</i>	
S. Patil .....	1174



**PANEL 8: DFT—CORRECT BY CONSTRUCTION OR MAKE IT WORK?**  
Moderator: M. Ricchetti, Organizer: F. Muradali ..... 1175

*P8.1 Can DFT be "Correct by Construction"?*  
R. Aitken ..... 1176

*P8.2 The DFT Trip—Dad Are We There Yet?*  
A. Crouch ..... 1177

*P8.3 Design for Testability: Where Does It Fit in the Design Flow?*  
B. Dervisoglu ..... 1178

*P8.4 Correct-by-Construction DFT or Make-It-Work DFT—Where  
Are We Today?*  
G. Roberts ..... 1179

**PANEL 9: LOWERING THE COST OF TEST: ATPG VS. BIST**  
Moderator: R. Leckie, Organizers: Y. Zorian, C. Hay ..... 1180

*P9.1 ATPG Versus Logic BIST – Now and in the Future*  
K. Butler ..... 1181

*P9.2 The DFT Cost Dilemma*  
S. Davidson ..... 1182

*P9.3 Scan-based ATPG or Logic BIST?*  
T.W. Williams ..... 1183

**PANEL 10: STANDARDIZED TESTING OF AC-COUPLED ICs  
ON HIGH-SPEED BOARDS AND SYSTEMS**  
Moderator: A. Cron, Organizer: K. Parker ..... 1184

*P10.1 Testing Differential Signals*  
C. Barnhart ..... 1185

*P10.2 Trying to Solve the Problem of Testing AC-coupled,  
Differential Nets*  
B. Eklow ..... 1186

*P10.3 Boundary-Scan Testing of High-Speed Differential Signals*  
K. Filliter ..... 1187

*P10.4 Boundary-Scan Testing of AC-coupled Nets*  
K. Parker ..... 1188

*P10.5 Test AC-coupled Digital Pins with 1149.1 and 1149.4*  
S. Sunter ..... 1189

**2000 ITC BEST PAPER:**  
*A Stand-Alone Integrated Test Core for Time and Frequency  
Domain Measurements*  
M. Hafed, N. Abaskharoun, G. Roberts ..... 1190