Forward to the Special Section on "Materials, Processing, and Reliability of 3-D Interconnects"

THREE-DIMENSIONAL (3-D) integration has emerged as a potential solution to overcome the wiring limit imposed on chip performance, power dissipation and packaging form factor beyond the 32 nm technology node. The development of 3-D interconnects has been established as a focus area in the ITRS roadmaps. The fabrication of 3-D integrated circuits involves through-silicon vias (TSVs), wafer/die thinning, and wafer/die bonding. Those are structures and processes distinctly different from the copper interconnects, leading to serious materials and reliability challenges.

The development of the 3-D interconnects is at a rapid growth stage where innovative structure, design and processing are being developed at a fast pace. Technical exchange of information and research results can be particularly useful at this time to advance the development of this important technology. This is a special issue in the IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY devoted to current research on materials, processing, and reliability of 3-D interconnects. The issue contains 13 papers and is organized into two parts, one on materials and processing and the other on reliability. There are seven papers in the first part covering a wide range of subjects on design, fabrication, and materials characterization for 3-D integration. The papers on design and fabrication include one by Lee *et al.* "Design and Fabrication of a Silicon Interposer with TSVs in Cavities for 3D IC Packaging," on design and fabrication of silicon interposers, one by Tan *et al.* "3D Wafer Stacking Using Cu-Cu Bonding for Simultaneous Formation of Electrical, Mechanical and Hermetic Bonds," on Cu-Cu bonding for wafer stacking, one by Che *et al.* "Structure Design Optimization and Reliability Analysis on a Pyramidal Shape 3-Die Stacked Package with Through-Silicon Via (TSV)," on structure optimization using a pyramidal shape 3-die stack, and one by Chen *et al.* "A Wafer-level 3D Integration Scheme with Cu TSVs Based on Micro-bump/Adhesive Hybrid Bonding for 3D Memory Application," on the use of micro-bump/adhesive hybrid bonding for 3-D integration. The papers on material characterization include one by Yeap *et al.* "A Critical Review on Multi-Scale Materials Database Requirement for Accurate 3D IC Simulation Input," on multi-scale materials database, one by Karmarkar *et al.* "Copper Anisotropy Effects in Three-Dimensional Integrated Circuits using Through-Silicon Vias," on copper anisotropy effect on 3-D integration using TSVs and one by Chuang *et al.* "Critical Concerns in Soldering Reactions Arising from Space Confinement in 3D IC Packages," on effects of solder reactions on 3-D integrated packaging.

The second part on reliability consists of six papers reflecting issues arising from interactions between interconnect and packaging structures. These include one by Subbarayan *et al.* "Simulations of Damage, Crack Initiation and Propagation in Interlayer Dielectric Structures: Understanding Assembly-Induced Fracture in Dies," on chip-packaging interaction in 3-D structures, one by Jiang *et al.* "Effect of Thermal Stresses on Carrier Mobility and Keep-out Zone around Through-Silicon Vias for 3-D Integration," on keep-out zone around TSVs, one by Sitaraman *et al.* "Reliability Assessment of Through-Silicon Vias in Multi-Die Stack Packages," on reliability assessment of TSVs in multi-die stacks, one by Sukharev *et al.* "Physics-Based Models for EM and SM Simulation in 3D IC Structures," on electromigration and stress-migration simulation in 3-D IC structures, one by Cassidy *et al.* "Through Silicon Via Reliability," on TSV reliability and one by Lu *et al.* "Effects of Bonding Parameters on the Reliability of Fine-Pitch Cu/Ni/SnAg Micro Bump Chip-to-Chip (C2C) Interconnection for 3D Chip Stacking," on reliability of micro-bumps for 3-D die stacks.

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