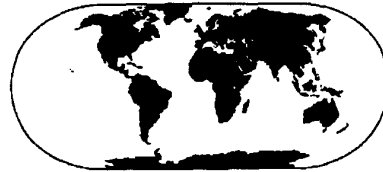


**Advanced Semiconductor
Manufacturing Conference and Workshop**



World Class Manufacturing

**2000
IEEE/SEMI®
Advanced
Semiconductor
Manufacturing
Conference
And Workshop**

“Advancing the Science of Semiconductor Manufacturing Excellence”

ASMC 2000 PROCEEDINGS

The IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop is an annual forum that provides a venue for the presentation of methodologies, approaches and techniques required to achieve world class semiconductor manufacturing. A key role this conference plays is in promoting interaction among semiconductor professionals at all levels. The goal and objective of the conference are to assist in making the participating companies more knowledgeable of semiconductor production methods, encourage open communication between participants, and develop the strategic relationship between users and suppliers needed to achieve manufacturing excellence and improve global competitiveness.

September 12 – 14, 2000
Boston, Massachusetts, USA

**2000 PROCEEDINGS
IEEE/SEMI ADVANCED SEMICONDUCTOR
MANUFACTURING CONFERENCE AND
WORKSHOP (ASMC)**

PERMISSION TO REPRINT OR COPY:

Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 09123 USA. For other copying, reprint or re-publication permission, write to IEEE Copyright Manager, IEEE Operations Center, 445 Hoes Lane, Piscataway, NJ 08855 USA; or SEMI, 805 East Middlefield Road, Mountain View, CA 94043 USA.

Copyright © 2000 by Institute of Electrical & Electronics Engineering, Inc. (IEEE)
All rights reserved

PRINTED AND BOUND IN THE UNITED STATES OF AMERICA

Additional copies of these Proceedings may be purchased from:

SEMI
3081 Zanker Road
San Jose, CA 95135 USA
Phone: 1.408.943.6900
<http://www.semi.org>

IEEE Service Center
445 Hoes Lane
Piscataway, NJ 08855-0060 USA
Phone: 1.732.981.0060
In the US 1-800-678-IEEE
<http://www.ieee.org>

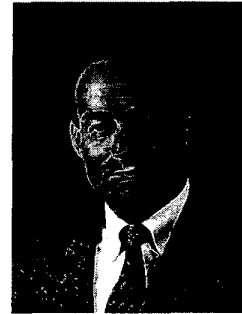
Refer to the IEEE Catalog Number, printed below:

IEEE Catalog Number;	00CH37072	
ISBN Number:	0-7803-5921-6	Softbound Edition
	0-7803-5922-4.1	Casebound Edition
	0-7803-5923-2	Microfiche Edition
ISSN:	1078-8743	

Layout, composition and compilation by
Semiconductor Equipment and Materials International (SEMI®)

Welcome to ASMC 2000

I would like to welcome you to the 11th Annual IEEE/SEMI Advanced Semiconductor Manufacturing Conference. The ASMC takes place during remarkable growth in our industry as we see the internet, communications, as well as the base computer semiconductor businesses fuel demand that in most circumstances is beyond the capacity of our industry. After several years of slow growth this has been a very welcome change to our industry, but where the focus has shifted from reducing costs to finding ways of getting more out of the installed base. The fundamentals of both is to increase fab productivity and this is the area with which the ASMC can help the semiconductor professionals.



The ASMC is the premier conference of the industry on improving semiconductor fabs productivity through yield improvements by defect detection and reduction, advanced processes and equipment to shrink die size, tool productivity/capacity increases, factory dynamics, and productivity improvements through teaming with equipment suppliers, manufacturing, and engineering as well as ensuring a well educated workforce that is focused on improving the full fabs productivity.

At ASMC 2000, we have set up the conference into sessions with presentations on the most up to date industry leading practices. Each session will be focused around an area of productivity, which we hope will foster and stimulate exchanges between the presenters and attendees. In addition we are again fortunate to have three keynote addresses. On day one, George Scalise, President of the Semiconductor Industry Association, will give the keynote on the outlook of the Semiconductor Industry; day two we will again have a presentation by GartnerGroup/Dataquest, which will be given by Klaus Rinnen, Director, Semiconductor Manufacturing Analysis Group, on Capital Spending and Fab Equipment Outlook; and day three we will have Bernard Meyerson, IBM Fellow and Vice President, Telecom Technology IBM Research Division give a presentation on The Emergence of Silicon Germanium Technology in Communications.

All presentations at ASMC are peer reviewed and selected by a dedicated team of industry professionals who have many years of experience in all aspects of the semiconductor business and whose goal is to deliver a conference that all attendees can learn something and take back to their fabs. Without this group ASMC could not take place and I would like to personally thank them all for their time and effort. I would especially thank Patricia Gabella, the ASMC Technical Chair for all her efforts for ASMC 2000, as well as Kim Conway, our General Chair for years of dedicated service to ASMC. Of special note and thanks is Margaret Kindling whose coordination is key to the success of ASMC.

In 2001, we will begin alternating ASMC between Europe and Boston as well as changing the conference timing to the spring to accommodate the growth of the industry in Europe and to coordinate with ISSM. The conference next year will take place April 23-24, 2001 in Munich, Germany. The ASMC committees will continue to dedicate themselves to delivering the top quality conference in the industry, and we look forward to expanding our European participation.

From all of the ASMC committee members we hope you find ASMC 2000 informative and are able to learn and take back with you new and useful techniques for improving your business.

William J. Miller – 2000 ASMC Conference Chairman
IBM Microelectronics

ABOUT THE ASMC SPONSORS



Semiconductor Equipment and Materials International (SEMI) is a global membership-based trade association serving more than 2,400 companies around the world that provide equipment, materials and services to the \$65 billion semiconductor and flat panel display industries. SEMI maintains offices in San Jose, Austin, Boston, Brussels, Hsinchu, Moscow, Seoul, Singapore, Tokyo and Washington, D.C. SEMI trade shows, sited worldwide SEMICON expositions, are just one of the many events that SEMI organizes. SEMI services include market data collection and reporting programs, technical and industry education programs, industry communications, worldwide public policy activities, export assistance, educational publications and audio/visual materials.

In addition, SEMI supports the development of standards that have become recognized as the only resource for manufacturing specifications accepted by the worldwide microelectronics industry. These standards incorporate the needs and recommendations of suppliers, customers, and industry consultants. Over 4,000 volunteers from every semiconductor region in the world, who serve on standards technical committees, work together to develop draft documents that are then balloted to members of the SEMI International Standards Program. The result of this effort is over 440 specifications covering process gases, process chemicals, equipment automation/hardware, equipment automation/software, facility specifications and safety guidelines, materials, microlithography, packaging, and traceability of importance to the global semiconductor and flat panel display industries.

Industry professionals, business experts, and respected members of the academic community and research institutions discuss the latest technological advances and timely industry issues at SEMI organized events scheduled throughout the year in the United States, China, Europe, Japan, Korea, Russia, Singapore, and Taiwan. These meetings provide opportunities for industry experts to exchange valuable technical knowledge. For information write to: SEMI, 3081 Zanker Road, San Jose CA 95134, USA.; phone 1.408.943.6900. For up-to-date information, visit the SEMI website at www.semi.org.



The Electron Devices Society (EDS) and the Components, Packaging, & Manufacturing Technology (CPMT) Society are two of the 36 technical societies within the Institute of Electrical and Electronics Engineers, which, in turn, is the largest professional engineering organization in the world with over 350,000 members. It is transnational, with conferences and chapters in most countries. EDS and CPMT also sponsor a number of other related conferences:

- VLSI Chip Packaging Workshop
- Semiconductor Thermal and Temperature Management (SEMI-THERM) Symposium
- International Electron Devices Meeting (IEDM)
- International Symposium on Semiconductor Manufacturing (ISSM)
- Intersociety Conference on Thermal Phenomena in Electronic Systems (I-THERM)
- Electronic Components & Technology Conference (ECTC)
- International Electronic Manufacturing Technology (IEMT) Symposium

Copies of past proceedings of some of these conferences are available for purchase. In addition, EDS and CPMTS publish the Transactions on Semiconductor Manufacturing, the archival journal in this field. We invite you to consider membership for one of the IEEE Societies and to participate with us in furthering advancements in these fields. If you already belong to another professional society, you can affiliate with EDS or CPMT at reduced fees. Please refer to the back cover for additional information.

2000 ASMC ORGANIZING COMMITTEE

Our special appreciation to the following people who together volunteered countless hours to the organization of the IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop:

GENERAL CHAIR

Kim Conway, Alpha Industries, Inc.

CONFERENCE CHAIR

William Miller, IBM Microelectronics

TECHNICAL CHAIR

Patricia Gabella, International SEMATECH (AMD Assignee)

Prashant Aji, KLA-Tencor Corp.
Duane Boning, Massachusetts Institute of Technology
Mark Burns, KLA-Tencor Corp.
Tom Carbone, Fairchild Semiconductor
Gary Cheek, WaferTech
Susan M. Cogley, IBM Microelectronics
John Conway, Intel Corp.
Kim Conway, Alpha Industries
Craig Core, Analog Devices, Inc.
Rick Cosway, Motorola, Inc.
Michael Della Selva, Sarnoff Corporation
Christopher Demetrius, Numerical Technologies
Mel Effron, Yield Management Assoc.
David Fletcher, KLA-Tencor Corp.
Patricia Gabella, International SEMATECH
John Goodman, Entegris, Inc.
Pradeep K. Goel, Lucent Technologies
Michael Goss, Lam Research Corp.
Mart Graef, Philips Research
Galen Halverson, Sony Semiconductor Co. of America
Martin Henry, STMicroelectronics
Christopher Hess, PDF Solutions, Inc.
Karl Hirschman, RIT Microelectronic Engineering
Marlene Jaworski, Shipley Company
Gary V. Johnson, IBM Microelectronics
Yuri Karzhavin, White Oak Semiconductor
James Kawski, Axcelis Technologies
William King, Novellus Systems, Inc.
Greg Klusewitz, Intersil Corp.
Patrice Koch, Applied Materials, Inc.
Mark N. Lakritz, MiCRUS
Fourmun Lee, Motorola, Inc.
Terry Leslie, Dominion Semiconductor
Christopher W. Long, SEMATECH (IBM Assignee)
Sid Marshall, SMA
Scott R. McClure, IBM Microelectronics
Christopher J. McDonald, Intel Corp.

Mike McIntyre, Advanced Micro Devices
Doron Meyersdorf, TEFEN Ltd.
Kirk Mikkelson, Entegris, Inc.
William Miller, IBM Microelectronics
James Moyne, University of Michigan
Bruce Nonnemaker, Alpha Industries
Sassan Nour, Shipley Company
Jose M. Padillo, i2 Technologies
Charles Pappis, Applied Materials, Inc.
Harold G. Parks, University of Arizona
Michael Pas, Texas Instruments
Michael Passow, IBM Corp.
Robert Pearson, Virginia Commonwealth University
Murty S. Polavarapu, Dominion Semiconductor
Kanti Prasad, University of Massachusetts at Lowell
Jeff Proulx, DuPont Photomasks, Inc.
Lawrence Pulvirent, Motorola, Inc.
Richard Quattrini, KLA-Tencor Corp.
Ray Rerick, Intersil Corp.
Michael Retersdorf, Advanced Micro Devices
Randall Rhoads, Applied Materials, Inc.
Rodney S. Ridley, Sr., Intersil Corp.
Ken Rose, Rensselaer Polytechnic Institute
Sujit Saha, Intel Corp.
Rajendra Singh, Clemson University
Stuart Spitzer, Polaroid Corp.
Andrzej Strojwas, Carnegie Mellon University
Hua Su, KLA-Tencor Corp.
Wanda Tomlinson, IBM Microelectronics
Tohru Tsujide, NEC Corp.
William W. Tyler, ULVAC Technologies
Jacek Tyminski, Nikon Precision Inc.
Peter van der Meulen, Brooks Automation
Robert Virgalla, FEI Corp.
Mitchell Weiss, PRI Automation
Paul Werbaneth, Tegal Corp.
Randy Williams, Intel Corp.
Douglas Wilson, Fairchild Semiconductor
Tim Wooldridge, Texas Instruments

Introduction to the 2000 ASMC

The 11th Annual IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC) has come into its second decade. ASMC continues to bring to the participants an excellent conference program focused on the business, operations, technology and manufacturing of semiconductors. These microchips (and nanochips) are the heart and essence that drive the electronics revolution. This revolution includes the Internet, the World Wide Web, global telecommunications and networking, computers that now fit into one hand and the ease and portability of world wide communication, data gathering and data manipulation. Eleven years ago the Internet was only available to a small few and the World Wide Web was being proposed. The overall electronics industry is now a major market affecting the global economy and semiconductors make that all possible. As ASMC 2000 opens, the industry is in a year of growth and expansion which puts a strain on the human and capital resources which make manufacturing possible. The conference brings information and ideas to help make the industry productive during these growth times.



This year's program again brings a premier selection of presentations in the areas of business, operations, technology and manufacturing of semiconductors. ASMC 2000 includes excellent articles in the areas of educating and training the workforce, cost and profitability, equipment productivity and effectiveness, factory dynamics, defect reduction for yield enhancement, defect source methodology, yield analysis and modeling, process specific yield, process control, advanced processes for lithography, etch, front end of the line deposition, cleaning, and chemical mechanical polish. In addition, another fine poster session will be held on day one of the conference.

We have the great honor of having three fine keynotes again this year, opening each day of the conference. Opening ASMC is George Scalise, President of the Semiconductor Industry Association, who will look at the future of semiconductor industry and global impact. Day two, Klaus Rinnen, Director of Development for the Semiconductor Manufacturing Analysis Group at Dataquest (Gartner Group) will give an update on capital spending and the equipment industry. On the last day of the conference, Bernard Meyerson, IBM Fellow and Director of Telecom Technology in the IBM Research Division, gives a talk on the emergence of silicon germanium technology in communication, enlightening the ASMC community on the alternative technology platforms that have been developed to expand performance.

Our panel this year on day two promises to offer some stimulating challenges to ponder. Entitled "Dare to Share", Ajit Manocha, Senior Vice President and General Manager of MOS3 and MOS4YOU will lead ASMC in a discussion encouraging more open exchange among manufacturers during the pre-development phase of a technology node to help continue the acceleration of electronics technology. Come prepared to share your views on an interesting and occasionally controversial subject.

ASMC is a great opportunity to know your peers, exchange ideas, challenge each other and hold open discussions. The best of the best in semiconductor manufacturing are at the conference, so do not miss the opportunity to develop relationships and engage in two-way interaction.

ASMC would not continue to be the excellent conference that it is without the dedicated volunteers on the committees that drive and guide the conference, seek out excellent articles and topics for presentation and give of their time to make this an outstanding conference. The ASMC committees would also like to recognize and thank Margaret Kindling, SEMI's Program Manager, East Coast Industry Programs, for all the hard work and effort in making ASMC a premier event. Additionally, the committee would like to thank IEEE and SEMI for their continued sponsorship of this conference. ASMC welcomes MICRO magazine's assistance and support this year.

As we head into another positive growth year for the semiconductor industry, ASMC continues to strive to provide a forum of the exchange of ideas towards making the semiconductor industry productive. The committee welcomes your suggestions and inputs to continue to make this conference an excellent event.

Have a great conference!

Patricia Gabella, ASMC 2000 Technical Chairman

Lithography Project Manager, Advanced Micro Devices at International SEMATECH

TABLE OF CONTENTS

Overview of SEMI and the IEEE

Process Specific Yield Learning

Invited: Evaluation of the Yield Impact of Epitaxial Defects on Advanced Semiconductor Technologies R. Williams, R. Jacques, <i>Intel Corp.</i> ; W. Chen, M. Akbulut, <i>KL A-Tencor Corporation</i>	1
Case Study For Root Cause Analysis of Yield Problems D. Malinaric, <i>ATMEL</i> ; R. Hoffmeister, <i>Wafer Pro Software</i> ; C. Sun, <i>KL A-Tencor Corporation</i>	8
Yield Enhancement Through Understanding The Particle Adhesion and Removal Mechanisms in CMP and Post-CMP Cleaning Processes J. Taylor, <i>IBM Microelectronics</i> ; A. Busnaina, <i>Clarkson University</i>	14
The Use of Historical Defect Imagery for Yield Learning K. Tobin, T. Karnowski, <i>Oak Ridge National Laboratory</i> ; F. Lakhani, <i>SEMATECH</i>	18
The 100% Yield Explanation Approach in Lucent Technologies Madrid M. Recio, M. Merino, V. Martín, J. Ayucar, J. Moreno, A. Godino, C. Mata, C. Morilla, A. Lorenzo, R. Fernández, J. Iñarrea, M. Alvarez, A. Sacedón, C. Mateos, K. Theryl, G. González, S. Cruceta, <i>Lucent Technologies Madrid</i>	26
Advanced Process Control Based on Lithographic Defect Inspection and Reduction A. Skumanich, J. Boyle, <i>Applied Materials</i> ; J. Leavy, <i>IBM Microelectronics</i>	33
Factory Dynamics	
Invited: Yield and Equipment Utilization Improvements Achieved Through Fab Conversion to Carbon Fiber/CF/PEEK Wafer Carriers and Carbon Fiber/Polypropylene Storage Boxes E. Merrill, J. Bostwick, <i>IBM Microelectronics</i> ; C. Gilhoi, K. Mikkelsen, <i>Entegris, Inc.</i>	41
Solving Tough Semiconductor Manufacturing Problems Using Data Mining R. Gardner, J. Bieker, S. Elwell, <i>ON Semiconductor</i> ; R. Thalman, E. Rivera, <i>Motorola, Inc.</i>	46
Measuring Efficiency of Semiconductor Manufacturing Operations Using Data Envelopment Analysis (DEA) T. Carbone, <i>Fairchild Semiconductor</i>	56
Maximizing Productivity Improvements Using Short Cycle Time Manufacturing (SCM) Concepts in a Semiconductor Manufacturing Line D. Martín, <i>IBM Microelectronics</i>	63
Effective Methodology For Movement of Rapid Turn Around Time (RTAT) Hardware in a Multi-flow Fabricator J. LaFreniere, L. Labanowski, <i>IBM Microelectronics</i>	68
The Positive Cycle Time Impact of Closely Monitoring Your Factory's Critical Tools J. Berry, N. Pierce, L. Serrano, S. Stankus, R. Darrington, W. Scott, B. Sinclair, <i>Motorola, Inc.</i>	75†
Yield Analysis and Modeling	
Invited: Technology Assessment of Commercially Available Critical Area Extraction Tools C. Long, <i>SEMATECH (IBM Assignee)</i> ; D. Maynard, <i>IBM Microelectronics</i> ; M.A. Bjornsen, <i>Agilent Technologies</i>	76
Critical Area Based Yield Prediction Using In-line Defect Classification Information J. Segal, A. Sagatelian, B. Hodgkins, <i>HPL, Inc.</i> ; B. Chu, T. Singh, H. Berman, <i>Dominion Semiconductor</i>	83
A Technology Development SRAM Approach With DFM Considerations M. Craig, D. Deshazo, S. Prior, B. Tranchina, M. Erhart, S.S. Mahant-Shetti, R. Taylor, <i>TestChip Technologies, Inc.</i> ; Y. Xing, E. Quek, K.L. Chok, N. Kamat, M. Redford, <i>Chartered Semiconductor Manufacturing, Singapore</i>	89
The Identification and Analysis of Systematic Yield Loss R. Langford, <i>Silicon Manufacturing Partners</i> ; G. Hsu, C. Sun, <i>KL A-Tencor Corporation</i>	92
A Defect-to-Yield Correlation Study for Marginally Printing Reticle Defects in the Manufacture of a 16MB Flash J. Erhardt, K. Phan, E. Backe, Q. Tran, B. Fletcher, <i>AMD - Submicron Development Center</i> ; B. Hopper, <i>Spotfire, Inc.</i> ; I. Peterson, A. Zuo, <i>KL A-Tencor, Corp.</i>	96
Combination of TCAD and Physical MOSFET Model for LSI Development Time Reduction K. Ishimaru, K. Kasai, Y. Fukaura, Y. Okayama, T. Imamura, S. Irie, T. Hirano, K. Watanabe, M. Ueno, K. Hashimoto, F. Matsuoka, <i>Toshiba Corp. Semiconductor Company</i>	103

† Not available at time printing.

Defect Source Methodology

Invited: Defect Localization Using Physical Design and Electrical Test Information Z. Stanojevic, D. M. H. Walker, <i>Texas A&M University</i> ; H. Balachandran, S. Jandhyala, <i>Texas Instruments, Inc.</i> ; F. Lakhani, <i>SEMATECH</i>	108
Optimizing Automatic Defect Classification Feature and Classifier Performance For Post-Fab Yield Analysis M. A. Hunt, <i>nLine Corp.</i> ; T. P. Karnowski, <i>Oak Ridge National Laboratory</i> ; C. Kiest, L. Villalobos, <i>Electroglas, Inc.</i>	116
In-line Wafer Inspection Data Warehouse For Automated Defect Limited Yield Analysis H. Iwata, M. Ono, J. Konishi, S. Isogai, T. Furutani, <i>Hitachi, Ltd.</i>	124
Multiple Applications of an Automatic Defect Review of SEM in Semiconductor Manufacturing Yield Enhancement B. Hance, <i>Advanced Micro Devices – Fab 25</i>	130†
In-Line SEM Based ADC For Advanced Process Control A. Skumanich, D. Farrington, <i>Applied Materials</i> ; W. Tomlinson, B. Halliday, <i>IBM Microelectronics</i>	131
Poster Session	
The Application and Use of ATPG Data In Problem Solving Efforts To Improve Yields on Advanced Microprocessors M. McIntyre, E. Ehrichs, <i>AMD</i>	138†
Bitmapped Yield Enhancement Solutions: A Case Study of Escalating Yield L. Jacobson, D. Crain, C. Joyce, <i>National Semiconductor</i>	139†
Comparative Study of Two KLA-Tencor Advanced Patterned Wafer Inspection Systems S. Rowley, S. Thorne, <i>Texas Instruments</i> ; A. Bousetta, C. Perry, C. Dutton, <i>KLA-Tencor Corp.</i>	141†
A Comparison of Extra Material Critical Area Extraction Methods G. Allan, <i>University of Edinburgh</i>	142
A Comparison of Inspection Strategy Models for Optimized Tool Utilization A. Skumanich, <i>Applied Materials</i>	152†
Contact Size Dependence of Highly Selective Self-Aligned Contact Etching with Polymer Formation and Its Mechanism Y.H. Liu, Y.L. Tu, W.Y. Lain, B.W. Chain, M. Chi, <i>Worldwide Semiconductor Manufacturing Corp. (WSMC)</i>	153
Critical Factors in Successful Transfer of Semiconductor Products Across Factories M. Pullon, G. Kong, <i>Motorola Inc.</i>	157
Effects of Dilute HCl Wafer Cleaning Solutions on Borophosphosilicate Glass Films R. Webb, R. Glahn, R.S. Ridley, Sr., <i>Intersil Corporation</i>	162
Fab Automation – Where’s the Payback D. Scott, <i>PRI Automation</i>	168
The Impact of Tolerance on Kill Ratio Estimation for Memory O. Patterson, M. Hansen, <i>Lucent Technologies</i>	175
Implementation of Best Known Methods J. Foster, T. Nugent, <i>TEFEN USA</i> ; P. Marxoux, <i>IBM</i>	181
Managing Arsenic in GaAs Fab Wastewater J. Peterson, <i>Motorola - SPS</i>	187
Preparing the Workforce for Semiconductor/VLSI Industry for the 21st Century at UMASS Lowell K. Prasad, <i>UMASS - Lowell</i>	193†
SmartBit™: Bitmap to Defect Correlation Software For Yield Improvement M. Merino, S. Cruceta, A. Garcia, M. Recio, <i>Lucent Technologies, Inc.</i>	194
Tighter Process Control and Reduced Cycle Times Using Off-line Recipe Setup S. Stevens, R. Harper, <i>Analog Devices, Inc.</i> ; P. Knutrud, A. Carlson, <i>Schlumberger</i>	199
Trace Gas Detection with CW Cavity Ring-Down Laser Absorption Spectroscopy W.B. Yan, <i>MEECO, Inc.</i> ; J. Dudek, K. Lehmann, P. Rabinowitz, <i>Princeton University</i>	203
Wafer Probe Process Verification Tools R. Enrique, C. Carlos, S.V. Javier, M. Julián, <i>Lucent Technologies, Inc.</i>	207

† Not available at time printing.

Educating and Training the Workforce

- Invited: **3 Massachusetts Semiconductor Manufacturing Companies Improve Their Workforce Productivity Through Collaboration with Community Colleges** 213
A. Yu, S. Gharib, *Alpha Industries*; L. Solomon, S. Dutru, *MA/Com*; J. Burke, D. Planchard, *Middlesex Community College*;
M. O'Connor, *Massachusetts Bay Community College*

- The Implementation of a Performance Management System in an 8 Inch Fabrication Facility Within A Unionized Workforce** 219
A. Acri, A. Markowski, R. Rerick, *Intersil Corporation*

- The Role of Retired Engineers in Pre-College Science and Mathematics Education** 227
C. Zahopoulos, D. Weedon, *RE-SEED, Northeastern University*

- Effects of Operator Grouping on the VLSI Final Test Facility Layout Scale** 231
K. Nakamae, W. Koga, H. Fujioka, *Osaka University*

Cost and Profitability

- Invited: **Effect of Fab Scale, Process Diversity and Setup on Semiconductor Wafer Processing Cost** 237
Y. Iwata, S. Wood, *Stanford University*

- Value-Based Dispatching for Semiconductor Wafer Fabrication** 245
N. Pierce, T. Yurtsever, *Motorola, Inc.*

- Maximizing Profitability Through Easy Information Transfer** 250
C. Weber, E. von Hippel, *Massachusetts Institute of Technology*

- Optimizing the Cost of Design Rule Modifications For Subsequent Generations of Semiconductor Technology** 256
A. Balasinski, *Cypress Semiconductor*

Advanced Process: Photo/Etch

- Invited: **An Integrated Hardmask/Poly RIE Process for Sub0.25 μ m Gate Etch** 263†
S. Shah, J. Andrews, *MiCRUS*; M. Goss, R. Kurjansky, *LAM Research, Corp*

- Stepper Exposure Field Uniformity Mapping Using Electrical Critical Dimension Measurements** 264
B. McCarson, T. Salisbury, *Motorola, Inc.*

- GC Hard Mask Open Tool CD Monitoring and Matching** 274
C. Yu, D. Bennett, J. Brown, *IBM ASTC*

- 2-in-1 Total Process Integration in MERIE Etch Chamber For Cu Dual Damascene Applications** 278
R. Wu, L. Zhang, J. Yang, J. Tsui, A. Jiang, J. Sun, J. Yuan, P. Hsieh, R. Hung, Y. Ye, G. Hsueh, *Applied Materials*;
J. Shieh, J. Liu, C. Tsai, *Taiwan Semiconductor Manufacturing Company*

- A Dry Process For Polymer Sidewall Residue Removal After Via-Hole Etching** 281
X. Han, M. Boumerzoug, R. Bersin, *ULVAC Technologies*; L. Mikus, A. Horn, D. Dopp, *Motorola, Inc.*

- Optical CD Applications for <200nm Lithography Control and Productivity Improvement** 287
E. Morita, F. Leung, C. Fruga, B. Gwynn, H. Pourmasr, R. Pierce, *Nikon Precision*

Defect Reduction for Yield Enhancement

- Invited: **Investigation and Elimination of Sphere Defects** 296
F. Lee, M. Newtran, T. Hulseweh, *Motorola, Inc.*

- Evaluation of the 'HiVoP' Above-Wafer In-situ Monitoring Sensor** 302
R. Williams, E. Wickesberg, R. Jacques, *Intel Corporation*; M. Bonin, D. Holve, *Process Metrics*

- Defect Reduction Methodology For Advanced Copper Dual Damascene Oxide Etch** 312
P. Biolisi, *IBM Microelectronics*; S. Ellinger, D. Morvay, *LAM Research Corp*

- Defect Control Methods for SIMOX SOI Wafer Manufacture and Processing** 323
M. Alles, J. Dunne, *IBIS Technology Corp.*; S. MacNish, M. Burns, L. Cheung *KLA-Tencor Corporation*

- Surface Cleaning Mechanisms and Future Cleaning Requirements** 328
A.A. Busnaina, H. Lin, N. Moumen, *Clarkson University*

- Elimination of Contamination in the Epitaxial Process For High-Volume Power Semiconductor Device Manufacturing** 334
R. Glahn, R. S. Ridley, Sr., *Intersil Corp*

† Not available at time printing.

Advanced Process: FEOL Deposition and Cleaning	
Invited: Tungsten Silicide Gate Stack Optimization for 170-nm DRAM Technology V. Rao, J. Morgan, J. Barden, Y. Karzhavin, P. Van Holt, R. Petter, H. Ollendorf, K. Christensen, D. Ricks, <i>Whiteoak Semiconductor</i> ; W. Hoesler, <i>Infineon Analytical Labs.</i>	340
Advanced Multi-Objective Control for Epitaxial Silicon Deposition A. Gower, D. Boning, <i>Massachusetts Institute of Technology</i> ; P. Rosenthal, <i>On-Line Technologies</i> ; A. Waldhauer, <i>Applied Materials, Inc.</i>	347
Developing a Manufacturable Process for the Deposition of Thick Polysilicon Films for Micro Machined Devices K. Nunan, G. Ready, P. Garone, G. Sturdy, J. Sledziewski, <i>Analog Devices</i>	357
The Influence of the Pre-Anneal Ambient on the Gate Oxide Integrity Effect of Copper Contamination B. Vermiere, H.G. Parks, <i>University of Arizona</i>	367
Effect of HCl and Chemical Clean on Thin Oxide Growth R. Naujokaitis, R. Cosway, <i>Motorola MOS 12</i>	372
Process Control	
Invited: A Tolerance Analysis for Manufacturing to Direct Process Capability Improvement Efforts K. Hirshman, <i>Rochester Institute of Technology</i>	377
Optimization of MOS Capacitor Based Short Flow for Monitoring Ion Implantation-induced Charging T. Brozek, C. Norton, <i>CISD Motorola, Inc</i>	387
A Novel Method for Statistical Process Control of Gate Oxide and Front-end Cleans Monitoring in a Manufacturing Environment R. Cosway, L. Pirastehfar, R. Root, T. Roche, R. Naujokaitis, <i>Motorola, Inc.</i>	392
A Sensor Fusion Based Methodology for Real Time Furnace Diagnostics J. Wang, C. Spanos, <i>University of California/Berkeley</i>	397
Quantifying the Capability of a New In-situ Interferometer W. Roberts, C. Gould, <i>Infineon Technologies</i> ; K. Rebitz, A. Smith, <i>Litel Instruments</i> ; J. Guerro, <i>Rochester Institute of Technology</i>	407
Advanced Process: Chemical Mechanical Polishing (CMP)	
Invited: Interconnect Strategies for Deep Submicron CMOS Manufacture K. Rose, C. Mark, <i>Rensselaer Polytechnic Institute</i>	413
Evaluation of an Advanced Wafer Carrier Design for ILD Planarization M. Jaso, T. Glynn, J. Giunta, D. Diefenderfer, <i>Dominion Semiconductor</i>	419
Development of Slurry Concentration Adjustable Tungsten Chemical Mechanical Planarization (CMP) Process X. Wang, J. Tan, P. Tan, C. Lin, H. Zhao, <i>Chartered Semiconductor Manufacturing Ltd.</i>	422
Nanotopography Effects on Chemical Mechanical Polishing for Shallow Trench Isolation B. Lee, T. Gan, D. Boning, <i>Massachusetts Institute of Technology, Microsystems Technology Laboratories</i> ; P. Hester, N. Poduje, <i>ADE Corporation</i> ; W. Baylies, <i>BayTech Group</i>	425
Post-Chemical-Mechanical Planarization Cleaning Application in Metallization C. Huynh, J. Chapple-Sokol, <i>IBM Microelectronics</i> ; K. Pope, <i>IBM Research Division</i>	433
Copper CMP Planarity Control Using ITM A. Ravid, A. Sharon, A. Weingarten, V. Machavariani, D. Scheiner, <i>Nova Measuring Instruments, Ltd.</i>	437
Equipment Productivity and Effectiveness	
Invited: STM Crolles TPM Deployment and Success Story C. Ribes, <i>STMicroelectronics</i>	444
Pilot Studies of the Manufacturing Worthiness of Mixed Chemistry Processing in a MERIE Plasma Tool J. Yang, L. Zhang, J. Tsui, A. Jiang, J. Sun, K. Vaidya, R. Wu, <i>Applied Materials</i>	451
Capacity Planning Model: The Important Inputs, Formulas, and Benefits T. Occhino, <i>White Oak Semiconductor</i>	455
Productivity Improvement Focus at White Oak Semiconductor Y. Karzhavin, <i>White Oak Semiconductor</i>	459
Determining the Capacity Components of Multi-Chamber Systems D. Martin, M. McClintock, R. Woods, <i>IBM Microelectronics</i>	466
Using Overall Equipment Effectiveness (OEE) and the Equipment Improvement Process (EI) to Improve Fab Throughput R. Freck, <i>Resource Dynamics International</i>	469
BIOGRAPHIES OF SPEAKERS	472

† Not available at time printing.