Guest Editorial
Special Section on the International Conference on Frontiers of Characterization and Metrology for Nanoelectronics

SINCE 1995, the International Conference on Frontiers of Characterization and Metrology for Nanoelectronics (formally titled "Characterization and Metrology for ULSI Technology") has provided a forum for the characterization and metrology community to meet and discuss important breakthroughs and challenges that directly and indirectly affect manufacturing. The methods and techniques presented have included many approaches: chemical and physical, electrical, optical, *in situ*, and real-time control and monitoring.

As the semiconductor industry continues to move toward silicon nanoelectronics and beyond, the introduction of new materials, innovative processing and assembly, novel devices, and new metrology bring formidable challenges. Characterization and metrology are key enablers for developing semiconductor materials, processes, and technology used in manufacturing today's sophisticated chips. The worldwide semiconductor community faces increasingly difficult challenges as it moves into manufacturing chips with feature sizes approaching 45 nm and less. The magnitude of these challenges demands special attention from those of us in the metrology and analytical communities. These challenges have led to the refocusing/renaming of the conference series, the newest entry of which will be held March 27–29, 2007, in Gaithersburg, Maryland.

The special section here presents a diverse selection of four papers from the last meeting held in March 2005. The authors were asked to expand and extend the scope of their work presented so that the latest developments were included. Papers were selected based upon the quality of the work and the potential interest from readers.

The four papers presented in this section report on metrology aspects for particle detection, strained-Si devices, transmission electron microscopy imaging, and metrology challenges for emerging research devices and materials.

"Detection of 30 nm–40 nm particles on bulk-silicon and SOI wafers using deep UV laser scanning" is by Akira Okamoto, Hitoshi Kuniyasu, and Takeshi Hattori (Sony). This paper discusses particle detection for both bulk-silicon and SOI surfaces and describes the challenges faced in small particle detection to meet the current ITRS roadmap requirements. The authors report on a wafer-surface particle detection system employing a new deep-ultraviolet all-solid-state continuous-wave laser as the light source to detect particles as small as 30 and 40 nm on unpatterned bulk-silicon wafers and SOI wafers, respectively.

"Metrology challenges for 45-nm strained-Si device technology" is by V. Vartanian *et al.* (Freescale Semiconductor). Strained-Si/SiGe CMOS technology has already been implemented at the 90- and 65-nm technology nodes. This paper describes the more extensive metrology and monitoring that needs to be implemented to continue the scaling progress. Materials and integration issues are investigated by a wide variety of techniques described: spectroscopic ellipsometry, X-ray reflectivity, X-ray fluorescence, X-ray diffraction, Raman spectroscopy, SIMS, Auger, Rutherford backscattering, and photoluminescence.

"Application of aberration-corrected TEM and image simulation to nanoelectronics and nanotechnology" is by Roar Kilass *et al.* (University of Texas Austin, Carl Zeiss, and SEMATECH). High-resolution transmission microscopy (HRTEM) and scanning TEM (STEM) provide critical information on structures and devices at nano-scale dimensions. This information proves invaluable in diagnostics and process development for manufacturing, as well as being instrumental for R&D. With the introduction of aberration-corrected lenses, images with sub-0.1-nm spatial resolution are now routine. This paper reviews the use of multislice imaging to interpret the resulting phase contrast images and then shows how silicon nanowires serve as useful test samples in developing microscopy methods for future generations of integrated circuits.

"Metrology challenges for emerging research devices and materials" is by Mike Garner and Eric Vogel (Intel and National Institute of Standards and Technology). The semiconductor industry is expected to undergo radical changes in design and manufacturing as silicon CMOS technology approaches fundamental limits. In this beyond CMOS era, what structures and devices will exist and what kinds of metrology will be most useful? This paper sets the stage for answering these questions and getting us prepared to tackle the difficult issues ahead of us.

I would like to thank the authors for their efforts in preparing their manuscripts and for submitting their materials on time to meet the manuscript deadlines. Finally, I thank Prof. D. Boning and Dr. Bob Doering for their encouragement and support of this special section.

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