Guest Editorial Special Section on Issues Related to Semiconductor Manufacturing at Technology Nodes Below 70 nm

DURING the last 40 years, increased wafer size, decreased line widths and larger capacities in wafer out per month have driven a decrease in cost and improved the performance, reliability, and functionality of semiconductor products. In order to continue this trend, manufacturing beyond 70-nm nodes poses many new challenges. The key new challenges include introduction of new materials, introduction of new processes, reduced time to market new products and overall cost reduction. Thus a major challenge is to provide a broad spectrum of knowledge that will lead to the continuation of the success of silicon integrated circuit (IC) manufacturing.

In the fall of 2000, the idea of a special section on manufacturing issues beyond the 70-nm node technologies was originated in the IEEE Electron Devices Society Technical Committee on Semiconductor Manufacturing. In conjunction with International Symposium on Semiconductor Manufacturing (www.issm.com) 2001, a half-day workshop on the same topic was also organized by three of the guest editors. Two of the papers presented in the workshop were invited to submit full papers in this special issue.

This special section contains a total of seven papers. Out of these seven papers, five are invited papers and two are contributed papers.

The first paper by Kim and Jeong describes the scaling issues and directions of capacitor over bitline (COB) stack dynamic random access memory (DRAM) cell below 100-nm technology node. The authors identify several essential technologies (e.g., metal–insulator–metal high dielectric constant capacitor with inner-cylinder-type storage node, planar memory cell transistor with spike-doped channel, storage node junction with low substrate doping, etc.) for the 70-nm node technology node. The well-proven $8F^2$ (minimum feature size F denotes the half pitch of bit line that is typically the tightest dimension of the DRAM cell) folded bit line architecture together with these technologies can make $8F^2$ COB stack cell the most suitable technology for 70- and 50-nm DRAM technology nodes.

The second paper by Krivokapic and Heavlin assesses the manufacturability of single gate (SG) and symmetric double-gate (DG) complimentary metal–oxide–silicon (CMOS) transistors for gate length between 15 and 70 nm. Using statistical modeling, the authors find that SG devices are manufacturable, in most cases have tighter distributions, are faster and consume less power. DG devices may be more suitable for low power applications and for circuits dominated by interconnect capacitance. For future technologies down to 25 nm, the authors expect ultrathin silicon single-gate fully depleted silicon-on-insulator devices to offer higher performance. At 20 nm, it is expected that DG technology will offer better nominal performance, but at the price of insufficient manufacturability.

In the third paper, Wakabayshi *et al.* investigate a tradeoff between performance and power consumption for below 70-nm MOSFETs. In order to optimize a supply-voltage, gate delay and energy-delay product trends are discussed using the characteristics with physical gate length of n-MOSFET as small as 24 nm. The authors show that the gate-delay dependence on the supply voltage down to 0.9 V is almost constant at the same off current of 0.1 nA/nm. On the other hand, the optimum supply voltage significantly depends on the short channel characteristics of the devices with physical gate length below 70 nm.

The fourth paper by Zhirnov *et al.* deals with the key issues in the design of sub-70-nm materials and processes. The authors examine salient materials and processing technologies that are believed to be necessary to sustain the continued cadence of mainstream silicon IC technology. The authors suggest the need for technologies that yield atomically smooth interfaces. In the context of next-generation patterning, the authors discuss the possible role of maskless patterning technologies. Tradeoffs involved in the precise control of the number and location of dopants for devices in the far nanometer regime are also considered. Briefly, environmental, safety, and health (ESH) issues and possible remedies for future generation process are also discussed.

In the fifth paper, Diebold reviews the key metrology issues for the 70-nm node technology. Due to increased aspect ratios, great advances in metrology and defect detection capability will be required. Memory devices will achieve line densities that will drive all areas of metrology. In this paper, the key metrology and defect trends for wafer manufacture are covered. The best available information on critical dimension, gate stack, and interconnect measurement and data management are described in light of the need to obtain statistically relevant information from microscopic features.

In the sixth paper, Shibata *et al.* describe the concept, fundamentals, and advantages of stencil mask ion implantation technology (SMIT). In the SMIT system, a stencil mask acts like a resist mask, and ions passing through the hole of the mask are implanted into selected regions of silicon substrate chip by

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chip. SMIT was applied to Damascene metal gate MOSFET fabrication process. As compared to conventional ion implantation process, lower manufacturing cost and shorter process time are obtained. The authors show that threshold voltage values can be controlled as effectively by implanted dose as they can be controlled in conventional implantation. In SMIT, reproducibility increases and parallelism of ion beam is better than that using conventional implanter because of small dot size.

The seventh and final paper of this special section, Imazono *et al.* propose and evaluate the double jet ionizer with the aim of eliminating electrostatic charge and contaminations from the ionizer. The double jet ionizer is made up of nozzles and jet emitters located at the center of the nozzles. The authors show that the number of particles from the emitters of the double jet ionizer can be reduced to $1/40$ of the number from the conventional nonjet ionizer. The concentration of ozone generated from the emitters of the double jet ionizer can be reduced to $1/20$ of the concentration from that of a conventional nonjet ionizer. Particle growth was absent from the emitter tip of the double jet ionizer.

The guest editors would like to thank all the authors for their hard work in preparing high-quality manuscripts and for promptly responding to reviewer's comments and suggestions. We would like to express our thanks to the Editor, Prof. D. Boning and previous Editor, Prof. G. May, for providing administrative help. Finally, we would like to express our gratitude to a large numbers of expert reviewers for their support in reviewing the manuscripts.

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From May 1979 to August 1979, he was Visiting Assistant Professor at the University of Waterloo, Waterloo, ON, Canada. He spent a year (1979–1980) at Colorado State University, Fort Collins, as Visiting Assistant Professor, Department of Electrical Engineering. In 1980, he joined Energy Conversion Devices, Inc., Troy, MI, as Senior Research Scientist and worked on amorphous silicon solar cells and thermoelectric devices. Part of the work done at Energy Conversion Devices resulted in one U.S. and four foreign patents. In August 1982, he joined the University of Oklahoma, Norman, as Associate Professor in the School of Electrical Engineering and Computer Science. In 1986, he was promoted to Professor, and in 1987, he became Director of the Microelectronics Laboratory. In January 1991, he joined Clemson University, Clemson, SC, as the first D. Houser Banks Professor in the Department of Electrical and Computer Engineering. From fall semester of 1996 to spring semester of 2000, he was the Director of the Materials Science and Engineering Program. Since November 1997, he has been appointed as the Director of Center for Silicon Nanoelectronics. He has published over 250 papers in various journals and conference proceedings in the area of solar cells, rapid thermal processing and semiconductor manufacturing. He is editor or co-editor of more than ten conference proceedings.

Prof. Singh was selected as an IEEE Distinguished Lecturer for Latin America in 1983. In 1987, he was selected by the United Nations as a Distinguished Technologist under transfer of knowledge through expatriate national (TOKTEN) scheme, India. At the University of Oklahoma, he won seven awards for his contributions to teaching, research, and service. He has served as guest editor of special issues of IEEE TRANSACTIONS ON ELECTRON DEVICES for the January 1992 (Topic: Rapid Isothermal Processing) and March 1998 (Topic: Process Integration and Manufacturability) issues and since February 2000, he is serving as the editor of IEEE TRANSACTIONS ON ELECTRON DEVICES. Currently, he is also serving on the steering committee of IEEE TRANSACTIONS OF SEMICONDUCTOR MANUFACTURING. He is also serving as chair of IEEE EDS Semiconductor Manufacturing Technical committee and member of IEEE EDS Nanotechnology Technical committee. He is also serving on the editorial board of *Journal of Nanoscience and Nanotechnology*. He has presented over 50 keynote and invited talks in various conferences. Professor Singh's most recent honors and awards include, 1998 Thomas D. Callinan Award of The Electrochemical Society, 1998 and 2002 Clemson University (CU) Faculty Excellence Award, and 1996 outstanding researcher award of CU Sigma XI Chapter. He is a Fellow of the Society of Optical Science and Engineering, American Association of Advancement of Science and ASM International, the Materials Information Society.

Robert R. Doering (M'81) received the B.S. degree in physics from the Massachusetts Institute of Technology, Cambridge, in 1968 and the Ph.D. degree in physics from Michigan State University, East Lansing, in 1974.

He joined Texas Instruments Incorporated (TI) in 1980, after several years on the faculty of the Physics Department at the University of Virginia. His physics research was on nuclear reactions and was highlighted by the discovery of the Giant Spin-Isospin Resonance in heavy nuclei in 1973. He is a Senior Fellow in Silicon Technology Development at TI. His primary area of responsibility is Technology Strategy. His previous positions at TI include: Manager of Future-Factory Strategy, Director of Scaled-Technology Integration, and Director of the Microelectronics Manufacturing Science and Technology (MMST) Program. The MMST Program was a five-year R&D effort, funded by DARPA, the U.S. Air Force, and TI, which developed a wide range of new technologies for advanced semiconductor manufacturing. The major highlight of the program was the demonstration, in 1993, of sub-three-day cycle time for manufacturing 350-nm CMOS integrated circuits. This was principally enabled by the development of 100% single-wafer processing. His early work at Texas Instruments was on SRAM, DRAM, and NMOS/CMOS device physics and process-flow design. Management responsibilities during his first 10 years at TI included advanced lithography and plasma etch as well as CMOS and DRAM technology development. He has authored over 140 published/conference papers and has 19 U.S. patents.

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Hidetoshi Koike (M'96) received the B.E. degree in 1984 and M.E. degree in 1986, in electronic engineering from Tokai University, Kanagawa, Japan, and the Ph.D. degree in 1999 in electronic engineering from Tohoku University, Sendai, Japan.

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Dr. Koike is a member of IEEE Electron Device Society, and Technical Committee member of Semiconductor Manufacturing. He is also a member of the Japan Program Committee of the International Symposium on Semiconductor Manufacturing (ISSM).

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In 1983 he joined Samsung Electronics Company Ltd., where he has been involved in the development of DRAMs, ranging from 64-kb to 1-Gb densities. Currently, he is a vice president responsible for the research and development of future memory technology. He has been a project leader for the development of world first 1-Gb DRAM using 0.18-μm CMOS technologies during 1994–1996. His current major activity is focused on the development of technologies for low-power and high-performance multigigabit density DRAMs. His research interests are memory device reliability, yield modeling on memory device, low power sub-0.15-μm CMOS technology, memory cell technology, and multilevel metallization for high performance of multigigabit DRAMs. He is also in charge of high-density ferroelectric memory technology. Recently, his group successfully demonstrated 4-Mb FRAM in which COB-1T1C cell structure was developed with multimetallization for high-density stand-alone ferroelectric memory as well as embedded application. He has much interest in applying SOI technology into DRAM application, resulting in the successful development of a 16-Mb SOI DRAM, which is the highest density ever, reported in 1994. He published more than 140 technical papers on the field of memory technology. He holds 60 patents related to memory technology. He plays an active part in advancing future memory technology through participating panel discussions of prime conferences such as VLSI technology symposium.

Dr. Kim twice received the grand prize of Samsung group for the successful developments of 1-Mb DRAM and 1-Gb DRAM in 1986 and 1996, respectively. He is listed in *Who's Who in the World* and nominated as *IBC's 21st Century Award for Achievement*. He will be listed in "*The Asia 500-Leaders for the new century*". He is a recipient of ISI's citation award for highly cited paper. Dr. Kim serves as a committee member of international electron device meeting (IEDM), he is a member of editorial advisory board of Microelectronics reliability.

Marc Heyns received the M.S. degree in 1979 and the Ph.D. degree in 1986, both from the Katholieke Universiteit Leuven, Belgium.

From 1979 to 1985, he held a fellowship from the National Fund for Scientific Research (NFWO) in the Laboratory for Physics and Electronics of Semiconductors of the K.U. Leuven, investigating the trapping and degradation of thermally grown SiO2-layers during various forms of carrier injection and field stressing. In January 1986, he joined IMEC where he is currently Department Director and responsible for a research group working on ultraclean processing technology, advanced gate stacks, thin dielectrics, epitaxial deposition of materials and environmentally benign processing technologies. In 2001, he was appointed IMEC Fellow. His current research topics include high-k dielectric materials, metal gate structures, advanced wet and dry cleaning technologies, single-wafer cleaning and environmentally friendly IC-production. He has authored or co-authored more than 350 technical papers in journals and conferences.