SOI MEMBRANE-BASED PRESSURE SENSOR IN STRESS SENSITIVE DIFFERENTIAL AMPLIFIER CONFIGURATION

M. Brezeanu[1], V. Dumitru[1], S. Costea[1], S.Z. Ali[2], F. Udrea[2], M. Gologanu[1], C. Bostan[1], I. Georgescu[1], V. Avramescu[1], O. Buiu[1]

[1]Honeywell Romania SRL, Sensors & Wireless Laboratory Bucharest,
169A Calea Floreasca, Building A, 014459, Bucharest, Romania
[2]Cambridge CMOS Sensors, Suite 820, 2nd Floor, 59 St Andrew's Street, Cambridge CB2 3BZ, UK
E-mail: mihai.brezeanu@honeywell.com

Abstract–*This paper introduces a pressure sensing structure configured as a stress sensitive differential amplifier (SSDA), built on a Silicon-on-Insulator (SOI) membrane. Theoretical calculation show the significant increase in sensitivity which is expected from the pressure sensors in SSDA configuration compared to the traditional Wheatstone bridge circuit. Preliminary experimental measurements, performed on individual transistors placed on the membrane, exhibit state-the-art sensitivity values (1.45mV/mbar).*

Keywords: *Pressure Sensor, SOI, Stress Sensitive Differential Amplifier (SSDA), Piezoresistive*

1. INTRODUCTION

For applications such as oil & gas storage and transportation, industrial and domestic boiler combustion monitoring, automotive and aerospace engine monitoring, steam pressure sensing, pressure sensors are expected to cope with harsh environments such as extended temperature range (-170^0C)–($+800^0$C), condensing and corrosive conditions, immersion in either oil or water.

Current pressure sensors with high sensitivity and able to operate in wide range of temperatures available on the market, like, for example, the Kulite XTEH-190 series [1], are based on the piezoresistive effect occurring in four resistors placed in Wheatstone configuration on a silicon membrane. Such pressure sensing structures operate at temperatures up to 482^0C. However, this technology suffers from several drawbacks: it is not CMOS-compatible, its maximum operating temperature cannot be further increased, and it has high power consumption levels. Pressure sensors based on polymer membranes, reported the literature [2, 3], seem a viable alternative for reducing power consumption, but their fabrication technology is still immature.

This paper introduces a pressure sensing structure based on the piezoresistive effect occuring in four Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) placed in stress sensitive differential amplifier (SSDA) configuration on a Silicon-on-Insulator (SOI) membrane. The SOI membrane technology, employing tungsten for metallization, is fully CMOS compatible and it has already proven its capability to cope with temperatures up to 600^0C, while requiring low power consumption (12mW at 600^0C) [4]. With suitable sensing layers, the structure has been successfully tested for gas sensing at temperatures up to 550^0C [5]. In the gas sensing structure, the sensing layer is meant to sense the targeted gas, while a ring MOSFET acts as a heater. In the SOI-based pressure sensing structure we propose, no sensing layer is needed, and the ring MOSFET is used as pressure sensing element. Based on the proven capability of the SOI technology, such a pressure sensor is expected to operate at temperatures up to 350^0C.

2. SSDA CONFIGURATION

The pressure sensor is based on a stress sensitive differential amplifier (SSDA) configuration [6], presented in Fig. 1. The configuration consists of two n-type MOSFETS, M1 and M2, acting as input differential pair, two p-type MOSFETS, M3 and M4, acting as current mirror and another n-type MOSFET, Mb, meant to bias the circuit. M1-M4 are placed on the SOI membrane (Fig. 2), while Mb is placed outside the membrane. A change in pressure difference leads to a strain applied to the SOI membrane. The strain determines a change in the M1-M4 channel carrier mobility which, in turn,

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determines a change of the M1-M4 drain current levels.

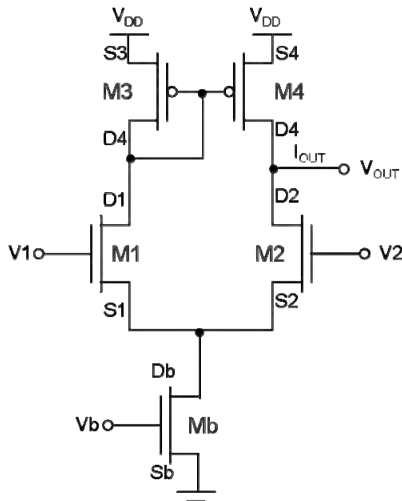

Fig. 1. SSDA configuration for pressure sensing.

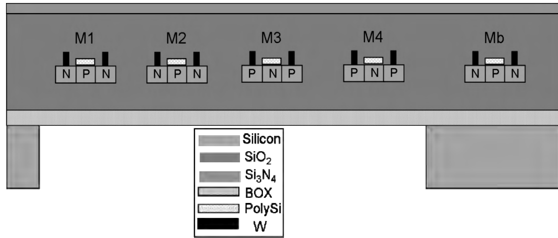

Fig. 2. SOI-based pressure sensor.

In order to understand the benefits of the SSDA configuration, we first take into consideration the situation when the SOI membrane, thus the SSDA circuit, is subject to no pressure difference. Since the gate and drain of M3 are connected together, M3 is in saturation. Therefore, its drain current is given by the following formula:

$$I_{D3} = \mu_3 C_{OX3} \left(\frac{W}{L} \right)_3 \frac{(V_{SG3} - V_{T3})^2}{2} \quad (1)$$

If we consider M4 to be in saturation ($V_{SD4} > V_{SG4} - V_{T4}$), assumption which is valid for low values of V_{OUT}, then the drain current of M4 is given by a formula similar to (1). Since M3 and M4 are built in the same technology (CMOS SOI) and they are both p-type, one can easily assume they have the same carrier (hole) mobility ($\mu_3 = \mu_4$), same geometrical dimensions ($(W/L)_3 = (W/L)_4$), and same threshold voltage ($V_{T3} = V_{T4}$). Therefore, $I_{D3} = I_{D4}$. At the same time, $I_{D3} = I_{D1}$ and $I_{OUT} = I_{D2} - I_{D4}$. The output current of the SSDA, I_{OUT}, when no pressure difference is applied to the membrane, is given by:

$$I_{OUT} = I_{D2} - I_{D4} = I_{D2} - I_{D3} = I_{D2} - I_{D1} \quad (2)$$

When a pressure difference occurs, it translates into a strain applied to the membrane. Numerical simulations indicate that, if M2 and M3 are placed as close as possible to the middle of the membrane, while M1 and M4 are placed as close as possible to the edges of the membrane, the two pairs (M2&M3 and M1&M4, respectively) respond in an antagonistic way to the strain applied to the membrane: when the channel conductivity of M2 and M3 increases, that of M1 and M4 decreases, and vice-versa. This influences channel carrier mobility. Thus:

$$\mu_1 \neq \mu_2 \quad (3)$$

$$\mu_3 \neq \mu_4 \quad (4)$$

In a first approximation, one can consider that the strain has no influence on the threshold voltage and on the geometrical dimensions of the MOSFETs. Therefore, I_{D3} and I_{D4} are in relation given by the mobilities ratio:

$$\frac{I_{D4}}{I_{D3}} = \frac{\mu_3}{\mu_4} \quad (5)$$

The output current becomes:

$$I_{OUT} = I_{D2} - \frac{\mu_3}{\mu_4} I_{D1} \quad (6)$$

The strain applied to the strain, ε, as result of the pressure difference, is given by:

$$\varepsilon = \frac{\frac{d\rho}{\rho}}{GF} \quad (7)$$

where ρ is the resistivity and GF is the gauge factor. For the p-type MOSFET, the resistivity is given by:

$$\rho = \frac{1}{qp\mu_p} \quad (8)$$

From (7) and (8), we have:

$$\frac{d\mu}{\mu} = -\frac{d\rho}{qp\rho^2} qp\rho = -\frac{d\rho}{\rho} = -GF * \varepsilon \quad (9)$$

If we consider GF to be the same for the p-type channel of M3 and M4, I_{OUT} becomes:

$$I_{OUT} = I_{D2} + \frac{\varepsilon_4}{\varepsilon_3} I_{D1} \quad (10)$$

It is thus obvious that, in the SSDA configuration, the output current is given by the superposition of three different phenomena. On one hand, there is the unbalance between the

mobilities in the channel of the p-type MOSFETs, M3 and M4, forming the current mirror. Secondly, there is the unbalance between the mobilities in the channel of the n-type MOSFETs, M1 and M2, which leads to the modification of I_{D1} and I_{D2}. Finally, the benefits of the Wheatstone bridge are also preserved by the SSDA configuration, by taking advantage of a third unbalance, the antagonistic effect that the pressure difference has on the transistor pairs M1 & M4 and M2 & M3, respectively. Therefore, the SSDA configuration is prone to significantly larger pressure sensitivities than the Wheatstone bridge circuit.

3. PRESSURE SENSOR DESIGN

The SOI membrane structure (Fig. 2) is obtained by the Deep Reaction Ion Etching (DRIE) of a bulk silicon layer of 375µm thickness, above which a 5 µm thick membrane, comprising layers of high quality SiO_2 (Buried Oxide = BOX), Silicon and SiO_2, is deposited. Silicon nitride (Si_3N_4) is used as passivation layer at the structure surface, tungsten is employed for circuit metallization, while poly-Silicon is the solution chosen for the MOSFETs gate. Transistors M1-M4 are placed on the membrane, while Mb is positioned outside. Numerical simulations show that the maximum stress point is 10µm from the edge for square SOI membranes (Fig. 3) and 6µm from the edge for circular SOI membranes (Fig. 3). At the same time, one can observe that the larger the membrane, the higher the stress peak next to the edge. Thus, for obtaining a pressure sensor with increased sensitivity, large membranes are required.

However, as the membrane dimensions increase, the pressure difference range which can be detected reduces because the membrane becomes more fragile and is capable to withstand lower stress levels. Thus, a trade-off needs to be done between sensitivity and targeted pressure range. For example, for a circular membrane with 560 µm diameter, the maximum pressure difference withstood is 1bar. Simulations also predict that circular membranes have less stress than square membranes. Taking all these into consideration, square membrane with curved corners seem to be the best option for high sensitivity and stable operation for a wide range of pressure variation.

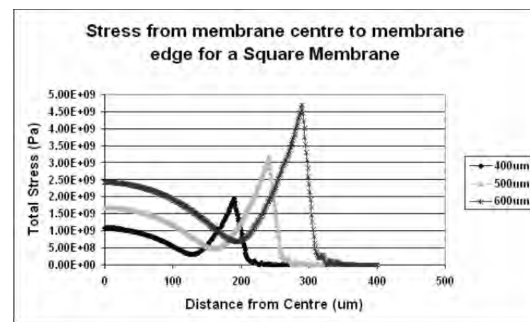

Fig. 3. Numerical simulation showing the distribution of the stress within a square SOI membrane.

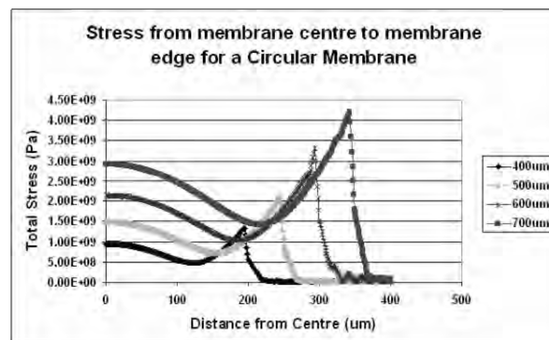

Fig. 4. Numerical simulation showing the distribution of the stress within a circular SOI membrane.

4. LAYOUT AND PRELIMINARY EXPERIMENTAL RESULTS

Based on the numerical simulations and theoretical calculations presented above, the layout in Fig. 5 was designed. In a 500µm × 500µm rectangular membrane with rounded corners, M1 and M4 were symmetrically placed at 10µm from the membrane edges, while M2 and M3 were symmetrically positioned at 10µm from the membrane center. The width/length (W/L) ratio was 6µm/1µm for the n-type MOSFETS and 12µm/1µm for the p-type MOSFETs.

Initially, chips allowing individual transistor measurements were fabricated (Fig. 6). The drain current of n-type M1 MOSFET exhibited a sensitivity of 1.45×10^{-5}mA/mbar when exposed to a pressure difference range from 0 to 170mbar (Fig. 7). For a typical load resistance of 100kΩ, this translates into 1.45mV/mbar. For comparison, the state-of-the-art piezoelectric PCB Piezotronics Series 106 High Sensitivity Pressure Sensors report 4.35mV/mbar sensitivity for a pressure range of 0-570mbar [7], while the piezoresistive Endevco 8510B pressure sensor report 1.45mV/mbar sensitivity for a pressure

range of 0-140mbar [8]. Thus, the SOI membrane technology proves its suitability for pressure sensing.

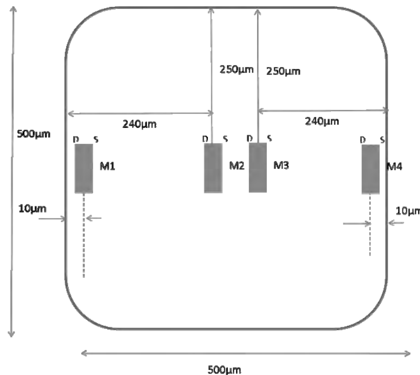

Fig. 5. Optimum design of the SSDA-based SOI pressure sensor.

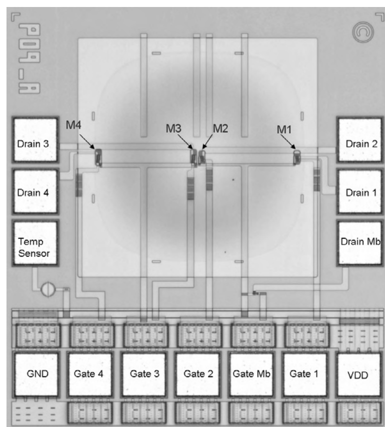

Fig. 6. Fabricated SOI pressure sensor chip suitable for individual transistor measurement.

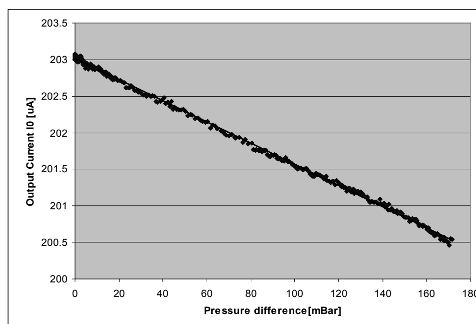

Fig. 7. M1 drain current variation with pressure difference applied on the SOI membrane.

In Fig. 8, the fabricated SOI pressure sensor chip based on the optimum theoretical design of the SSDA-configuration is shown. Next step is to perform extensive experimental measurements on this chip, in order to confirm the SOI-based SSDA configured pressure sensing capability.

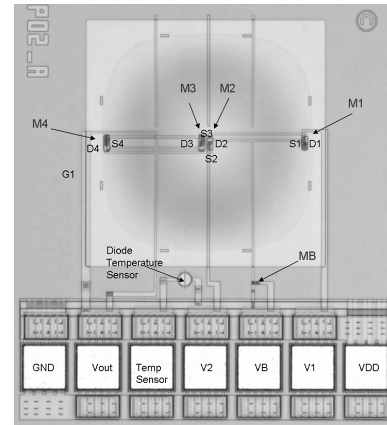

Fig. 8. Fabricated SOI pressure sensor chip based on the SSDA configuration.

5. CONCLUSIONS

A pressure sensing structure, in SSDA configuration, built on an SOI membrane, is presented. Theoretical calculations predict a significant increase in sensitivity expected from the SSDA-based pressure sensors compared to the traditional Wheatstone bridge circuit. Simulations lead to the fabrication of an optimum SSDA design, in which two MOSFETS are placed next to the edges of the membrane, while the other two are in the centre. Experimental results measured on individual transistors yield 1.45mV/mbar sensitivity, close to the state-of-the-art values.

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References

[1] www.kulite.com
[2] C. Cobianu, *et al.*, US Patent 7, 401, 525 B2, July 22, 2008.
[3] C. Cobianu, *et al.*, US Patent 7, 318, 351 B2, Jan 15, 2008.
[4] S.Z. Ali, *et al.*, Journal of Microelectromechanical Systems, **17**(6), pp. 1408–1417, 2008.
[5] P.K. Guha, *et al.*, Sens. and Actuat. **B127**, pp. 260–266, 2007.
[6] J. Li, *et al.*, Solid-State Electronics **48**, pp. 715–719, 2004.
[7] www.pcb.com
[8] www.endevco.com