Correspondence

Correction to "A Novel Joint-in-Via Flip-Chip Chip-Scale Package"

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In the above paper from the February 2006 issue, the biography for Teck Kheng Lee displayed the wrong author photo. His photograph and biography should appear as follows.

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Teck Kheng Lee (M'99) received the B.S. degree in mechanical engineering and the M.S. degree in materials science and engineering from the National University of Singapore in 1995 and 1999, respectively. He is currently pursuing the Ph.D degree in the School of Mechanical and Aerospace Engineering, Nanyang Technological University, Singapore.

He has been with the semiconductor packaging industry for the past ten years, working from the historical package of DIP to recent flip-chip packages. He joined the Institute of Microelectronics (IME), Singapore, in 1997, researching in the areas of MEMS, CSP, and flip-chip packaging. In 1999, he left IME and joined Micron Semiconductor Asia Pte Ltd, Singapore, where he worked in the areas of substrate and packaging technologies. Currently, he is a Senior Technical Member, responsible for substrate supplier management and leading some research programs in the field of advanced packaging and material characterization. He has authored and coauthored more than 10 international papers and currently holds 7 U.S patents, pending another 28 U.S patents.

Mr. Lee serves as a committee member for ICMAT and is also a member of the IEEE CPMT and IMPAS societies.

References

[1] T. K. Lee, S. Zhang, C. C. Wong, and A. C. Tan, "Joint-in-via flip-chip chip-scale package," *IEEE Trans. Adv. Packag.*, vol. 29, no. 1, pp. 186–194, Feb. 2006.

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