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Whole-Chip ESD Protection Design for RF and AMS ICs

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Abstract: As integrated circuits (IC) technologies advance into very-deep-sub-micron (VDSM), electrostatic discharge (ESD) failure becomes one of the most devastating IC reliability problems and on-chip ESD protection design emerges as a major challenge to radio frequency (RF), analog, and mixed-signal (AMS) IC designs. This paper reviews key design aspects and recent advances in whole-chip ESD protection designs for RF/AMS IC applications in CMOS technologies.

Key words: electrostatic discharge (ESD); ESD protection; radio frequency (RF); parasitic capacitance

Introduction

Semiconductor integrated circuit (IC) technologies continuously advance into the very-deep-sub-micron (VDSM) regime, which significantly improves circuit performance of analog, mixed-signal (AMS), and radio-frequency (RF) ICs. In particular, Si-based RF IC rapidly moves into main-stream wireless applications due to advances in CMOS technologies and circuit design techniques, reflected by improvement in key RF circuit parameters, such as cut-off frequency, maximum oscillation frequency, minimum noise figure and linearity, etc. Unfortunately, electrostatic discharge (ESD) protection design does not benefit proportionally from the advances in CMOS IC technologies at the same time. Consequently, on-chip ESD protection design rapidly becomes a grand design challenge to RF/AMS ICs at sub-100 nm nodes, particularly as RF IC operation quickly moves into the multi-GHz domain. Hence, it draws significant attentions and efforts in research and development of advanced RF ESD protection solutions[1-12]. The key problems in RF ESD protection circuit design include properly defining the uniqueness of RF ESD protection and accurately understanding the complex interactions between the ESD protection circuitry and the core RF IC circuit being protected[4]. In principle, RF ICs, typically used in wireless handheld devices, demand robust ESD protection because such devices are more prone to ESD-induced damages. The general principle for RF ESD protection remains the same, which is to provide a low-impedance current shunting path to discharge ESD transients without generating too much heat and to clamp the pad voltage to a sufficiently low level to avoid any dielectric rupture to CMOS[3]. This paper reviews various key aspects of ESD protection design for RF/AMS ICs and recent advances in the field.

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1 Whole-Chip ESD Protection

Figure 1 illustrates typical snapback I-V characteristics for an ESD protection structure where ESD-critical parameters are given for triggering (V_{t1}, I_{t1}, t_1), holding (V_h, I_h), discharging (R_{on}), and thermal breakdown (V_{t2}, I_{t2}). Several design considerations are critical to ensuring proper ESD protection.

Firstly, the triggering voltage (V_{t1}) must be lower than the breakdown voltage of the node under protection (e.g., BV_{DSS} for drain and BV_G for gate in CMOS) by a safety margin. Secondly, the holding voltage (V_h) should be higher than supply voltage (V_{DD}) by a margin to avoid any possible latch-up of ESD protection

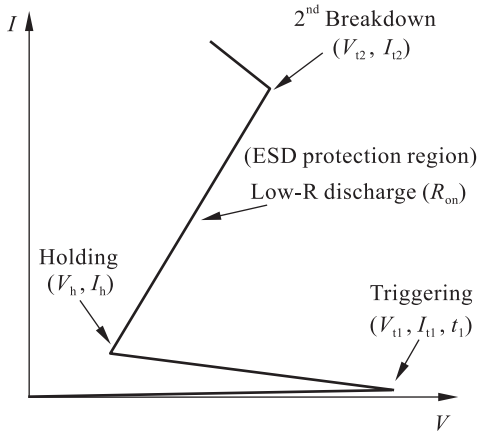

Fig. 1 Typical snapback *I-V* characteristics for an ESD protection structure

devices. Thirdly, the holding current (I_h) should be higher than the total supply currents (I_{DD}) on a chip to further eliminate possible latch-up effect. In other words, there exists a design window for good ESD protection design as illustrated in Fig. 2.

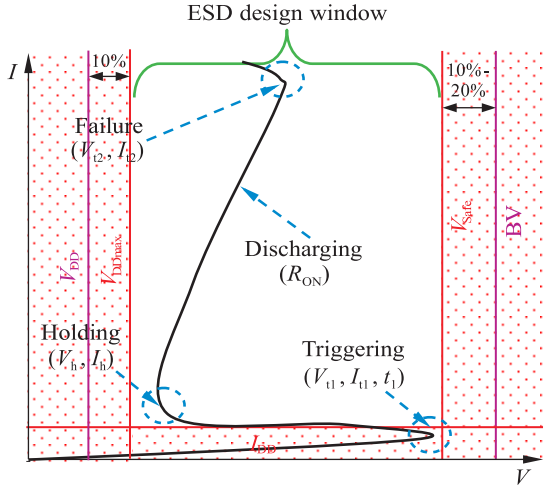

Fig. 2 ESD protection design window requires accurate design of ESD parameters to ensure proper ESD protection.

It is believed that this ESD design window is getting narrower for sub-100 nm CMOS if traditional ESD protection structures are used. For example, the BV_G for a 65 nm CMOS is around 3 V and an ESD V_{t1} of <3 V is required for sufficient input gate protection if ggNMOS ESD structure is used, which is extremely difficult, if even possible. Hence, it is imperative to explore novel non-traditional ESD protection mechanisms and structures to achieve very low ESD V_{t1} for VDSM CMOS.

It is important to understand that ESD protection design is application-specific in nature, which means that there is no portability for practical ESD protection design, or, one should not expect any universal ESD protection solution. However, practical ESD protection design is essentially a whole-chip design task, not a stand-alone ESD protection device design work.

First of all, a good practical ESD protection solution must ensure complete ESD protection for the whole IC chip. Figure 3 illustrates such a typical full-chip complete ESD protection scheme for a mixed-signal chip where ESD protection structures are used for all I/O pad to protect against all possible ESD pulse modes, i.e., positive (PD) and negative (ND) to V_{DD}, and positive (PS) and negative (NS) to V_{SS}, as well as a number of power clamping devices for all supply lines to defend against possible ESD surges from V_{DD} to V_{SS} (DS) or vice versa (SD)[4].

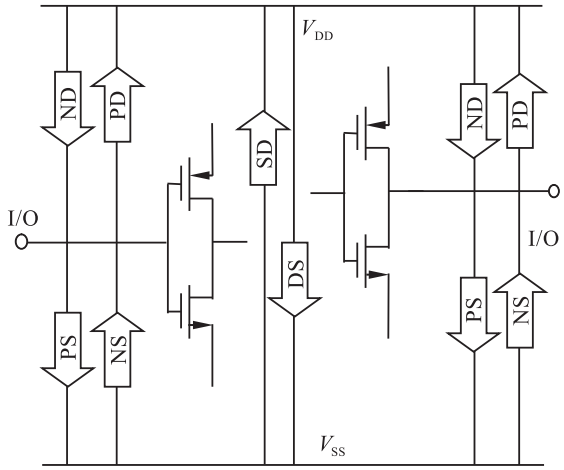

Fig. 3 Illustration of whole-chip complete ESD protection scheme using one-directional ESD protection devices

While practical IC products may adopt partial ESD protection only, full-chip complete ESD protection schemes would be ideal and should be considered if costs and parasitic effects are in controlled. This is because, as shown in Fig. 3, if traditional one-directional ESD protection devices are used, multiple ESD protection units may be needed to ensure all-active low-impedance full-chip ESD protection, which translates into significant ESD-induced parasitic effects and considerably large Si area used. To this end, novel multi-directional ESD protection structures are certainly advantageous as illustrated in Fig. 4 where dual-directional and multi-directional ESD protection structures are used to achieve complete ESD protection at whole-chip level while using fewer ESD protection devices and less Si. Secondly, AMS ICs often use

multiple supply buses and feature very different I/O circuitry. Smart and accurate whole-chip ESD protection scheme requires local-optimized ESD protection structures for different I/O blocks and supply lines. For example, while ESD protection structures of V_{t1}=4 V and 25 V may be ideal for circuitry blocks with V_{DD}= 3.3 V and 20 V, respectively; cross-use of such ESD protection structures might cause serious IC operation problems, such as short-circuit or slow ESD triggering. Smart ESD protection design approach should be I/O-specific with local optimization that achieves accurate ESD-critical parameter selection to ensure no under-design or over-design.

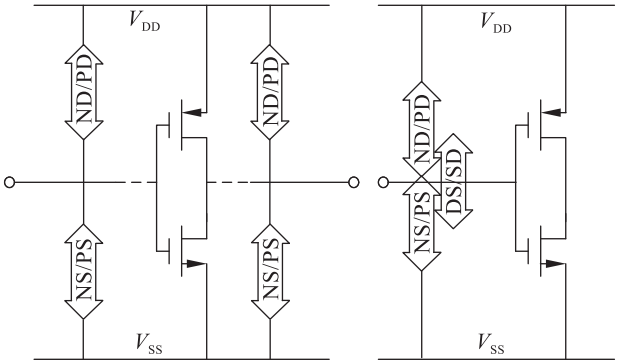

Fig. 4 Whole-chip ESD protection using dual-directional (left) and multi-directional (right) ESD protection structures results in fewer ESD protection devices, less ESD parasitic effects, and smaller Si area.

For emerging RF ESD protection design, it is critical to understand that RF ESD protection has unique features that are different from traditional IC ESD protection design. For instance, one key RF ESD protection design issue is to deal with the complex interactions between the ESD protection structure and the core RF IC circuit protected, which is defined as the ESD-circuit interactions[4]. Any ESD protection structure, being an extra device to the IC core, will inevitably introduce parasitic effects to the core circuit protected that negatively affect the chip performance, a phenomenon defined as the ESD-to-circuit influence[4]. While digital ICs are typically insensitive to the ESD-induced parasitic effects, which are often ignored by IC designers, such ESD-induced parasitic effects, including parasitic capacitance (C_{ESD}), resistance (R_{ESD}), noise coupling, and self-generated noises, etc, must be considered in RF IC design in order to avoid RF IC performance degradation due to ESD parasitic effects because RF ICs are extremely sensitive to any parasitic effect. This can be readily comprehended using the full-chip ESD protection scheme shown in Fig. 3. While the total number of ESD structures on a chip varies for different ESD protection requirements and types of ESD structures used, the total count of ESD protection units needed for full-chip complete ESD protection can be very large, resulting in substantial overall ESD-induced parasitic effects. On the other hand, the IC circuits may adversely affect the ESD protection circuit, a phenomenon defined as the Circuit-to-ESD influence[4]. For example, the normal RF signals are fast and strong, which may cause mis-triggering of an ESD protection structure, resulting in IC malfunction. Hence, RF ESD protection design must be particularly considered at whole chip level in order to ensure design success.

2 Cirucit Affects ESD Protection

Circuit-to-ESD influence phenomena state that the protected IC circuit may adversely affect the ESD protection structure, resulting in ESD protection performance degradation. In principle, an ESD protection device is a switch that remains OFF during normal circuit operation, however, can be turned ON by an ESD transient and forms a low-impedance conducting path to discharge the large ESD transients[3]. Critically, an ESD protection structure must be insensitive to any desired signals and its reasonable fluctuation; while it responds to any undesired ESD pulses efficiently and swiftly in order to provide ESD protection. However, it is observed that the displacement currents associated with any significant variation in incoming voltage signal ($\mathrm{d}V/\mathrm{d}t$) or current signal ($\mathrm{d}I/\mathrm{d}t$) may be coupled into the ESD devices through the parasitic capacitor and inductor, resulting in unwanted early turn-on of the ESD protection structures, which is defined as the mis-triggering of RF ESD protection structures[4]. The problem with this early triggering effect is that the ESD protection structure may be turned on by normal circuit signals, resulting in short-circuit and malfunction of the IC chip protected. This negative phenomenon can be understood from the following analysis.

It is observed in transmission line pulsing (TLP) measurements of ESD protection structures that the V_{t1} of an ESD protection structure may be altered by the TLP pulse rise time, t_r. TLP test data show that triggering voltage decreases as the TLP pulse rise time

decreases[4,13]. The triggering reduction effect is clearly shown in Fig. 5 for a group of different ESD protection structures including grounded-gate NMOS (ggNMOS, labeled NMOS1-3) and dual-direction silicon-controlled rectifier (SCR, labeled dSCR1-2) that were tested by a TLP tester with varying pulse rise time from 200 ps to 20 ns, where a strong relation of V_{t1} on t_r is readily observed. The relationship of V_{t1} - t_r is attributed to the displacement current associated with the substantial dV/dt of the incoming waveform. Taking a ggNMOS ESD protection structure shown in Fig. 6 as an example, ESD protection works when an ESD pulse appears at the drain and causes the drain junction breakdown.

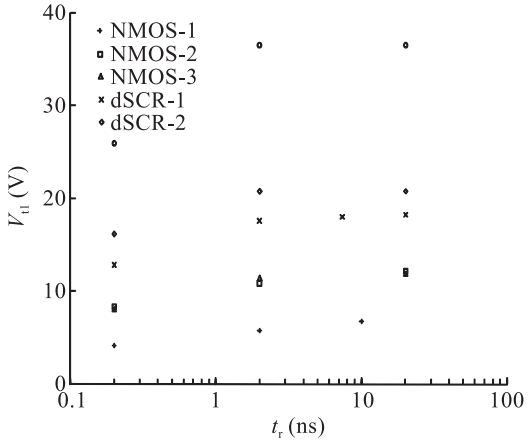

Fig. 5 Measured V_{t1}- t_r for different ESD protection structures shows strong relationship between ESD triggering and ESD pulse rise time.

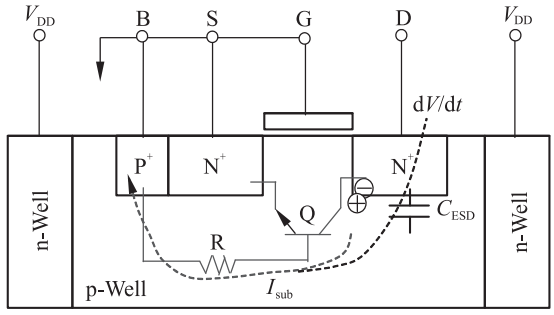

Fig. 6 Cross-section for a ggNMOS ESD protection structure depicts how ESD triggering occurs.

The avalanche current running through the p-well resistor will trigger the parasitic lateral NPN transistor, form a low-resistance conducting path, and then discharge. Apparently, the V_{t1} is directly controlled by the substrate current, I_{sub}. Hence, when unwanted dV/dt current across the drain junction capacitance (C_{ESD}) becomes significant, the displacement current, $i = C\dfrac{\mathrm{d}V}{\mathrm{d}t}$, will increase the I_{sub}, therefore accelerating the triggering process and reducing the V_{t1}. It is estimated that the required dV/dt threshold to turn-on the ggNMOS and SCR ESD protection structures ranges from 3×10^{10} V/s to 1×10^{11} V/s[4], shown as solid markers in Fig. 7. Meanwhile, typical dV/dt values for a set of human body model (HBM) ESD zapping testers, real HBM ESD waveforms and TLP testers are from 7×10^{8} V/s to 1×10^{11} V/s, shown in Fig. 7 as hollow markers[14]. These two groups of data are apparently at the same level, indicating that the dV/dt displacement does play a role in the V_{t1}-t_r relationship. Next, consider some RF IC circuit examples reported, for which the dV/dt data are extracted as ~2.5×10^{8} V/s for a 2.5 GHz CMOS clock recovery circuit[15], ~4.3×10^{7} V/s for a 1 GHz CMOS clock synthesizer chip[16], and ~1.23×10^{7} V/s caused by 7.1 MHz digital clock noise coupling in a mixed-signal CMOS receiver chip[17].

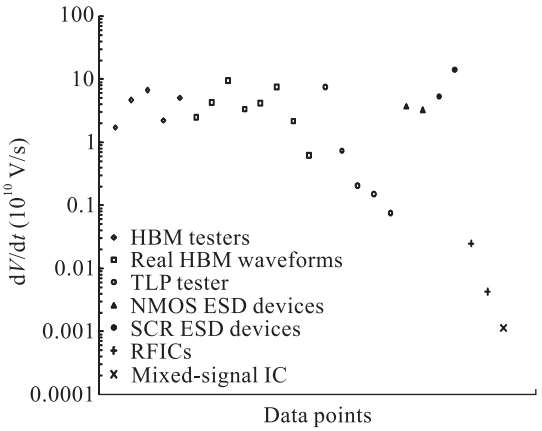

Fig. 7 dV/dt data for various ESD pulse waveforms, ESD protection structures, and normal RF/AMS signals.

Figure 7 shows that these dV/dt data for the practical RF ICs are still somewhat lower than the threshold dV/dt data needed to trigger an ESD protection structure for these examples. However, as the RF IC operation frequency gets higher and their signal becomes stronger, as being evident in the recent technology trends, it is inevitable that such mis-triggering effect will become a big issue in multi-GHz RF IC design where the ESD protection structures may cause chip malfunction by normal RF/AMS signals. It is, hence, imperative to explore novel ESD protection triggering mechanisms that are insensitive to the dV/dt effect.

3 ESD Affects RF IC Performance

Any ESD-induced parasitic effects will inevitably

affect circuit performance of IC protected. Such ESD-to-circuit influence effects include RC delay associated with the parasitic C_{ESD} and R_{ESD}, noise coupling between I/O and substrate due to C_{ESD}, ESD self-generated noises, and I/O impedance matching for RF ICs. All these ESD effects may substantially affect RF IC circuit performance, such as clock, signal integrity, RF impedance matching, power transfer efficiency bandwidth and noise figure, etc[4]. This section discusses RF IC design examples to demonstrate the ESD-to-circuit influences. In this study, two RF building circuits were designed including a 5 GHz low noise amplifier (LNA) and a 5 GHz mixer. The ESD protection used is an optimized ggNMOS structure with a width of 110 μm targeting for 2 kV HBM ESD protection level. The ggNMOS ESD structure is minimized using a mixed-mode ESD simulation-design methodology so that the measured parasitic C_{ESD} is only 0.41 pF. The designs were implemented in a commercial 0.35 μm SiGe BiCMOS technology[1,18]. Figure 8 shows the schematic for the LNA circuit, a two-stage high-gain LNA featuring on-chip impedance matching, power-down function, and high/low gain control. Its design specifications follow: power supply voltage V_{CC}=3 V, power consumption P_{supply}=19.8 mW, center frequency= 5 GHz, Gain=24 dB, noise figure NF=2.88 dB, and 3rd-order input intercept point IIP_3=−10.6 dBm.

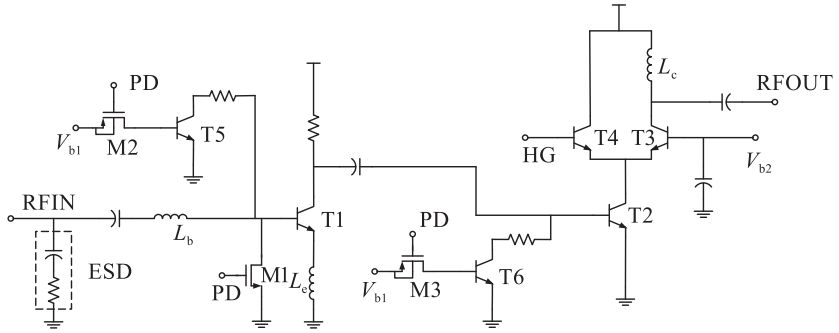

Fig. 8 Schematic for a two-stage LNA with and without ESD protection for comparison study

The ggNMOS ESD protection structure is connected at the input pad. The same LNA circuits without and with ESD protection were characterized with its critical circuit parameters listed in Table 1. It readily observes that all key LNA circuit specifications, e.g., gain (S_{21}), NF, reflection ratio (S_{11}), and bandwidth ($BW_{-3\,dB}$), are affected by the ggNMOS ESD protection structure substantially, even though the ESD protection structure was optimized for minimum parasitic effect by mixed-mode simulation in design.

Table 1 ESD+LNA circuit comparison

Specs	S_{21} (dB)	S_{11} (dB)	NF (dB)	BW_{-3dB} (GHz)
No ESD	24.25	−12	2.88	4.18-6.38
ggNMOS ESD	22.4	−7.5	4.28	4-6

Figure 9 shows the 5 GHz sub-harmonic direct down-conversion mixer with on-chip matching and featuring RF=5.25 GHz, local oscillation frequency LO=2.6 GHz, intermediate frequency IF=50 MHz, V_{cc}=3 V, P_{supply}= 10.8 mW, gain=2.16 dB, and NF=11 dB. The ggNMOS ESD protection structures are connected to both RF and LO ports. The mixer circuits with and without the ESD protection structures were characterized with its typical specifications listed in Table 2, which clearly shows that all the key circuit parameters, including gain, noise figure, and S_{11}, are significantly affected by the ESD protection structures as expected. These two examples demonstrate that even using an optimized RF ESD protection structure with minimum parasitic parameters, RF circuits may be substantially affected by the ESD-induced parasitic effects in practical designs. Therefore, such ESD-to-circuit influence must be carefully considered in practical RFIC designs.

Table 2 ESD + mixer circuit comparison

Specs	Conversion gain (dB)	S_{11} (dB)	NF (dB)
No ESD	2.16	−3.7	11.00
ggNMOS ESD	1.76	−3.0	12.35

4 RF ESD Protection Solutions

Due to the complex ESD-circuit interactions, designing RF ESD protection becomes very challenging. From previous discussions, it is clear that there is no universal all-fit RF ESD protection solution because

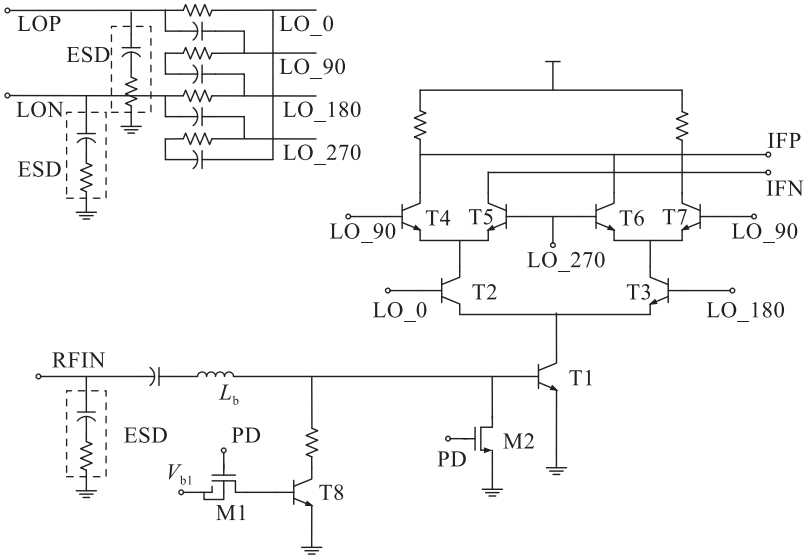

Fig. 9 Schematic for a mixer with and without ESD protection for comparison study

RF ESD protection design is really I/O-specific that strongly depends upon the RF IC circuits to be protected. In principle, any conventional ESD protection structure may be used for RF ESD protection as well, provided that the ESD-circuit interactions are fully considered and minimized. RF ESD protection is still an active research topic in the field.

Table 3 lists some key guidelines that should be considered in practical RF ESD protection circuit design. A few promising RF ESD protection structures are presented below. In general, novel, low-parasitic, compact, multiple-mode ESD protection structures are preferred for RF ESD protection. As an example, Fig. 10 shows the cross-section of a novel three-terminal all-mode ESD protection structure that delivers a high ESD protection to area ratio of 80 V/μm-width[19].

Table 3 RF ESD protection guidelines

Key factors	Comments
Triggering	Immune to normal RF signals
Low parasitics	Reduce ESD-to-circuit influences
Compact	Reduce parasitic; be layout friendly
Robustness	Higher RF ESD protection level
Constant C_{ESD}	Stable performance across bandwidth
Flexible V_{t1}	Meet specifications at different pads
Multiple-mode	Reduce count of ESD protection devices

The main advantage of this structure is that it guarantees an active low-R_{on} discharging path formed by a SCR-type device between any two terminals in both directions. As a result, only one such all-mode ESD protection device is needed at each I/O pad, as shown in Fig. 4 (right), to provide complete ESD protection

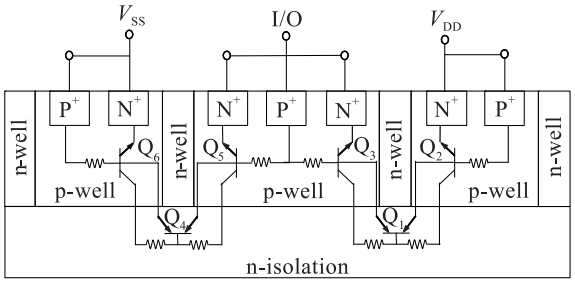

Fig. 10 Cross-section for a novel multi-directional SCR type ESD protection structure in CMOS

as compared to using up to four traditional one-directional ESD protection devices as illustrated in Fig. 3[20]. This protection scheme requires fewer and smaller ESD protection devices per chip, hence minimized total ESD-induced parasitic on a chip. It is generally believed that the widely used MOSFET type ESD protection structure is not a suitable RF ESD protection solution due to its large size and strong parasitic effect. Recently, a diode string has been considered as an attractive RF ESD protection solution due to its low total parasitic C_{ESD} in its series connection[7]. Certainly, one has to minimize diode dynamic resistance by designing proper sizes in order to make sure that the increase in voltage drop over the diode string would not cause a voltage clamping problem under large ESD currents. In the mean time, the Darlington application substantially increases the leakage in such diode-string ESD structures, which must be considered in designs[3]. Stacked diodes in polysilicon were reported to reduce the C_{ESD} and to suppress the Darlington effect; however, its poor heat dissipation may be a practical problem[6]. Further,

in using diode strings, other types of parasitic C_{ESD}, e.g., metal interconnects, might increase as more diodes are stacked up. Considering the conflicts in designing diode strings, one has to consider the overall ESD protection performance in practical design[4]. Recently, there are several designs reported to address the RF impedance mis-matching problem, including using a bonding wire inductor or an LC tank to ensure impedance matching and using transmission line coil networks to realize broadband ESD protection[10-12], etc. In fact, it is very desirable to have a new design method that can integrate RF IC design and ESD protection design in the same phase in order to optimize ESD-protected RF IC chip design. Such a new ESD-RFIC co-design method was recently reported, which achieves excellent whole-chip design optimization for some key RF block circuits[21,22].

Figure 11 shows the reported 2.4 GHz ESD-protected power amplifier (PA) circuit featuring 5 kV ESD protection using diode structure designed in a commercial 0.18 μm CMOS technology with its die photo shown in Fig. 12. In this study, the 5 kV ESD diode was optimized for minimum parasitic C_{ESD}. Unfortunately, the optimized ESD protection structure still affects the PA circuit performance due to I/O impedance mis-matching. The new ESD-RFIC co-design

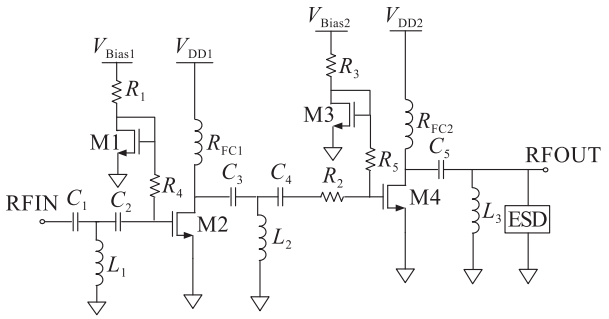

Fig. 11 Schematic for a PA circuit with and without ESD protection for comparison study

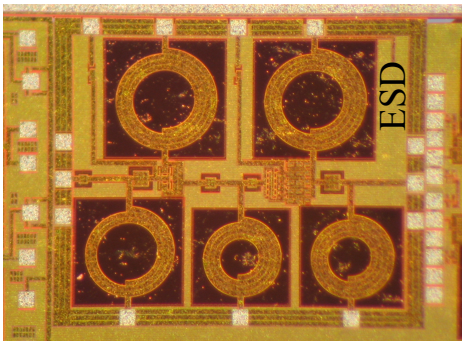

Fig. 12 Die photo for the ESD-protected PA circuit

method allows including the parasitic effects into PA circuit simulation by using a direct s-parameter insertion technique, hence, the I/O impedance corruption can be eliminated by re-matching the design.

Table 4 shows the PA gain comparison for the CMOS PA circuit in different conditions, i.e., without ESD protection, with 5 kV ESD protection and after ESD-RFIC co-design (ESD REM). It clearly shows that the ESD parasitic effect degrades PA gain performance substantially due to ESD-induced I/O mismatching, while such performance degradation can be almost recovered by using the new ESD-RF co-design method.

Table 4 S_{21} for the 2.4 GHz PA (dB)

No ESD	5 kV ESD	5 kV ESD REM
26.9	26.7	26.9

Layout is very critical to ESD protection design for at least two reasons: first, different ESD layout results in different parasitic effects; second, ESD protection structures are usually large and that makes full chip layout difficult. Hence, novel ESD protection layout design can be very beneficial for full chip design. Figure 13 shows one example novel pad-oriented all-mode ESD protection design that is very layout-friendly[19].

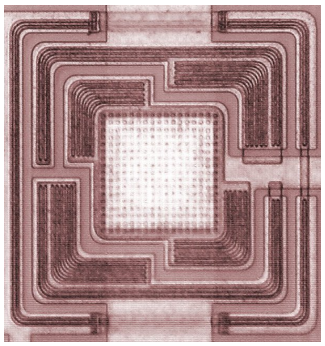

Fig. 13 Die photo for a novel multi-directional ESD protection

In addition, a well-thought-out whole-chip RF ESD protection scheme is highly preferred in RF ESD protection design. For example, Fig. 4 (left) illustrates a whole-chip RF ESD protection solution using dual-direction ESD protection structures[23], where a low-R, active SCR-type ESD discharging path is created between any two pads. Compared with an ESD protection scheme using traditional uni-direction ESD devices as shown in Fig. 3, the total number of ESD protection devices per chip is greatly reduced using this

scheme, resulting in much lower overall ESD-induced parasitics on chips. Use of a common ESD discharging bus can also help to reduce the number of ESD devices needed on a chip[3]. Recently, Xie et al.[24] reported a new low-parasitic polysilicon SCR ESD protection structure that achieved very low reported parasitic C_{ESD} of ~92.3 fF for a 3.2 kV ESD protection level as shown in Fig. 14. In brief, while there are many good RF ESD protection designs reported, exploring novel RF ESD protection structures remain an active and challenging design task to address the unique RF ESD protection problem.

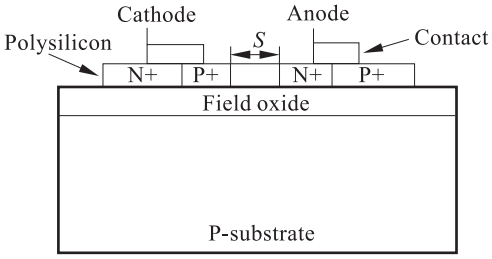

Fig. 14 Cross-section for a low-parasitic poly-Si diode ESD protection structure in CMOS

5 Accurate RF ESD Characterization

The complex ESD-to-circuit influences call for accurate characterization techniques for RF ESD protection designs. One new RF ESD evaluation method is to characterize its s-parameters, using a series or parallel C_{ESD}-R_{ESD} network[4], from which the parasitic C_{ESD} and R_{ESD} can be extracted and used for ESD-RF co-design[21,22]. In s-parameter measurement, a co-planar ground-source-ground (GSG) RF test pattern is required and a de-embedding dummy test pattern is also needed to ensure measurement accuracy. The following example depicts the s-parameter characterization procedure where a group of commonly used ESD protection structures were investigated, including ggNMOS, diode strings using N^+/Pwell diodes, SCR, and a dual-direction SCR structure (dSCR).

The diode strings consist of 1, 2, 3, 4, and 5 diodes (i.e., Dx1, Dx2, Dx3, Dx4, and Dx5). All ESD protection structures were designed and fabricated in a commercial 0.35 μm BiCMOS technology. For comparison purposes, all ESD protection structures were designed for 2 kV HBM[25] ESD protection level.

Figures 15 and 16 show the measured total parasitic ESD capacitances, C_{ESD}, in a 10 GHz spectrum for all the ESD protection structures studied. It is observed that the ggNMOS has the highest C_{ESD} due to its large size. For diode strings, the total C_{ESD} of the diode strings reduces in general as the number of diodes in the diode strings increases; however, it does not follow the trend of $C_{ESDtotal} = \dfrac{C_{junction}}{n}$. The reason is that the total measured C_{ESD} includes extra parasitic capacitances in addition to its junction capacitance. Hence, the reduction in total C_{ESD} is not governed by the above formula. Further, the measured data show that the C_{ESD} reduction trend saturates as the number of diodes increases to more than three in a diode string. Considering the fact that increasing the number of diodes in a diode string will result in linear increase in the total Si area consumed, it is obvious that, for RF ESD protection design with optimized overall specifications including parasitic C_{ESD} and total size, a two- or three-diode string seems to be an optimal RF ESD protection solution. In addition, it clearly shows that the dSCR is a favorable RF ESD protection structure because of its

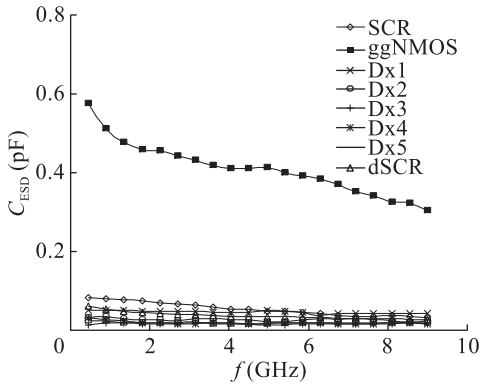

Fig. 15 Measured C_{ESD} for various ESD protection structures shows poor ggNMOS performance.

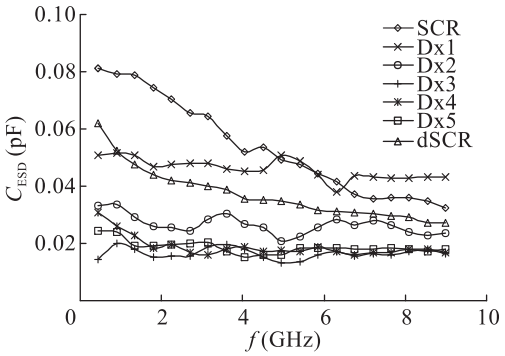

Fig. 16 Measured C_{ESD} for various ESD protection structures without ggNMOS

low C_{ESD}. For overall performance of the RF ESD protection structures, it is important to consider other factors, such as the layout sizes, in addition to the C_{ESD}.

Figure 17 shows the sizes of different ESD protection structures, which indicates that neither ggNMOS nor very large diode strings are good candidates for RF ESD protection structures. SCR ESD protection structures typically enjoy a small size. To better characterize the overall ESD performance of various RF ESD protection structures, a new figure-of-merit parameter, called F-factor, defined as $F = \dfrac{V}{\text{Size} \times C_{ESD} \times \text{NF}}$, was proposed in Ref. [4], where V is the ESD protection voltage level in volts and NF is noise figure.

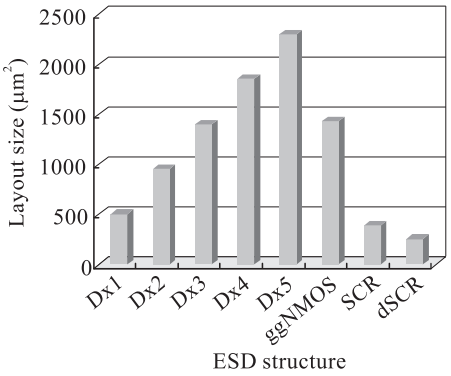

Fig. 17 Layout sizes for various ESD protection structures

Clearly, a large F value is preferred for a better RF ESD protection structure. Figure 18 shows the measured F-factor data, which indicates that the dSCR is the best RF ESD protection design and a 2/3-diode string can also be an attractive solution. In addition to s-parameter characterization, noise behavior should be evaluated as well by characterizing the noise figure of an RF ESD protection structure. This new RF ESD characterization method was further confirmed recently by a series of ESD protection design implemented in a commercial 0.13 μm RFCMOS technology, where Fig. 19 shows the measured parasitic $C_{ESD}-f$ curve across a 10 GHz spectrum for a 5 kV+ diode ESD protection structure that is optimized for very low C_{ESD} of less than 50 fF.

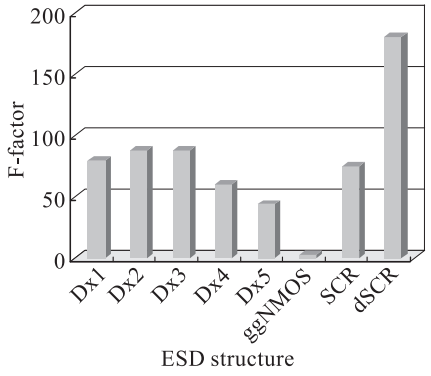

Fig. 18 F-factor for various ESD protection structures shows their overall ESD performance.

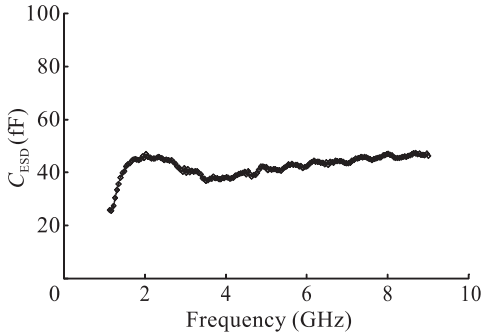

Fig. 19 Measured C_{ESD}-f characteristics for a 5 kV diode ESD protection structure in a commercial 0.13 μm RFCMOS

From these observations, a new RF-ESD co-design method that integrates measured ESD-parasitics into RF IC circuit simulation was developed recently, which makes it possible to realize full chip RF IC design optimization including ESD protection[21,22,25].

6 Summary

This paper reviews various key aspects and recent developments in RF/AMS ESD protection circuit designs, including unique challenges, ESD-circuit interactions, possible RF ESD solutions, and RF ESD characterization. It concludes that it is extremely important to deal with the complicated ESD-circuit interactions properly in order to achieve whole-chip RF/AMS IC optimization with adequate ESD protection. Practical design examples are presented to argue the new RF/AMS ESD protection design techniques.

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