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This index covers all technical items — papers, correspondence, reviews, etc. — that appeared in this periodical during 2007, and items from previous years that were commented upon or corrected in 2007. Departments and other items may also be covered if they have been judged to have archival value.

The Author Index contains the primary entry for each item, listed under the first author's name. The primary entry includes the coauthors' names, the title of the paper or other item, and its location, specified by the publication abbreviation, year, month, and inclusive pagination. The Subject Index contains entries describing the item under all appropriate subject headings, plus the first author's name, the publication abbreviation, month, and year, and inclusive pages. Note that the item title is found only under the primary entry in the Author Index.

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- Cheng, C. H.**, Pan, H. C., Yang, H. J., Hsiao, C. N., Chou, C. P., McAlister, S. P., and Chin, A., Improved High-Temperature Leakage in High-Density MIM Capacitors by Using a TiLaO Dielectric and an Ir Electrode; *EDL Dec. 2007 1095-1097*
- Cheng, C. Y.**, Fang, Y. K., Hsieh, J. C., Hsia, H., Sheu, Y. M., Lu, W. T., Chen, W. M., and Lin, S. S., Investigation and Localization of the SiGe Source/Drain (S/D) Strain-Induced Defects in PMOSFET With 45-nm CMOS Technology; *EDL May 2007 408-411*
- Cheng, H.-C.**, see Tsai, C.-C., *EDL July 2007 599-602*
- Cheng, H.-C.**, see Tsai, C.-C., *EDL Nov. 2007 1010-1013*
- Cheng, I.-C.**, see Kattamis, A. Z., *EDL July 2007 606-608*
- Cheng, K.-Y.**, see Lai, H.-C., *EDL Sept. 2007 837-839*
- Cheng, L.-W.**, see Lin, C.-T., *EDL Feb. 2007 111-113*
- Cheng, L.-W.**, see Lin, C.-T., *EDL May 2007 376-378*
- Cheng, L.-W.**, see Huang, Y.-T., *EDL Sept. 2007 815-817*
- Cheng, L.-W.**, see Lin, C.-T., *EDL Sept. 2007 831-833*
- Cheng, M.-L.**, see Lin, D.-W., *EDL Dec. 2007 1132-1134*
- Cheng, O.**, see Huang, Y.-T., *EDL Sept. 2007 815-817*
- Cheng, X.**, see Fu, Y., *EDL Feb. 2007 174-176*
- Cheng, Z.**, see Song, D., *EDL March 2007 189-191*
- Cheng, Z.**, see Cai, Y., *EDL May 2007 328-331*
- Cherenack, K. H.**, see Kattamis, A. Z., *EDL July 2007 606-608*
- Cherenack, K. H.**, Kattamis, A. Z., Hekmatshoar, B., Sturm, J. C., and Wagner, S., Amorphous-Silicon Thin-Film Transistors Fabricated at 300 °C on a Free-Standing Foil Substrate of Clear Plastic; *EDL Nov. 2007 1004-1006*
- Cheung, K. P.**, see Wang, Y., *EDL April 2007 279-281*
- Cheung, K. P.**, see Wang, Y., *EDL Jan. 2007 51-53*
- Cheung, K. P.**, see Wang, Y., *EDL July 2007 640-642*
- Chew, H.G.**, see Yu, H. P., *EDL Dec. 2007 1098-1101*
- Chi, D. Z.**, see Lee, R. T. P., *EDL Feb. 2007 164-167*
- Chi, D. Z.**, see Yu, H. P., *EDL Dec. 2007 1098-1101*
- Chi, S.**, see Liu, P.-T., *EDL May 2007 401-403*
- Chi, T.-W.**, see Su, K.-H., *EDL Feb. 2007 96-99*
- Chi, Y.**, see Huang, F., *EDL Nov. 2007 1025-1028*
- Chiang, K. C.**, Cheng, C. H., Jhou, K. Y., Pan, H. C., Hsiao, C. N., Chou, C. P., McAlister, S. P., Chin, A., and Hwang, H. L., Use of a High-Work-Function Ni Electrode to Improve the Stress Reliability of Analog SrTiO₃ Metal-Insulator-Metal Capacitors; *EDL Aug. 2007 694-696*
- Chiang, K. C.**, Cheng, C. H., Pan, H. C., Hsiao, C. N., Chou, C. P., Chin, A., and Hwang, H. L., High-Temperature Leakage Improvement in Metal-Insulator-Metal Capacitors by Work-Function Tuning; *EDL March 2007 235-237*
- Chiang, S.**, see Huang, Y.-T., *EDL Sept. 2007 815-817*
- Chien, C.**, see Lai, S., *EDL July 2007 643-645*
- Chien, C.-H.**, see Lin, Y.-H., *EDL April 2007 267-269*
- Chien, C.-H.**, see Chen, Y.-Y., *EDL Aug. 2007 700-702*
- Chien, C.-H.**, see Yang, M.-J., *EDL Oct. 2007 902-904*
- Chikyow, T.**, see Umezawa, N., *EDL May 2007 363-365*
- Chin, A.**, see Chiang, K. C., *EDL March 2007 235-237*
- Chin, A.**, see Wang, X. P., *EDL April 2007 258-260*
- Chin, A.**, see Wu, C. H., *EDL April 2007 292-294*
- Chin, A.**, see Chiang, K. C., *EDL Aug. 2007 694-696*
- Chin, A.**, see Yang, H. J., *EDL Oct. 2007 913-915*
- Chin, A.**, see Cheng, C. H., *EDL Dec. 2007 1095-1097*
- Chin, A.**, see Cheng, C. F., *EDL Dec. 2007 1092-1094*
- Chin, T. P.**, see Mei, X. B., *EDL June 2007 470-472*
- Chiou, Y.**, see Lai, S., *EDL July 2007 643-645*
- Chiou, Y. Z.**, Lin, Y. C., and Wang, C. K., AlGaIn Photodetectors Prepared on Si Substrates; *EDL April 2007 264-266*
- Chiu, F.-C.**, see Liu, C.-H., *EDL Jan. 2007 62-64*
- Chiu, S.-C.**, see Yang, M.-J., *EDL Oct. 2007 902-904*
- Cho, B. J.**, see Zang, H., *EDL Dec. 2007 1117-1119*
- Cho, B.-J.**, see Maji, D., *EDL Aug. 2007 731-733*
- Cho, C.**, see Kim, D., *EDL June 2007 520-522*
- Cho, C.**, see Kim, D., *EDL July 2007 616-618*
- Cho, H.-J.**, see Ragnarsson, L.-A., *EDL June 2007 486-488*
- Cho, H.-J.**, see Yu, H. Y., *EDL July 2007 656-658*
- Cho, K.**, see Kim, H., *EDL Jan. 2007 42-44*
- Cho, K. H.**, Suk, S. D., Yeoh, Y. Y., Li, M., Yeo, K. H., Kim, D.-W., Park, D., Lee, W.-S., Jung, Y. C., Hong, B. H., and Hwang, S. W., Temperature-Dependent Characteristics of Cylindrical Gate-All-Around Twin Silicon Nanowire MOSFETs (TSNWFETs); *EDL Dec. 2007 1129-1131*
- Cho, W.-S.**, Lee, H.-J., Lee, Y.-D., Park, J.-H., Kim, J.-K., Lee, Y.-H., and Ju, B. K., Carbon Nanotube-Based Triode Field Emission Lamps Using Metal Meshes With Spacers; *EDL May 2007 386-388*
- Choe, K.**, see Chae, Y., *EDL June 2007 495-498*
- Choi, C. H.**, see Akbar, M. S., *EDL Feb. 2007 132-134*
- Choi, L. J.**, Van Huylbroeck, S., Piontek, A., Sibaja-Hernandez, A., Kunnen, E., Meunier-Beillard, P., van Noort, W. D., Hijzen, E., and Decoutere, S., On the Use of a SiGe Spike in the Emitter to Improve the $f_T \times BV_{CEO}$ Product of High-Speed SiGe HBTs; *EDL April 2007 270-272*
- Choi, R.**, see Chang, M., *EDL Jan. 2007 21-23*
- Choi, R.**, see Wang, Y., *EDL Jan. 2007 51-53*
- Choi, R.**, see Heh, D., *EDL March 2007 245-247*
- Choi, R.**, see Wang, Y., *EDL April 2007 279-281*
- Choi, R.**, see Wang, Y., *EDL July 2007 640-642*
- Choi, R.**, see Heh, D., *EDL Aug. 2007 734-736*
- Choi, S.**, see Kim, M., *EDL Nov. 2007 967-969*
- Choi, W. K.**, see Yu, H. P., *EDL Dec. 2007 1098-1101*
- Choi, W. Y.**, Park, B.-G., Lee, J. D., and Liu, T.-J. K., Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec; *EDL Aug. 2007 743-745*
- Choi, Y.-K.**, see Han, J.-W., *EDL July 2007 625-627*
- Chou, C. P.**, see Chiang, K. C., *EDL March 2007 235-237*
- Chou, C. P.**, see Chiang, K. C., *EDL Aug. 2007 694-696*
- Chou, C. P.**, see Cheng, C. H., *EDL Dec. 2007 1095-1097*
- Chou, T. H.**, see Lai, C.-M., *EDL Feb. 2007 142-144*
- Chou, T.-H.**, see Lin, Y.-H., *EDL April 2007 267-269*
- Chow, L. L. W.**, Volakis, J. L., Saitou, K., and Kurabayashi, K., Lifetime Extension of RF MEMS Direct Contact Switches in Hot Switching Operations by Ball Grid Array Dimple Design; *EDL June 2007 479-481*
- Chu, J.-T.**, see Lu, T.-C., *EDL Oct. 2007 884-886*
- Chu, L. H.**, Chang, E. Y., Chang, L., Wu, Y. H., Chen, S. H., Hsu, H. T., Lee, T. L., Lien, Y. C., and Chang, C. Y., Effect of Gate Sinking on the Device Performance of the InGaP/AlGaAs/InGaAs Enhancement-Mode PHEMT; *EDL Feb. 2007 82-85*
- Chu, L.-H.**, see Lien, Y.-C., *EDL Feb. 2007 93-95*
- Chu, R.**, see Poblenz, C., *EDL Nov. 2007 945-947*

- Chu, R.**, Suh, C. S., Wong, M. H., Fichtenbaum, N., Brown, D., McCarthy, L., Keller, S., Wu, F., Speck, J. S., and Mishra, U. K., Impact of CF₄ Plasma Treatment on GaN; *EDL Sept. 2007* 781-783
- Chua, K. T.**, see Loh, W. Y., *EDL Nov. 2007* 984-986
- Chui, K.-J.**, see Ang, K.-W., *EDL April 2007* 301-304
- Chui, K.-J.**, see Ang, K.-W., *EDL June 2007* 509-512
- Chung, H. K.**, see Jeong, J. K., *EDL May 2007* 389-391
- Chung, T. M.**, see Simoen, E., *EDL Oct. 2007* 919-921
- Chyi, J.-I.**, see Chen, S.-H., *EDL Aug. 2007* 679-681
- Claeys, C.**, see Guo, W., *EDL April 2007* 288-291
- Claeys, C.**, see Simoen, E., *EDL Oct. 2007* 919-921
- Claeys, C.**, see Simoen, E., *EDL Nov. 2007* 987-989
- Clark, W. F.**, see Erturk, M., *EDL Sept. 2007* 812-814
- Clavelier, L.**, see Mayer, F., *EDL July 2007* 619-621
- Collaert, N.**, see Kapila, G., *EDL March 2007* 232-234
- Collaert, N.**, see Kilchytka, V., *EDL May 2007* 419-421
- Collaert, N.**, see Rudenko, T., *EDL Sept. 2007* 834-836
- Collaert, N.**, Rooyackers, R., De Keersgieter, A., Leys, F. E., Cayrefourcq, I., Ghyselen, B., Loo, R., Jurczak, M., and Biesemans, S., Stress Hybridization for Multigate Devices Fabricated on Supercritical Strained-SOI (SC-SSOI); *EDL July 2007* 646-648
- Compagnoni, C. M.**, Spinelli, A. S., and Lacaita, A. L., Experimental Study of Data Retention in Nitride Memories by Temperature and Field Acceleration; *EDL July 2007* 628-630
- Conard, T.**, see Ragnarsson, L.-A., *EDL June 2007* 486-488
- Conard, T.**, see Aoulaiche, M., *EDL July 2007* 613-615
- Cooper, J. A.**, see Sui, Y., *EDL Aug. 2007* 728-730
- Cooper, S.**, see Yu, C., *EDL Jan. 2007* 45-47
- Cordier, C.**, see Pichon, L., *EDL Aug. 2007* 716-718
- Cornu-Frueux, F.**, Penaud, J., Dubois, E., Coronel, P., Larrieu, G., and Skotnicki, T., Spacer-First Damascene-Gate FinFET Architecture Featuring Stringer-Free Integration; *EDL June 2007* 523-526
- Cornel, P.**, see Cornu-Frueux, F., *EDL June 2007* 523-526
- Corrion, A. L.**, see Poblencz, C., *EDL Nov. 2007* 945-947
- Crespo, A.**, see Jessen, G. H., *EDL May 2007* 354-356
- Cretu, B.**, see Guo, W., *EDL April 2007* 288-291
- Cretu, B.**, see Pichon, L., *EDL Aug. 2007* 716-718
- Culurciello, E.**, and Weerakoon, P., Three-Dimensional Photodetectors in 3-D Silicon-On-Insulator Technology; *EDL Feb. 2007* 117-119
- Cumming, D. R. S.**, see Khalid, A., *EDL Oct. 2007* 849-851

D

- Dang, B.**, see Sekar, D. C., *EDL Aug. 2007* 767-769
- Dang, L.**, see Mei, X. B., *EDL June 2007* 470-472
- Datta, A.**, Kumar, P. B., and Mahapatra, S., Dual-Bit/Cell SONOS Flash EEPROMs: Impact of Channel Engineering on Programming Speed and Bit Coupling Effect; *EDL May 2007* 446-448
- Datta, S.**, see Chang, C. Y., *EDL Oct. 2007* 856-858
- Datta, S.**, Dewey, G., Fastenau, J. M., Hudait, M. K., Loubychev, D., Liu, W. K., Radosavljevic, M., Rachmady, W., and Chau, R., Ultrahigh-Speed 0.5 V Supply Voltage In_{0.7}Ga_{0.3}As Quantum-Well Transistors on Silicon Substrate; *EDL Aug. 2007* 685-687
- Davis, J. A.**, see Sekar, D. C., *EDL Aug. 2007* 767-769
- Dawood, M. K.**, see Yu, H. P., *EDL Dec. 2007* 1098-1101
- De Gendt, S.**, see Ragnarsson, L.-A., *EDL June 2007* 486-488
- De Gendt, S.**, see Aoulaiche, M., *EDL July 2007* 613-615
- De Gendt, S.**, see Yu, H. Y., *EDL July 2007* 656-658
- De Jaeger, B.**, see Guo, W., *EDL April 2007* 288-291
- De Keersgieter, A.**, see Lousberg, G. P., *EDL Feb. 2007* 123-125
- De Keersgieter, A.**, see Collaert, N., *EDL July 2007* 646-648
- De Meyer, K.**, see Severi, S., *EDL March 2007* 198-200
- De Meyer, K.**, see Furnemont, A., *EDL April 2007* 276-278
- De Meyer, K.**, see Yu, H. Y., *EDL July 2007* 656-658
- De Meyer, K.**, see Veloso, A., *EDL Nov. 2007* 980-983
- De Meyer, K.**, see Singanamalla, R., *EDL Dec. 2007* 1089-1091
- DeVoe, D. L.**, see Marshall, J. C., *EDL Nov. 2007* 960-963
- Deal, W. R.**, see Mei, X. B., *EDL June 2007* 470-472
- Decoutere, S.**, see Choi, L. J., *EDL April 2007* 270-272
- Delabie, A.**, see Ragnarsson, L.-A., *EDL June 2007* 486-488
- Delabie, A.**, see Chang, S. Z., *EDL July 2007* 634-636
- Deleonibus, S.**, see Mayer, F., *EDL July 2007* 619-621
- Demand, M.**, see Veloso, A., *EDL Nov. 2007* 980-983

- Demeurisse, C.**, see Yu, H. Y., *EDL Feb. 2007* 154-156
- Deng, C.-K.**, see Chang, C.-W., *EDL Nov. 2007* 993-995
- Denning, L.**, see Huang, Y.-T., *EDL Sept. 2007* 815-817
- Desmaris, V.**, see Shiu, J.-Y., *EDL June 2007* 476-478
- Devriendt, K.**, see Masahara, M., *EDL March 2007* 217-219
- Deweerd, W.**, see Aoulaiche, M., *EDL July 2007* 613-615
- Dewey, G.**, see Datta, S., *EDL Aug. 2007* 685-687
- Dey, S.**, see Sarkar, J., *EDL May 2007* 449-451
- Dimitriadis, C. A.**, see Hatzopoulos, A. T., *EDL Sept. 2007* 803-805
- Do, Q.-T.**, Blekker, K., Regolin, I., Prost, W., and Tegude, F. J., High Transconductance MISFET With a Single InAs Nanowire Channel; *EDL Aug. 2007* 682-684
- Domeij, M.**, see Lee, H.-S., *EDL Nov. 2007* 1007-1009
- Dong, Y.-W.**, see Guo, P., *EDL July 2007* 572-574
- Dong, Z.**, see Xu, C., *EDL Nov. 2007* 942-944
- Doornbos, G.**, see Masahara, M., *EDL March 2007* 217-219
- Doutreloigne, J.**, see Bakeroot, B., *EDL May 2007* 416-418
- Droopad, R.**, see Rajagopalan, K., *EDL Feb. 2007* 100-102
- Droopad, R.**, see Hill, R. J. W., *EDL Dec. 2007* 1080-1082
- Duan, F.**, see Yu, C., *EDL Jan. 2007* 45-47
- Duane, R.**, Rafhay, Q., Beug, M. F., and van Duuren, M., Intrinsic Mismatch Between Floating-Gate Nonvolatile Memory Cell and Equivalent Transistor; *EDL May 2007* 440-442
- Dubois, E.**, see Cornu-Frueux, F., *EDL June 2007* 523-526
- Duffy, R.**, see Severi, S., *EDL March 2007* 198-200
- Dunn, G. M.**, see Khalid, A., *EDL Oct. 2007* 849-851
- Duttgupta, S. P.**, see Maji, D., *EDL Aug. 2007* 731-733

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- Eastman, L. F.**, see Felbinger, J. G., *EDL Nov. 2007* 948-950
- Echtermeyer, T. J.**, see Lemme, M. C., *EDL April 2007* 282-284
- Eisele, I.**, see Abelein, U., *EDL Jan. 2007* 65-67
- Eisenstein, G.**, see Mikhelashvili, V., *EDL Jan. 2007* 24-26
- Ejckam, F.**, see Felbinger, J. G., *EDL Nov. 2007* 948-950
- El Khakani, M. A.**, see Brassard, D., *EDL April 2007* 261-263
- Endo, K.**, see Liu, Y., *EDL June 2007* 517-519
- Endo, K.**, Ishikawa, Y., Liu, Y. X., Matsukawa, T., O'uchi, S., Ishii, K., Masahara, M., Tsukada, J., Yamauchi, H., Sekigawa, T., Koike, H., and Suzuki, E., A Dynamical Power-Management Demonstration Using Four-Terminal Separated-Gate FinFETs; *EDL May 2007* 452-454
- Endo, K.**, Ishikawa, Y., Liu, Y., Masahara, M., Matsukawa, T., O'uchi, S.-I., Ishii, K., Yamauchi, H., Tsukada, J., and Suzuki, E., Experimental Evaluation of Effects of Channel Doping on Characteristics of FinFETs; *EDL Dec. 2007* 1123-1125
- Eneman, G.**, see Shickova, A., *EDL March 2007* 242-244
- Erturk, M.**, Xia, T., and Clark, W. F., Gate Voltage Dependence of MOSFET 1/f Noise Statistics; *EDL Sept. 2007* 812-814
- Esseni, D.**, see Zilli, M., *EDL Nov. 2007* 1036-1039
- Everaert, J.-L.**, see Chang, S. Z., *EDL July 2007* 634-636
- Eyben, P.**, see Carnel, L., *EDL Oct. 2007* 899-901

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- Faili, F.**, see Felbinger, J. G., *EDL Nov. 2007* 948-950
- Fainbrun, A.**, see Stopel, A., *EDL May 2007* 357-359
- Fan, J.-F.**, see Lin, H.-T., *EDL Nov. 2007* 951-953
- Fang, W. W.**, see Singh, N., *EDL July 2007* 558-561
- Fang, W. W.**, see Rustagi, S. C., *EDL Nov. 2007* 1021-1024
- Fang, W. W.**, Singh, N., Bera, L. K., Nguyen, H. S., Rustagi, S. C., Lo, G. Q., Balasubramanian, N., and Kwong, D.-L., Vertically Stacked SiGe Nanowire Array Channel CMOS Transistors; *EDL March 2007* 211-213
- Fang, Y. K.**, see Cheng, C. Y., *EDL May 2007* 408-411
- Fang, Y.-K.**, see Lai, C.-M., *EDL Feb. 2007* 142-144
- Fang, Y.-K.**, see Lin, C.-T., *EDL Feb. 2007* 111-113
- Fang, Y.-K.**, see Lin, C.-T., *EDL May 2007* 376-378
- Fang, Y.-K.**, see Lin, C.-T., *EDL Sept. 2007* 831-833
- Fantini, P.**, see Ventrice, D., *EDL Nov. 2007* 973-975
- Fantini, P.**, Ghetti, A., Marinoni, A., Ghidini, G., Visconti, A., and Marmiroli, A., Giant Random Telegraph Signals in Nanoscale Floating-Gate Devices; *EDL Dec. 2007* 1114-1116

- Farrokh-Baroughi, M.**, and Sivovthaman, S., A Novel Silicon Photovoltaic Cell Using a Low-Temperature Quasi-Epitaxial Silicon Emitter; *EDL July 2007 575-577*
- Fastenau, J. M.**, see Datta, S., *EDL Aug. 2007 685-687*
- Fatima, H.**, see Agarwal, A., *EDL July 2007 587-589*
- Fay, P.**, see Su, N., *EDL May 2007 336-339*
- Fejes, P.**, see Rajagopalan, K., *EDL Feb. 2007 100-102*
- Felbinger, J. G.**, Chandra, M. V. S., Sun, Y., Eastman, L. F., Wasserbauer, J., Fäili, F., Babic, D., Francis, D., and Ejeckam, F., Comparison of GaN HEMTs on Diamond and SiC Substrates; *EDL Nov. 2007 948-950*
- Feng, H.-G.**, see Yang, C., *EDL July 2007 652-655*
- Feng, J.**, Woo, R., Chen, S., Liu, Y., Griffin, P. B., and Plummer, J. D., P-Channel Germanium FinFET Based on Rapid Melt Growth; *EDL July 2007 637-639*
- Feng, Y. P.**, see Wang, X. P., *EDL April 2007 258-260*
- Fichou, D.**, see Tiwari, S. P., *EDL Oct. 2007 880-883*
- Fichtenbaum, N.**, see Chu, R., *EDL Sept. 2007 781-783*
- Fiori, G.**, and Iannaccone, G., Simulation of Graphene Nanoribbon Field-Effect Transistors; *EDL Aug. 2007 760-762*
- Fitzgerald, E. A.**, see Yu, H. P., *EDL Dec. 2007 1098-1101*
- Flandre, D.**, see Kilchyska, V., *EDL May 2007 419-421*
- Flandre, D.**, see Rudenko, T., *EDL Sept. 2007 834-836*
- Flandre, D.**, see Simoen, E., *EDL Oct. 2007 919-921*
- Fogel, K. E.**, see Sun, Y., *EDL June 2007 473-475*
- Foisy, M.**, see Winstead, B., *EDL Aug. 2007 719-721*
- Fompeyrine, J.**, see Sun, Y., *EDL June 2007 473-475*
- Forchel, A.**, see Muller, C. R., *EDL Oct. 2007 859-861*
- Forrest, S. R.**, see Sun, Y., *EDL June 2007 473-475*
- Fossum, J. G.**, see Lu, Z., *EDL Feb. 2007 145-147*
- Fossum, J. G.**, Lu, Z., and Trivedi, V. P., New Insights on "Capacitorless" Floating-Body DRAM Cells; *EDL June 2007 513-516*
- Francis, D.**, see Felbinger, J. G., *EDL Nov. 2007 948-950*
- Freeman, G.**, see Kim, D., *EDL June 2007 520-522*
- Freeman, M.**, see Huang, Y.-T., *EDL Sept. 2007 815-817*
- Froment, B.**, see Lousberg, G. P., *EDL Feb. 2007 123-125*
- Fu, Y.-C.**, see Kuo, P.-S., *EDL July 2007 596-598*
- Fu, Y.**, Cheng, X., Chen, Y., Liou, J. J., and Shen, Z. J., A 20-V CMOS-Based Monolithic Bidirectional Power Switch; *EDL Feb. 2007 174-176*
- Fujiwara, A.**, see Nishiguchi, K., *EDL Jan. 2007 48-50*
- Fulde, M.**, see Nirschl, Th., *EDL April 2007 315-315*
- Fulgoni, D. J. F.**, see Nicholas, G., *EDL Sept. 2007 825-827*
- Fung, A.**, see Mei, X. B., *EDL June 2007 470-472*
- Furnemont, A.**, Rosmeulen, M., van der Zanden, K., Van Houdt, J., De Meyer, K., and Maes, H., New Operating Mode Based on Electron/Hole Profile Matching in Nitride-Based Nonvolatile Memories; *EDL April 2007 276-278*
- Fursin, L.**, see Zhang, Y., *EDL May 2007 404-407*
- Furst, J.**, see Tedde, S., *EDL Oct. 2007 893-895*
- Fuyuki, T.**, see Sugawara, Y., *EDL May 2007 395-397*

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- Gaevski, M.**, see Adivarahan, V., *EDL March 2007 192-194*
- Gaier, T.**, see Mei, X. B., *EDL June 2007 470-472*
- Gaitan, M.**, see Marshall, J. C., *EDL Nov. 2007 960-963*
- Ganguly, U.**, see Hou, T.-H., *EDL Feb. 2007 103-106*
- Garcia-Canton, J.**, Merlos, A., and Baldi, A., High-Quality Factor Electrolyte Insulator Silicon Capacitor for Wireless Chemical Sensing; *EDL Jan. 2007 27-29*
- Garcia-Gutierrez, D. I.**, see Shahrjerdi, D., *EDL Sept. 2007 793-796*
- Geng, C.-Q.**, see Li, R., *EDL May 2007 360-362*
- Germann, R.**, see Sun, Y., *EDL June 2007 473-475*
- Ghetti, A.**, see Fantini, P., *EDL Dec. 2007 1114-1116*
- Ghidini, G.**, see Fantini, P., *EDL Dec. 2007 1114-1116*
- Ghyselen, B.**, see Collaert, N., *EDL July 2007 646-648*
- Gillespie, J. K.**, see Jessen, G. H., *EDL May 2007 354-356*
- Gleskova, H.**, see Kattamis, A. Z., *EDL July 2007 606-608*
- Gomez, L.**, Aberg, I., and Hoyt, J. L., Electron Transport in Strained-Silicon Directly on Insulator Ultrathin-Body n-MOSFETs With Body Thickness Ranging From 2 to 25 nm; *EDL April 2007 285-287*
- Gonzalez, M.**, see Brosteaux, D., *EDL July 2007 552-554*
- Goo, J.-S.**, see Yu, C., *EDL Jan. 2007 45-47*
- Gordon, I.**, see Carnel, L., *EDL Oct. 2007 899-901*

- Goto, K.-I.**, see Wang, J.-S., *EDL Nov. 2007 1040-1043*
- Grasby, T. J.**, see Nicholas, G., *EDL Sept. 2007 825-827*
- Griffin, P. B.**, see Wang, Z., *EDL Jan. 2007 14-16*
- Griffin, P. B.**, see Feng, J., *EDL July 2007 637-639*
- Groeseneken, G.**, see Shickova, A., *EDL March 2007 242-244*
- Groeseneken, G. V.**, see Kapila, G., *EDL March 2007 232-234*
- Groeseneken, G.**, see Zhang, J. F., *EDL April 2007 298-300*
- Groeseneken, G.**, see Martens, K., *EDL May 2007 436-439*
- Groeseneken, G.**, see Aoulaiche, M., *EDL July 2007 613-615*
- Guan, X.-K.**, see Yang, C., *EDL July 2007 652-655*
- Guo, P.**, Dong, Y.-W., Ji, X., Lu, Y.-X., and Xu, W., Nonvolatile Multilevel Conductance and Memory Effect in Molecule-Based Devices; *EDL July 2007 572-574*
- Guo, W.**, Nicholas, G., Kaczer, B., Todi, R. M., De Jaeger, B., Claeys, C., Mercha, A., Simoen, E., Cretu, B., Routoure, J.-M., and Carin, R., Low-Frequency Noise Assessment of Silicon Passivated Ge pMOSFETs With TiN/TaN/HfO₂ Gate Stack; *EDL April 2007 288-291*
- Guo, X.**, and Silva, S. R. P., An Efficient Macromodeling Approach for Simulating Carbon-Nanotube Field-Emission Triode Devices in Display Applications; *EDL Aug. 2007 710-712*
- Guo, X.**, and Silva, S. R. P., A Simple and Effective Approach to Improve the Output Linearity of Switched-Current AMOEDL Pixel Circuitry; *EDL Oct. 2007 887-889*
- Guo, Y.**, see Luo, X., *EDL May 2007 422-424*
- Gupta, J. A.**, see Lew, K. L., *EDL Dec. 2007 1083-1085*

H

- Hadjisavvas, G.**, Tsetseris, L., and Pantelides, S. T., The Origin of Electron Mobility Enhancement in Strained MOSFETs; *EDL Nov. 2007 1018-1020*
- Han, G.**, see Chae, Y., *EDL June 2007 495-498*
- Han, J.-W.**, Lee, J., Park, D., and Choi, Y.-K., Body Thickness Dependence of Impact Ionization in a Multiple-Gate FinFET; *EDL July 2007 625-627*
- Han, M.**, see Lim, B. O., *EDL July 2007 546-548*
- Haney, S.**, see Agarwal, A., *EDL July 2007 587-589*
- Hao, Y.**, see Xu, C., *EDL Nov. 2007 942-944*
- Harris, H. R.**, see Joshi, S., *EDL April 2007 308-311*
- Harris, R.**, see Oh, J., *EDL Nov. 2007 1044-1046*
- Haruehanroengra, S.**, and Wang, W., Analyzing Conductance of Mixed Carbon-Nanotube Bundles for Interconnect Applications; *EDL Aug. 2007 756-759*
- Hatayama, T.**, see Sugawara, Y., *EDL May 2007 395-397*
- Hatzopoulos, A. T.**, Arpatzani, N., Tassis, D. H., Dimitriadis, C. A., Templier, F., Oudwan, M., and Kamarinos, G., Stability of Amorphous-Silicon and Nanocrystalline Silicon Thin-Film Transistors Under DC and AC Stress; *EDL Sept. 2007 803-805*
- Hayafuji, T.**, see Sasa, S., *EDL July 2007 543-545*
- Hayashi, R.**, see Ofuji, M., *EDL April 2007 273-275*
- Hayashi, T.**, see Kawahara, T., *EDL Oct. 2007 868-870*
- Heh, D.**, see Joshi, S., *EDL April 2007 308-311*
- Heh, D.**, Choi, R., and Bersuker, G., Comparison of On-The-Fly, DC I_d-V_g , and Single-Pulse Methods for Evaluating Threshold Voltage Instability in High- κ nMOSFETs; *EDL March 2007 245-247*
- Heh, D.**, Young, C. D., Choi, R., and Bersuker, G., Extraction of the Threshold-Voltage Shift by the Single-Pulse Technique; *EDL Aug. 2007 734-736*
- Hekmatshoar, B.**, see Kattamis, A. Z., *EDL July 2007 606-608*
- Hekmatshoar, B.**, see Cherenack, K. H., *EDL Nov. 2007 1004-1006*
- Hennessy, J.**, see Ritenour, A., *EDL Aug. 2007 746-749*
- Henry, H. G.**, see Jessen, G. H., *EDL May 2007 354-356*
- Henseler, D.**, see Tedde, S., *EDL Oct. 2007 893-895*
- Henson, K.**, see Severi, S., *EDL March 2007 198-200*
- Herman, D. L.**, see Marshall, J. C., *EDL Nov. 2007 960-963*
- Heyns, M. M.**, see Aoulaiche, M., *EDL July 2007 613-615*
- Heyns, M. M.**, see Nicholas, G., *EDL Sept. 2007 825-827*
- Higashi, M.**, see Kawahara, T., *EDL Oct. 2007 868-870*
- Hijzen, E.**, see Choi, L. J., *EDL April 2007 270-272*
- Hill, R. J. W.**, Moran, D. A. J., Li, X., Zhou, H., Macintyre, D., Thoms, S., Asenov, A., Zurcher, P., Rajagopalan, K., Abrokwhah, J., Droopad, R., Passlack, M., and Thayne, I. G., Enhancement-Mode GaAs MOSFETs With an In_{0.3}Ga_{0.7}As Channel, a Mobility of Over 5000 cm²/V·s, and Transconductance of Over 475 $\mu\text{S}/\mu\text{m}$; *EDL Dec. 2007 1080-1082*
- Hilton, K. P.**, see Kuball, M., *EDL Feb. 2007 86-89*
- Hiramoto, T.**, see Ohtou, T., *EDL Aug. 2007 740-742*

- Ho, C.-L.**, see Wu, M.-C., *EDL Sept. 2007 797-799*
- Hoang, T.**, see van der Steen, J.-L. P. J., *EDL Sept. 2007 821-824*
- Hoang, T.**, LeMinh, P., Holleman, J., and Schmitz, J., Strong Efficiency Improvement of SOI-EDLs Through Carrier Confinement; *EDL May 2007 383-385*
- Hoe, K. M.**, see Tan, K.-M., *EDL Oct. 2007 905-908*
- Hoffmann, T.**, see Chang, S. Z., *EDL July 2007 634-636*
- Hoffing, S.**, see Muller, C. R., *EDL Oct. 2007 859-861*
- Hohkawa, K.**, see Shigekawa, N., *EDL Feb. 2007 90-92*
- Holland, M. C.**, see Khalid, A., *EDL Oct. 2007 849-851*
- Holleman, J.**, see Hoang, T., *EDL May 2007 383-385*
- Holleman, J.**, see van der Steen, J.-L. P. J., *EDL Sept. 2007 821-824*
- Honda, K.**, see Kawahara, T., *EDL Oct. 2007 868-870*
- Hong, B. H.**, see Cho, K. H., *EDL Dec. 2007 1129-1131*
- Hong, Y.-K.**, see Lee, K.-S., *EDL Aug. 2007 672-675*
- Hopfner, P.**, see Muller, C. R., *EDL Oct. 2007 859-861*
- Horng, S.-F.**, see Liao, Y.-Y., *EDL Sept. 2007 828-830*
- Hosono, H.**, see Ofuji, M., *EDL April 2007 273-275*
- Hou, T.-H.**, Ganguly, U., and Kan, E. C., Fermi-Level Pinning in Nanocrystal Memories; *EDL Feb. 2007 103-106*
- Hou, Y. T.**, see Yen, F. Y., *EDL March 2007 201-203*
- Hou, Y. T.**, see Wu, C. H., *EDL April 2007 292-294*
- Houssa, M.**, see Aoulaiche, M., *EDL July 2007 613-615*
- Hoyt, J. L.**, see Gomez, L., *EDL April 2007 285-287*
- Hsia, H.**, see Cheng, C. Y., *EDL May 2007 408-411*
- Hsiao, C. N.**, see Chiang, K. C., *EDL March 2007 235-237*
- Hsiao, C. N.**, see Chiang, K. C., *EDL Aug. 2007 694-696*
- Hsiao, C. N.**, see Cheng, C. H., *EDL Dec. 2007 1095-1097*
- Hsiao, R.-S.**, see Su, K.-H., *EDL Feb. 2007 96-99*
- Hsiao, Y.-W.**, and Ker, M.-D., Bond Pad Design With Low Capacitance in CMOS Technology for RF Applications; *EDL Jan. 2007 68-70*
- Hsieh, C.-I.**, see Pan, T.-M., *EDL Nov. 2007 954-956*
- Hsieh, C.-Y.**, see Chen, M.-J., *EDL Feb. 2007 177-179*
- Hsieh, C.-Y.**, and Chen, M.-J., Measurement of Channel Stress Using Gate Direct Tunneling Current in Uniaxially Stressed nMOSFETs; *EDL Sept. 2007 818-820*
- Hsieh, I. J.**, see Yang, H. J., *EDL Oct. 2007 913-915*
- Hsieh, J.**, see Lai, S., *EDL July 2007 643-645*
- Hsieh, J. C.**, see Cheng, C. Y., *EDL May 2007 408-411*
- Hsieh, J.-Y.**, see Hsu, T.-H., *EDL May 2007 443-445*
- Hsieh, K.**, see Lai, S., *EDL July 2007 643-645*
- Hsieh, K.-Y.**, see Hsu, T.-H., *EDL May 2007 443-445*
- Hsieh, M. F.**, see Chang, K. M., *EDL Jan. 2007 39-41*
- Hsieh, R.-J.**, see Chen, S.-H., *EDL Aug. 2007 679-681*
- Hsieh, S.-I.**, see Chen, H.-T., *EDL June 2007 499-501*
- Hsieh, T.-M.**, see Wu, W.-C., *EDL March 2007 214-216*
- Hsu, C.-H.**, see Lin, C.-T., *EDL Feb. 2007 111-113*
- Hsu, C.-H.**, see Lin, C.-T., *EDL May 2007 376-378*
- Hsu, C.-H.**, see Huang, Y.-T., *EDL Sept. 2007 815-817*
- Hsu, C.-H.**, see Lin, C.-T., *EDL Sept. 2007 831-833*
- Hsu, H. T.**, see Chu, L. H., *EDL Feb. 2007 82-85*
- Hsu, H.-M.**, and Tseng, C.-W., Design of On-Chip Transformer With Various Coil Widths to Achieve Minimal Metal Resistance; *EDL Nov. 2007 1029-1032*
- Hsu, H.-T.**, see Chang, C. Y., *EDL Oct. 2007 856-858*
- Hsu, H.**, Chang, I. Y., and Lee, J. Y., Metal-Oxide-High- κ Dielectric-Oxide-Semiconductor (MOHOS) Capacitors and Field-Effect Transistors for Memory Applications; *EDL Nov. 2007 964-966*
- Hsu, K. Y.-J.**, see Lai, K.-S., *EDL Sept. 2007 800-802*
- Hsu, P. F.**, see Yen, F. Y., *EDL March 2007 201-203*
- Hsu, S. L.**, see Chen, J. F., *EDL Nov. 2007 1033-1035*
- Hsu, T.-H.**, Lue, H. Y., King, Y.-C., Hsieh, J.-Y., Lai, E.-K., Hsieh, K.-Y., Liu, R., and Lu, C.-Y., A High-Performance Body-Tied FinFET Bandgap Engineered SONOS (BE-SONOS) for NAND-Type Flash Memory; *EDL May 2007 443-445*
- Hsu, W.-C.**, see Su, K.-H., *EDL Feb. 2007 96-99*
- Hu, C.**, see Lin, C.-Y., *EDL May 2007 366-368*
- Hu, C.-M.**, Wu, Y. C. S., and Lin, C.-C., Improving the Electrical Properties of NILC Poly-Si Films Using a Gettering Substrate; *EDL Nov. 2007 1000-1003*
- Hu, C.-W.**, see Lee, F.-M., *EDL Feb. 2007 120-122*
- Huang, F.**, Lu, J., Zhu, Y., Jiang, N., Wang, X., and Chi, Y., Effect of Substrate Parasitic Inductance on Silicon-Based Transmission Lines and On-Chip Inductors; *EDL Nov. 2007 1025-1028*
- Huang, G.-W.**, see Chang, C. Y., *EDL Oct. 2007 856-858*
- Huang, H.-W.**, see Lu, T.-C., *EDL Oct. 2007 884-886*
- Huang, J.**, see Yu, X., *EDL May 2007 373-375*
- Huang, J.-C.**, see Shiu, J.-Y., *EDL June 2007 476-478*
- Huang, J.-C.**, see Lai, K.-S., *EDL Sept. 2007 800-802*
- Huang, K.**, see Li, R., *EDL May 2007 360-362*
- Huang, K.-F.**, see Lee, F.-M., *EDL Feb. 2007 120-122*
- Huang, P.-W.**, see Chen, M.-J., *EDL Feb. 2007 177-179*
- Huang, R.**, see Li, Y., *EDL July 2007 622-624*
- Huang, R.**, see Li, C., *EDL Aug. 2007 763-766*
- Huang, S.-F.**, see Zhu, H., *EDL Feb. 2007 168-170*
- Huang, T.-Y.**, see Yang, M.-J., *EDL Oct. 2007 902-904*
- Huang, T.-Y.**, see Pan, T.-M., *EDL Nov. 2007 954-956*
- Huang, T.-Y.**, see Chen, J. F., *EDL Nov. 2007 1033-1035*
- Huang, W. L.**, see Yang, H. J., *EDL Oct. 2007 913-915*
- Huang, Y.-H.**, see Wu, M.-C., *EDL Sept. 2007 797-799*
- Huang, Y.-T.**, see Lin, C.-T., *EDL Sept. 2007 831-833*
- Huang, Y.-T.**, Pinto, A., Lin, C.-T., Hsu, C.-H., Ramin, M., Seacrist, M., Ries, M., Matthews, K., Nguyen, B., Freeman, M., Wilks, B., Stager, C., Johnson, C., Denning, L., Bennett, J., Joshi, S., Chiang, S., Cheng, L.-W., Lee, T.-H., Ma, M., Cheng, O., and Wise, R., PMOSFET Reliability Study for Direct Silicon Bond (DSB) Hybrid Orientation Technology (HOT); *EDL Sept. 2007 815-817*
- Hudait, M. K.**, see Datta, S., *EDL Aug. 2007 685-687*
- Huetting, R. J. E.**, see van der Steen, J.-L. P. J., *EDL Sept. 2007 821-824*
- Hung, B. F.**, see Wu, C. H., *EDL April 2007 292-294*
- Hung, C. L.**, see Yen, F. Y., *EDL March 2007 201-203*
- Hur, S.-H.**, see Park, M., *EDL Aug. 2007 750-752*
- Hurkx, G. A. M.**, and Agarwal, P., A Quantum-Mechanical View on the Capacitance of a Silicon p-n Junction; *EDL April 2007 312-314*
- Hwang, G.-W.**, see Lin, H.-T., *EDL Nov. 2007 951-953*
- Hwang, H.**, see Chang, M., *EDL Jan. 2007 21-23*
- Hwang, H. L.**, see Chiang, K. C., *EDL March 2007 235-237*
- Hwang, H. L.**, see Chiang, K. C., *EDL Aug. 2007 694-696*
- Hwang, J. D.**, see Chen, Y. H., *EDL Dec. 2007 1111-1113*
- Hwang, S. W.**, see Cho, K. H., *EDL Dec. 2007 1129-1131*
- Hwang, W. S.**, see Lim, A. E.-J., *EDL June 2007 482-485*
- Hyun, J. W.**, see Padilla, A., *EDL June 2007 502-505*

I

- Iacoponi, J.**, see Pan, J., *EDL Aug. 2007 691-693*
- Iannaccone, G.**, see Fiori, G., *EDL Aug. 2007 760-762*
- Ielmini, D.**, see Mantegazza, D., *EDL Oct. 2007 865-867*
- Inokawa, H.**, see Nishiguchi, K., *EDL Jan. 2007 48-50*
- Inoue, M.**, see Sasa, S., *EDL July 2007 543-545*
- Inoue, M.**, see Kawahara, T., *EDL Oct. 2007 868-870*
- Ishii, K.**, see Endo, K., *EDL May 2007 452-454*
- Ishii, K.**, see Liu, Y., *EDL June 2007 517-519*
- Ishii, K.**, see Endo, K., *EDL Dec. 2007 1123-1125*
- Ishikawa, Y.**, see Endo, K., *EDL May 2007 452-454*
- Ishikawa, Y.**, see Liu, Y., *EDL June 2007 517-519*
- Ishikawa, Y.**, see Endo, K., *EDL Dec. 2007 1123-1125*
- Ito, M.**, see Mizutani, T., *EDL July 2007 549-551*
- Iwami, M.**, see Kambayashi, H., *EDL Dec. 2007 1077-1079*

J

- Jackson, T. N.**, see Park, S. K., *EDL Oct. 2007 877-879*
- Jaeger, N. A. F.**, see Ristic, S., *EDL Jan. 2007 30-32*
- Jamei, M.**, Karbassian, F., Mohajerzadeh, S., Abdi, Y., Robertson, M. D., and Yuill, S., The Preparation of Nanocrystalline Silicon by Plasma-Enhanced Hydrogenation for the Fabrication of Light-Emitting Diodes; *EDL March 2007 207-210*
- Jammy, R.**, see Joshi, S., *EDL April 2007 308-311*
- Jammy, R.**, see Oh, J., *EDL Nov. 2007 1044-1046*
- Jang, J.-H.**, see Kim, T.-W., *EDL Dec. 2007 1086-1088*
- Jang, S. M.**, see Yen, F. Y., *EDL March 2007 201-203*
- Jarndal, A.**, see Srinidhi, E. R., *EDL May 2007 343-345*
- Jayanarayanan, S. K.**, see Yu, C., *EDL Jan. 2007 45-47*

- Jeong, J. K.**, Jin, D. U., Shin, H. S., Lee, H. J., Kim, M., Ahn, T. K., Lee, J., Mo, Y. G., and Chung, H. K., Flexible Full-Color AMOEDL on Ultrathin Metal Foil; *EDL May 2007 389-391*
- Jeong, Y. H.**, Lim, J. B., Nahm, S., Sun, H.-J., and Lee, H. J., High-Performance Metal-Insulator-Metal Capacitors Using Amorphous BaSm₂Ti₄O₁₂ Thin Film; *EDL Jan. 2007 17-20*
- Jeong, Y.-H.**, see Lee, K.-S., *EDL Aug. 2007 672-675*
- Jessen, G. H.**, Gillespie, J. K., Via, G. D., Crespo, A., Langley, D., Aumer, M. E., Ward, C. S., Henry, H. G., Thomson, D. B., and Partlow, D. P., RF Power Measurements of InAlN/GaN Unstrained HEMTs on SiC Substrates at 10 GHz; *EDL May 2007 354-356*
- Jhou, K. Y.**, see Chiang, K. C., *EDL Aug. 2007 694-696*
- Ji, T.**, Jung, S., and Varadan, V. K., Field-Controllable Flexible Strain Sensors Using Pentacene Semiconductors; *EDL Dec. 2007 1105-1107*
- Ji, X.**, see Guo, P., *EDL July 2007 572-574*
- Jiang, J. C.**, see Yen, F. Y., *EDL March 2007 201-203*
- Jiang, N.**, see Huang, F., *EDL Nov. 2007 1025-1028*
- Jiang, Y.**, Loh, W. Y., Chan, D. S. H., Xiong, Y. Z., Ren, C., Lim, Y. F., Lo, G. Q., and Kwong, D. L., Flicker Noise and Its Degradation Characteristics Under Electrical Stress in MOSFETs With Thin Strained-Si/SiGe Dual-Quantum Well; *EDL July 2007 603-605*
- Jin, D. U.**, see Jeong, J. K., *EDL May 2007 389-391*
- Jin, Y.**, see Yen, F. Y., *EDL March 2007 201-203*
- Jin, Y.**, see Wu, C. H., *EDL April 2007 292-294*
- Jindal, R. P.**, What is in a Page Charge?; *EDL Jan. 2007 1-1*
- Jindal, R. P.**, A New Look for IEEE Transactions on Electron Devices Briefs; *EDL June 2007 469-469*
- Jindal, R. P.**, Confidentiality of the Review Process; *EDL Dec. 2007 1076-1076*
- Jo, M.**, see Chang, M., *EDL Jan. 2007 21-23*
- Johnson, C.**, see Huang, Y.-T., *EDL Sept. 2007 815-817*
- Joo, Y.**, see Park, D., *EDL Oct. 2007 890-892*
- Joshi, S.**, see Huang, Y.-T., *EDL Sept. 2007 815-817*
- Joshi, S.**, Krug, C., Heh, D., Na, H. J., Harris, H. R., Oh, J. W., Kirsch, P. D., Majhi, P., Lee, B. H., Tseng, H.-H., Jammy, R., Lee, J. C., and Banerjee, S. K., Improved Ge Surface Passivation With Ultrathin SiO_x Enabling High-Mobility Surface Channel pMOSFETs Featuring a HfSiO/WN Gate Stack; *EDL April 2007 308-311*
- Ju, B. K.**, see Cho, W.-S., *EDL May 2007 386-388*
- Ju, B.-K.**, see Shin, K.-S., *EDL July 2007 581-583*
- Jung, H.-A.-R.**, Park, K.-H., and Lee, J.-H., n⁺/p⁺ Gate Bulk FinFETs With Locally Separated Channel Structure for Sub-50-nm DRAM Cell Transistors; *EDL Dec. 2007 1126-1128*
- Jung, J.**, see Moon, C.-R., *EDL Feb. 2007 114-116*
- Jung, K.-D.**, Lee, C. A., Park, D.-W., Park, B.-G., Shin, H., and Lee, J. D., Admittance Measurements on OFET Channel and Its Modeling With R-C Network; *EDL March 2007 204-206*
- Jung, S.**, see Ji, T., *EDL Dec. 2007 1105-1107*
- Jung, Y. C.**, see Cho, K. H., *EDL Dec. 2007 1129-1131*
- Jurczak, M.**, see Lousberg, G. P., *EDL Feb. 2007 123-125*
- Jurczak, M.**, see Shickova, A., *EDL March 2007 242-244*
- Jurczak, M.**, see Masahara, M., *EDL March 2007 217-219*
- Jurczak, M.**, see Kilchytska, V., *EDL May 2007 419-421*
- Jurczak, M.**, see Collaert, N., *EDL July 2007 646-648*
- Jurczak, M.**, see Rudenko, T., *EDL Sept. 2007 834-836*
- Jurczak, M.**, see Veloso, A., *EDL Nov. 2007 980-983*
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- Kaczer, B.**, see Kapila, G., *EDL March 2007 232-234*
- Kaczer, B.**, see Shickova, A., *EDL March 2007 242-244*
- Kaczer, B.**, see Guo, W., *EDL April 2007 288-291*
- Kaczer, B.**, see Martens, K., *EDL May 2007 436-439*
- Kaji, N.**, see Ofuji, M., *EDL April 2007 273-275*
- Kakiuchi, Y.**, see Saito, W., *EDL Aug. 2007 676-678*
- Kamarinos, G.**, see Hatzopoulos, A. T., *EDL Sept. 2007 803-805*
- Kambayashi, H.**, Niiyama, Y., Ootomo, S., Nomura, T., Iwami, M., Satoh, Y., Kato, S., and Yoshida, S., Normally Off n-Channel GaN MOSFETs on Si Substrates Using an SAG Technique and Ion Implantation; *EDL Dec. 2007 1077-1079*
- Kamiya, T.**, see Ofuji, M., *EDL April 2007 273-275*
- Kan, E. C.**, see Hou, T.-H., *EDL Feb. 2007 103-106*
- Kang, C. Y.**, see Akbar, M. S., *EDL Feb. 2007 132-134*
- Kang, C. Y.**, see Oh, J., *EDL Nov. 2007 1044-1046*
- Kang, E. T.**, see Song, Y., *EDL Feb. 2007 107-110*
- Kang, I. M.**, Lee, J. D., and Shin, H., Extraction of π -Type Substrate Resistance Based on Three-Port Measurement and the Model Verification up to 110 GHz; *EDL May 2007 425-427*
- Kang, J. Y.**, see Shin, K.-S., *EDL July 2007 581-583*
- Kang, S. J.**, see Pimparkar, N., *EDL July 2007 593-595*
- Kao, C.-C.**, see Lu, T.-C., *EDL Oct. 2007 884-886*
- Kao, K.-H.**, see Ma, M.-W., *EDL March 2007 238-241*
- Kao, M.-J.**, see Chao, D.-S., *EDL Oct. 2007 871-873*
- Kao, T.-T.**, see Lu, T.-C., *EDL Oct. 2007 884-886*
- Kapila, G.**, Kaczer, B., Nackaerts, A., Collaert, N., and Groeseneken, G. V., Direct Measurement of Top and Sidewall Interface Trap Density in SOI FinFETs; *EDL March 2007 232-234*
- Karbasian, F.**, see Jamei, M., *EDL March 2007 207-210*
- Karim, K.**, see Sanaie, G., *EDL Jan. 2007 33-35*
- Karmalkar, S.**, see Balaji, S., *EDL March 2007 229-231*
- Kato, S.**, see Kambayashi, H., *EDL Dec. 2007 1077-1079*
- Kattamis, A. Z.**, see Cherenack, K. H., *EDL Nov. 2007 1004-1006*
- Kattamis, A. Z.**, Cherenack, K. H., Hekmatshoar, B., Cheng, I.-C., Gleskova, H., Sturm, J. C., and Wagner, S., Effect of SiN_x Gate Dielectric Deposition Power and Temperature on a-Si:H TFT Stability; *EDL July 2007 606-608*
- Kauerauf, T.**, see Yu, H. Y., *EDL Nov. 2007 957-959*
- Kawahara, T.**, Nishida, Y., Sakashita, S., Mizutani, M., Inoue, M., Yamanari, S., Higashi, M., Hayashi, T., Murata, N., Honda, K., Yugami, J., Yoshimura, H., and Yoneda, M., Reduction of Threshold Voltage by Diffusion Control Technique in p-MISFETs Using Poly-Si/TiN/HfSiON Gate Stacks; *EDL Oct. 2007 868-870*
- Kawamura, T.**, see Zhu, H., *EDL Feb. 2007 168-170*
- Kawasaki, M.**, see Sasa, S., *EDL July 2007 543-545*
- Keller, S.**, see Chu, R., *EDL Sept. 2007 781-783*
- Kellsall, R. W.**, see Sadi, T., *EDL Sept. 2007 787-789*
- Ker, M.-D.**, see Hsiao, Y.-W., *EDL Jan. 2007 68-70*
- Kerner, C.**, see Chang, S. Z., *EDL July 2007 634-636*
- Khalid, A.**, Pilgrim, N. J., Dunn, G. M., Holland, M. C., Stanley, C. R., Thayne, I. G., and Cumming, D. R. S., A Planar Gunn Diode Operating Above 100 GHz; *EDL Oct. 2007 849-851*
- Khan, A.**, see Tipirneni, N., *EDL Sept. 2007 784-786*
- Khan, M. A.**, see Koudymov, A., *EDL Jan. 2007 5-7*
- Khan, M. A.**, see Adivarahan, V., *EDL March 2007 192-194*
- Khramtsov, A.**, see Stoppel, A., *EDL Jan. 2007 357-359*
- Kiewra, E. W.**, see Sun, Y., *EDL June 2007 473-475*
- Kilchytska, V.**, see Rudenko, T., *EDL Sept. 2007 834-836*
- Kilchytska, V.**, Pailioncy, G., EDLerer, D., Raskin, J.-P., Collaert, N., Jurczak, M., and Flandre, D., Frequency Variation of the Small-Signal Output Conductance of Decanometer MOSFETs Due to Substrate Crosstalk; *EDL May 2007 419-421*
- Kim, B.**, see Chae, Y., *EDL June 2007 495-498*
- Kim, D.-H.**, see Kim, T.-W., *EDL Dec. 2007 1086-1088*
- Kim, D.-J.**, see Lee, J.-W., *EDL May 2007 379-382*
- Kim, D.-W.**, see Kim, H., *EDL Jan. 2007 42-44*
- Kim, D.-W.**, see Cho, K. H., *EDL Dec. 2007 1129-1131*
- Kim, D.**, Kim, J., Plouchart, J.-O., Cho, C., Trzcinski, R., Kumar, M., and Norris, C., Symmetric Vertical Parallel Plate Capacitors for On-Chip RF Circuits in 65-nm SOI Technology; *EDL July 2007 616-618*
- Kim, D.**, Kim, J., Plouchart, J.-O., Cho, C., Trzcinski, R., Lee, S., Kumar, M., Norris, C., Rieh, J.-S., Freeman, G., and Ahlgren, D., Manufacturable Parasitic-Aware Circuit-Level FETs in 65-nm SOI CMOS Technology; *EDL June 2007 520-522*
- Kim, H. S.**, see Zhang, M. H., *EDL March 2007 195-197*
- Kim, H.-S.**, see Akbar, M. S., *EDL Feb. 2007 132-134*
- Kim, H.**, Kim, D.-W., Cho, K., and Kim, S., HgTe Nanocrystal-Based Thin-Film Transistors Fabricated on Glass Substrates; *EDL Jan. 2007 42-44*
- Kim, J.**, see Kim, D., *EDL June 2007 520-522*
- Kim, J.-K.**, see Cho, W.-S., *EDL May 2007 386-388*
- Kim, J.-K.**, see Lee, J.-W., *EDL May 2007 379-382*
- Kim, J.-S.**, and Lee, H.-J., Effect of Load Distribution on the Voltage Drop and the Luminance Variation in an AC-PDP; *EDL Oct. 2007 896-898*
- Kim, J.**, see Kim, D., *EDL July 2007 616-618*
- Kim, K.**, see Moon, C.-R., *EDL Feb. 2007 114-116*
- Kim, K.**, see Park, M., *EDL Aug. 2007 750-752*
- Kim, L.**, and Shin, M. W., Implementation of Side Effects in Thermal Characterization of RGB Full-Color EDLs; *EDL July 2007 578-580*

- Kim, M.**, see Jeong, J. K., *EDL May 2007 389-391*
- Kim, M.**, Choi, S., Ree, M., and Kim, O., Current-Dependent Switching Characteristics of PI-Diphenyl Carbamyl Films; *EDL Nov. 2007 967-969*
- Kim, O.**, see Kim, M., *EDL Nov. 2007 967-969*
- Kim, S.**, see Kim, H., *EDL Jan. 2007 42-44*
- Kim, S. C.**, see Lim, B. O., *EDL July 2007 546-548*
- Kim, S.**, and Wong, H.-S.P., Analysis of Temperature in Phase Change Memory Scaling; *EDL Aug. 2007 697-699*
- Kim, S.**, Xue, L., and Tiwari, S., Low-Temperature Polymer-Based Three-Dimensional Silicon Integration; *EDL Aug. 2007 706-709*
- Kim, T. H.**, Song, C. K., Park, J. S., and Suh, M. C., Constant Bias Stress Effects on Threshold Voltage of Pentacene Thin-Film Transistors Employing Polyvinylphenol Gate Dielectric; *EDL Oct. 2007 874-876*
- Kim, T.-S.**, see Shin, K.-S., *EDL July 2007 581-583*
- Kim, T.-W.**, Kim, D.-H., Park, S. D., Yeom, G. Y., Lim, B. O., Rhee, J.-K., Jang, J.-H., and Song, J.-I., Effect of a Two-Step Recess Process Using Atomic Layer Etching on the Performance of $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ p-HEMTs; *EDL Dec. 2007 1086-1088*
- Kim, Y. M.**, see Mei, X. B., *EDL June 2007 470-472*
- Kim, Y.-S.**, see Na, K.-Y., *EDL Feb. 2007 151-153*
- Kim, Y.-S.**, see Lee, K.-S., *EDL Aug. 2007 672-675*
- Kim, Y.-S.**, see Na, K.-Y., *EDL Nov. 2007 1047-1049*
- King Liu, T.-J.**, see Padilla, A., *EDL June 2007 502-505*
- King Liu, T.-J.**, see Lai, J., *EDL Aug. 2007 725-727*
- King, Y.-C.**, see Hsu, T.-H., *EDL May 2007 443-445*
- King, Y.-C.**, see Chen, H.-T., *EDL June 2007 499-501*
- King, Y.-C.**, see Lai, H.-C., *EDL Sept. 2007 837-839*
- Kirsch, P. D.**, see Joshi, S., *EDL April 2007 308-311*
- Kishimoto, S.**, see Mizutani, T., *EDL July 2007 549-551*
- Knoch, J.**, see Zhang, M., *EDL March 2007 223-225*
- Ko, S.-C.**, see Lee, F.-M., *EDL Feb. 2007 120-122*
- Kocabas, C.**, see Pimparkar, N., *EDL July 2007 593-595*
- Koester, S. J.**, see Sun, Y., *EDL June 2007 473-475*
- Koike, H.**, see Endo, K., *EDL May 2007 452-454*
- Koike, K.**, see Sasa, S., *EDL July 2007 543-545*
- Kompa, G.**, see Srinidhi, E. R., *EDL May 2007 343-345*
- Kong, W.-R.**, see Li, R., *EDL May 2007 360-362*
- Koskenvuori, M.**, and Tittonen, I., Improvement of the Conversion Performance of a Resonating Multimode Microelectromechanical Mixer-Filter Through Parametric Amplification; *EDL Nov. 2007 970-972*
- Koudymov, A.**, see Adivarahan, V., *EDL March 2007 192-194*
- Koudymov, A.**, Shur, M. S., and Simin, G., Compact Model of Current Collapse in Heterostructure Field-Effect Transistors; *EDL May 2007 332-335*
- Koudymov, A.**, Wang, C. X., Adivarahan, V., Yang, J., Simin, G., and Khan, M. A., Power Stability of AlGaIn/GaN HFETs at 20 W/mm in the Pinched-Off Operation Mode; *EDL Jan. 2007 5-7*
- Kranti, A.**, and Armstrong, G. A., Source/Drain Extension Region Engineering in FinFETs for Low-Voltage Analog Applications; *EDL Feb. 2007 139-141*
- Krishnan, S. A.**, see Akbar, M. S., *EDL Feb. 2007 132-134*
- Krug, C.**, see Joshi, S., *EDL April 2007 308-311*
- Kuball, M.**, Riedel, G. J., Pomeroy, J. W., Sarua, A., Uren, M. J., Martin, T., Hilton, K. P., Maclean, J. O., and Wallis, D. J., Time-Resolved Temperature Measurement of AlGaIn/GaN Electronic Devices Using Micro-Raman Spectroscopy; *EDL Feb. 2007 86-89*
- Kubicek, S.**, see Yu, H. Y., *EDL July 2007 656-658*
- Kubicek, S.**, see Singanamalla, R., *EDL Dec. 2007 1089-1091*
- Kubota, T.**, see Ohashi, T., *EDL July 2007 562-564*
- Kumakura, K.**, see Shiu, J.-Y., *EDL June 2007 476-478*
- Kumar, A.**, see Lin, H., *EDL June 2007 506-508*
- Kumar, A.**, see Lin, H., *EDL June 2007 506-508*
- Kumar, M.**, see Kim, D., *EDL June 2007 520-522*
- Kumar, M.**, see Kim, D., *EDL July 2007 616-618*
- Kumar, P. B.**, see Datta, A., *EDL May 2007 446-448*
- Kumar, S.**, see Pimparkar, N., *EDL Feb. 2007 157-160*
- Kumomi, H.**, see Ofuji, M., *EDL April 2007 273-275*
- Kung, C. Y.**, see Chen, Y. H., *EDL Dec. 2007 1111-1113*
- Kunnen, E.**, see Masahara, M., *EDL March 2007 217-219*
- Kunnen, E.**, see Choi, L. J., *EDL April 2007 270-272*
- Kuo, C.-I.**, see Chang, C. Y., *EDL Oct. 2007 856-858*
- Kuo, H.-C.**, see Lu, T.-C., *EDL Oct. 2007 884-886*
- Kuo, J. J.-Y.**, see Su, P., *EDL July 2007 649-651*
- Kuo, P.-S.**, see Pan, T.-M., *EDL Nov. 2007 954-956*
- Kuo, P.-S.**, Lin, C.-H., Peng, C.-Y., Fu, Y.-C., and Liu, C. W., Transport Mechanism of SiGe Dot MOS Tunneling Diodes; *EDL July 2007 596-598*
- Kurabayashi, K.**, see Chow, L. L. W., *EDL June 2007 479-481*
- Kurz, H.**, see Lemme, M. C., *EDL April 2007 282-284*
- Kwon, D.-W.**, see Moon, C.-R., *EDL Feb. 2007 114-116*
- Kwong, D. L.**, see Liu, J., *EDL Jan. 2007 11-13*
- Kwong, D. L.**, see Jiang, Y., *EDL July 2007 603-605*
- Kwong, D. L.**, see Rustagi, S. C., *EDL Nov. 2007 1021-1024*
- Kwong, D. L.**, see Loh, W. Y., *EDL Nov. 2007 984-986*
- Kwong, D.-L.**, see Fang, W. W., *EDL March 2007 211-213*
- Kwong, D.-L.**, see Wang, X. P., *EDL April 2007 258-260*
- Kwong, D.-L.**, see Bai, W., *EDL May 2007 369-372*
- Kwong, D.-L.**, see Lim, A. E.-J., *EDL June 2007 482-485*
- Kwong, D.-L.**, see Singh, N., *EDL July 2007 558-561*
- Kwong, D.-L.**, see Rustagi, S. C., *EDL Oct. 2007 909-912*

L

- Lacaita, A. L.**, see Compagnoni, C. M., *EDL July 2007 628-630*
- Lacaita, A. L.**, see Mantegazza, D., *EDL Oct. 2007 865-867*
- Lai, C.-M.**, see Lin, C.-T., *EDL Feb. 2007 111-113*
- Lai, C.-M.**, see Lin, C.-T., *EDL May 2007 376-378*
- Lai, C.-M.**, Fang, Y.-K., Yeh, W.-K., Lin, C. T., and Chou, T. H., The Investigation of Post-Annealing-Induced Defects Behavior on 90-nm In Halo nMOSFETs With Low-Frequency Noise and Charge-Pumping Measuring; *EDL Feb. 2007 142-144*
- Lai, C.-S.**, see Wu, W.-C., *EDL March 2007 214-216*
- Lai, E.**, see Lai, S., *EDL July 2007 643-645*
- Lai, E.-K.**, see Hsu, T.-H., *EDL May 2007 443-445*
- Lai, H.-C.**, Cheng, K.-Y., King, Y.-C., and Lin, C.-J., A 0.26- μm^2 U-Shaped Nitride-Based Programming Cell on Pure 90-nm CMOS Technology; *EDL Sept. 2007 837-839*
- Lai, J.**, and King Liu, T.-J., Defect Passivation by Selenium-Ion Implantation for Poly-Si Thin Film Transistors; *EDL Aug. 2007 725-727*
- Lai, K.-S.**, Huang, J.-C., and Hsu, K. Y.-J., High-Responsivity Photodetector in Standard SiGe BiCMOS Technology; *EDL Sept. 2007 800-802*
- Lai, R.**, see Mei, X. B., *EDL June 2007 470-472*
- Lai, S.**, Lue, H., Hsieh, J., Yang, M., Chiou, Y., Wu, C., Wu, T., Luo, G., Chien, C., Lai, E., Hsieh, K., Liu, R., and Lu, C., Study of the Erase Mechanism of MANOS (Metal/Al₂O₃/SiN/SiO₂/Si) Device; *EDL July 2007 643-645*
- Lange, M.**, see Mei, X. B., *EDL June 2007 470-472*
- Langley, D.**, see Jessen, G. H., *EDL May 2007 354-356*
- Larriue, G.**, see Cornu-Frueux, F., *EDL June 2007 523-526*
- Lau, K. M.**, see Song, D., *EDL March 2007 189-191*
- Lau, K. M.**, see Cai, Y., *EDL May 2007 328-331*
- Lau, K. M.**, see Zhou, W., *EDL July 2007 539-542*
- Lauwers, A.**, see Lousberg, G. P., *EDL Feb. 2007 123-125*
- Lauwers, A.**, see Yu, H. Y., *EDL Feb. 2007 154-156*
- Lauwers, A.**, see Chang, S. Z., *EDL July 2007 634-636*
- Lauwers, A.**, see Yu, H. Y., *EDL Nov. 2007 957-959*
- Lauwers, A.**, see Veloso, A., *EDL Nov. 2007 980-983*
- Le Carval, G.**, see Mayer, F., *EDL July 2007 619-621*
- Le Royer, C.**, see Mayer, F., *EDL July 2007 619-621*
- LeMinh, P.**, see Hoang, T., *EDL May 2007 383-385*
- EDLerer, D.**, see Kilchytka, V., *EDL May 2007 419-421*
- Lee, B. H.**, see Joshi, S., *EDL April 2007 308-311*
- Lee, B.-H.**, see Wang, Y., *EDL Jan. 2007 51-53*
- Lee, B.-H.**, see Wang, Y., *EDL April 2007 279-281*
- Lee, B.-H.**, see Wang, Y., *EDL July 2007 640-642*
- Lee, B.**, Biswas, N., Novak, S. R., and Misra, V., Characteristics of Ni/Gd FUSI for NMOS Gate Electrode Applications; *EDL July 2007 555-557*
- Lee, B.H.**, see Chang, M., *EDL Jan. 2007 21-23*
- Lee, C. A.**, see Jung, K.-D., *EDL March 2007 204-206*
- Lee, C.-H.**, see Wu, W.-C., *EDL March 2007 214-216*
- Lee, C.-M.**, see Chao, D.-S., *EDL Oct. 2007 871-873*
- Lee, C.-S.**, see Su, K.-H., *EDL Feb. 2007 96-99*
- Lee, C.-T.**, see Lien, Y.-C., *EDL Feb. 2007 93-95*
- Lee, D.-H.**, see Moon, C.-R., *EDL Feb. 2007 114-116*
- Lee, F.-M.**, Tsai, C.-L., Hu, C.-W., Huang, K.-F., Wu, M.-C., and Ko, S.-C., 1.3- μm GaInAsN Vertical-Cavity Surface-Emitting Lasers by Oxide-Planarized and Surface-Relief Processes for Single-Mode Operation; *EDL Feb. 2007 120-122*
- Lee, H.**, see Oh, J., *EDL Nov. 2007 1044-1046*
- Lee, H. J.**, see Jeong, Y. H., *EDL Jan. 2007 17-20*
- Lee, H. J.**, see Jeong, J. K., *EDL May 2007 389-391*

- Lee, H.-J., *see* Cho, W.-S., *EDL May 2007 386-388*
- Lee, H.-J., *see* Kim, J.-S., *EDL Oct. 2007 896-898*
- Lee, H.-S., Domeij, M., Zetterling, C.-M., Ostling, M., Allerstam, F., and Sveinbjornsson, E. O., 1200-V 5.2-mΩ·cm² 4H-SiC BJTs With a High Common-Emitter Current Gain; *EDL Nov. 2007 1007-1009*
- Lee, I.-C., *see* Tsai, C.-C., *EDL Nov. 2007 1010-1013*
- Lee, J., *see* Jeong, J. K., *EDL May 2007 389-391*
- Lee, J. C., *see* Akbar, M. S., *EDL Feb. 2007 132-134*
- Lee, J. C., *see* Zhang, M. H., *EDL March 2007 195-197*
- Lee, J. C., *see* Joshi, S., *EDL April 2007 308-311*
- Lee, J. D., *see* Jung, K.-D., *EDL March 2007 204-206*
- Lee, J. D., *see* Kang, I. M., *EDL May 2007 425-427*
- Lee, J. D., *see* Choi, W. Y., *EDL Aug. 2007 743-745*
- Lee, J. R., *see* Chen, J. F., *EDL Nov. 2007 1033-1035*
- Lee, J. Y., *see* Hsu, H., *EDL Nov. 2007 964-966*
- Lee, J.-H., *see* Park, K.-H., *EDL Feb. 2007 148-150*
- Lee, J.-H., *see* Jung, H.-A.-R., *EDL Dec. 2007 1126-1128*
- Lee, J.-W., *see* Chen, C.-Y., *EDL May 2007 392-394*
- Lee, J.-W., Chang, J.-W., Kim, D.-J., Yoon, Y.-S., and Kim, J.-K., Performance Improvement of Organic Thin-Film Transistors by Electrode/Pentacene Interface Treatment Using a Hydrogen Plasma; *EDL May 2007 379-382*
- Lee, J., *see* Mei, X. B., *EDL June 2007 470-472*
- Lee, J., *see* Han, J.-W., *EDL July 2007 625-627*
- Lee, K.-S., Kim, Y.-S., Hong, Y.-K., and Jeong, Y.-H., 35-nm Zigzag T-Gate In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As Metamorphic GaAs HEMTs With an Ultrahigh f_{\max} of 520 GHz; *EDL Aug. 2007 672-675*
- Lee, M. K., *see* Lim, B. O., *EDL July 2007 546-548*
- Lee, P.-H., *see* Chen, C.-Y., *EDL May 2007 392-394*
- Lee, R. T. P., *see* Lim, A. E.-J., *EDL June 2007 482-485*
- Lee, R. T. P., *see* Tan, K.-M., *EDL Oct. 2007 905-908*
- Lee, R. T. P., *see* Liow, T.-Y., *EDL Nov. 2007 1014-1017*
- Lee, R. T. P., Lim, A. E.-J., Tan, K.-M., Liow, T.-Y., Lo, G.-Q., Samudra, G. S., Chi, D. Z., and Yeo, Y.-C., N-channel FinFETs With 25-nm Gate Length and Schottky-Barrier Source and Drain Featuring Ytterbium Silicide; *EDL Feb. 2007 164-167*
- Lee, S., *see* Kim, D., *EDL June 2007 520-522*
- Lee, S. J., *see* Chen, J., *EDL Oct. 2007 862-864*
- Lee, S. J., *see* Loh, W. Y., *EDL Nov. 2007 984-986*
- Lee, S., and Yang, K., Sub-1-V Supply Self-Adaptive CMOS Image Sensor Cell With 86-dB Dynamic Range; *EDL June 2007 492-494*
- Lee, T., *see* Akbar, M. S., *EDL Feb. 2007 132-134*
- Lee, T. L., *see* Chu, L. H., *EDL Feb. 2007 82-85*
- Lee, T.-C., *see* Lin, C.-Y., *EDL May 2007 366-368*
- Lee, T.-H., *see* Lin, C.-T., *EDL Feb. 2007 111-113*
- Lee, T.-H., *see* Huang, Y.-T., *EDL Sept. 2007 815-817*
- Lee, W.-S., *see* Park, M., *EDL Aug. 2007 750-752*
- Lee, W.-S., *see* Cho, K. H., *EDL Dec. 2007 1129-1131*
- Lee, Y.-D., *see* Cho, W.-S., *EDL May 2007 386-388*
- Lee, Y.-H., *see* Cho, W.-S., *EDL May 2007 386-388*
- Lee, Y.-J., *see* Tsai, C.-C., *EDL Nov. 2007 1010-1013*
- Lehnen, P., *see* Yu, H. Y., *EDL July 2007 656-658*
- Lehnen, P., *see* Yu, H. Y., *EDL Nov. 2007 957-959*
- Lehnen, P., *see* Veloso, A., *EDL Nov. 2007 980-983*
- Lei, T.-F., *see* Ma, M.-W., *EDL March 2007 238-241*
- Lei, T.-F., *see* Lin, Y.-H., *EDL April 2007 267-269*
- Lei, T.-F., *see* Chen, C.-Y., *EDL May 2007 392-394*
- Lei, T.-F., *see* Chang, C.-W., *EDL Nov. 2007 993-995*
- Lemme, M. C., Echtermeyer, T. J., Baus, M., and Kurz, H., A Graphene Field-Effect Device; *EDL April 2007 282-284*
- Leobandung, E., *see* Zhu, H., *EDL Feb. 2007 168-170*
- Lew, K. L., Yoon, S. F., Wang, H., Wicaksono, S., Gupta, J. A., and McAlister, S. P., High-Gain Low Turn-On Voltage AlGaAs/GaAsNSb/GaAs Heterojunction Bipolar Transistors Grown by Molecular Beam Epitaxy; *EDL Dec. 2007 1083-1085*
- Leys, F. E., *see* Collaert, N., *EDL July 2007 646-648*
- Li, C., Liao, H., Wang, C., Yin, J., Huang, R., and Wang, Y., High-Q Integrated Inductor Using Post-CMOS Selectively Grown Porous Silicon (SGPS) Technique for RFIC Applications; *EDL Aug. 2007 763-766*
- Li, D., *see* Mei, X. B., *EDL June 2007 470-472*
- Li, H., *see* Sun, W., *EDL July 2007 631-633*
- Li, H., *see* Sun, W., *EDL Dec. 2007 1135-1137*
- Li, L., *see* Song, Y., *EDL Feb. 2007 107-110*
- Li, M., *see* Cho, K. H., *EDL Dec. 2007 1129-1131*
- Li, M.-F., *see* Lousberg, G. P., *EDL Feb. 2007 123-125*
- Li, M.-F., *see* Wang, X. P., *EDL April 2007 258-260*
- Li, M.-F., *see* Wu, C. H., *EDL April 2007 292-294*
- Li, M.-F., *see* Ang, K.-W., *EDL April 2007 301-304*
- Li, M.-F., *see* Ang, K.-W., *EDL June 2007 509-512*
- Li, M.-F., *see* Chen, J., *EDL Oct. 2007 862-864*
- Li, R., Kong, W.-R., Tao, K., Yu, L.-J., Huang, K., Ning, J., Geng, C.-Q., and Wang, C.-D., Threshold Voltage Shift Due to Mechanical Stress-Enhanced Plasma Process-Induced Damage in 0.13-μm pMOSFET; *EDL May 2007 360-362*
- Li, X., *see* Hill, R. J. W., *EDL Dec. 2007 1080-1082*
- Li, Y., Huang, R., Cai, Y., Zhou, F., Shan, X., Zhang, X., and Wang, Y., A Novel Dual-Doping Floating-Gate (DDFG) Flash Memory Featuring Low Power and High Reliability Application; *EDL July 2007 622-624*
- Li, Z., *see* Luo, X., *EDL May 2007 422-424*
- Lian, C., Xing, H., Wang, C. S., McCarthy, L., and Brown, D., DC Characteristics of AlGaAs/GaAs/GaN HBTs Formed by Direct Wafer Fusion; *EDL Jan. 2007 8-10*
- Liang, M. S., *see* Yen, F. Y., *EDL March 2007 201-203*
- Liang, M. S., *see* Wu, C. H., *EDL April 2007 292-294*
- Liang, Q., *see* Zhu, H., *EDL Feb. 2007 168-170*
- Liao, H., *see* Li, C., *EDL Aug. 2007 763-766*
- Liao, Y.-Y., Horng, S.-F., Chang, Y.-W., Lu, T.-C., Chen, K.-C., Wang, T., and Lu, C.-Y., Profiling of Nitride-Trap-Energy Distribution in SONOS Flash Memory by Using a Variable-Amplitude Low-Frequency Charge-Pumping Technique; *EDL Sept. 2007 828-830*
- Liaw, C.-W., Yeh, L., Lin, M.-J., and Lin, C. J., Pinch-Off Voltage-Adjustable High-Voltage Junction Field-Effect Transistor; *EDL Aug. 2007 737-739*
- Lien, C., *see* Chao, D.-S., *EDL Oct. 2007 871-873*
- Lien, C.-H., *see* Chen, S.-C., *EDL Sept. 2007 809-811*
- Lien, C., *see* Wang, J.-S., *EDL Nov. 2007 1040-1043*
- Lien, Y. C., *see* Chu, L. H., *EDL Feb. 2007 82-85*
- Lien, Y.-C., Chen, S.-H., Chang, E. Y., Lee, C.-T., Chu, L.-H., and Chang, C.-Y., Fabrication of 0.15-μm Γ-Shaped Gate In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As Metamorphic HEMTs Using DUV Lithography and Tilt Dry-Etching Technique; *EDL Feb. 2007 93-95*
- Lim, A., *see* Wang, X. P., *EDL April 2007 258-260*
- Lim, A. E.-J., *see* Lee, R. T. P., *EDL Feb. 2007 164-167*
- Lim, A. E.-J., Lee, R. T. P., Wang, X. P., Hwang, W. S., Tung, C. H., Samudra, G. S., Kwong, D.-L., and Yeo, Y.-C., Yttrium- and Terbium-Based Interlayer on SiO₂ and HfO₂ Gate Dielectrics for Work Function Modulation of Nickel Fully Silicided Gate in nMOSFET; *EDL June 2007 482-485*
- Lim, B. O., *see* Kim, T.-W., *EDL Dec. 2007 1086-1088*
- Lim, B. O., Lee, M. K., Baek, T. J., Han, M., Kim, S. C., and Rhee, J.-K., 50-nm T-Gate InAlAs/InGaAs Metamorphic HEMTs With Low Noise and High f_T Characteristics; *EDL July 2007 546-548*
- Lim, J. B., *see* Jeong, Y. H., *EDL Jan. 2007 17-20*
- Lim, P. S., *see* Yen, F. Y., *EDL March 2007 201-203*
- Lim, S. L., *see* Song, Y., *EDL Feb. 2007 107-110*
- Lim, Y. F., *see* Jiang, Y., *EDL July 2007 603-605*
- Lim, Y. F., *see* Rustagi, S. C., *EDL Oct. 2007 909-912*
- Lin, C. J., *see* Liaw, C.-W., *EDL Aug. 2007 737-739*
- Lin, C. T., *see* Lai, C.-M., *EDL Feb. 2007 142-144*
- Lin, C.-C., *see* Hu, C.-M., *EDL Nov. 2007 1000-1003*
- Lin, C.-H., *see* Kuo, P.-S., *EDL July 2007 596-598*
- Lin, C.-J., *see* Chen, H.-T., *EDL June 2007 499-501*
- Lin, C.-J., *see* Lai, H.-C., *EDL Sept. 2007 837-839*
- Lin, C.-L., and Chen, Y.-C., A Novel LTPS-TFT Pixel Circuit Compensating for TFT Threshold-Voltage Shift and OEDL Degradation for AMOEDL; *EDL Feb. 2007 129-131*
- Lin, C.-L., and Tsai, T.-T., A Novel Voltage Driving Method Using 3-TFT Pixel Circuit for AMOEDL; *EDL June 2007 489-491*
- Lin, C.-T., *see* Huang, Y.-T., *EDL Sept. 2007 815-817*
- Lin, C.-T., Fang, Y.-K., Yeh, W.-K., Lai, C.-M., Hsu, C.-H., Cheng, L.-W., and Ma, G. H., Impacts of Notched-Gate Structure on Contact Etch Stop Layer (CESL) Stressed 90-nm nMOSFET; *EDL May 2007 376-378*
- Lin, C.-T., Fang, Y.-K., Yeh, W.-K., Lee, T.-H., Chen, M.-S., Lai, C.-M., Hsu, C.-H., Chen, L.-W., Cheng, L.-W., and Ma, M., A Novel Strain Method for Enhancement of 90-nm Node and Beyond FUSI-Gated CMOS Performance; *EDL Feb. 2007 111-113*
- Lin, C.-T., Ramin, M., Pas, M., Wise, R., Fang, Y.-K., Hsu, C.-H., Huang, Y.-T., Cheng, L.-W., and Ma, M., CMOS Dual-Work-Function Engineering by Using Implanted Ni-FUSI; *EDL Sept. 2007 831-833*

- Lin, C.-Y.**, Wu, C.-Y., Wu, C.-Y., Lee, T.-C., Yang, F.-L., Hu, C., and Tseng, T.-Y., Effect of Top Electrode Material on Resistive Switching Properties of ZrO_2 Film Memory Devices; *EDL May 2007 366-368*
- Lin, D.-W.**, Cheng, M.-L., Wang, S.-W., Wu, C.-C., and Chen, M.-J., A Constant-Mobility Method to Enable MOSFET Series-Resistance Extraction; *EDL Dec. 2007 1132-1134*
- Lin, G. M.**, see Chang, K. M., *EDL Jan. 2007 39-41*
- Lin, G. M.**, see Chang, K. M., *EDL Sept. 2007 806-808*
- Lin, H. C.**, see Xuan, Y., *EDL Nov. 2007 935-938*
- Lin, H. J.**, see Yen, F. Y., *EDL March 2007 201-203*
- Lin, H.-T.**, Pei, Z., and Chan, Y.-J., Carrier Transport Mechanism in a Nanoparticle-Incorporated Organic Bistable Memory Device; *EDL July 2007 569-571*
- Lin, H.-T.**, Pei, Z., Chen, J.-R., Hwang, G.-W., Fan, J.-F., and Chan, Y.-J., A New Nonvolatile Bistable Polymer-Nanoparticle Memory Device; *EDL Nov. 2007 951-953*
- Lin, H.-Y.**, see Chen, C.-Y., *EDL May 2007 392-394*
- Lin, H.**, Liu, H., Kumar, A., Avci, U., Van Delden, J. S., Tiwari, S., and Kumar, A., Strained-Si Channel Super-Self-Aligned Back-Gate/Double-Gate Planar Transistors; *EDL June 2007 506-508*
- Lin, H.**, and Tiwari, S., A Novel Dual-Polarity Nonvolatile Memory; *EDL May 2007 412-415*
- Lin, L.-F.**, see Lu, T.-C., *EDL Oct. 2007 884-886*
- Lin, M.-J.**, see Liaw, C.-W., *EDL Aug. 2007 737-739*
- Lin, M.-R.**, see Pan, J., *EDL Aug. 2007 691-693*
- Lin, P.-S.**, see Chen, S.-C., *EDL Sept. 2007 809-811*
- Lin, S. S.**, see Cheng, C. Y., *EDL May 2007 408-411*
- Lin, Y. C.**, see Chiou, Y. Z., *EDL April 2007 264-266*
- Lin, Y.-H.**, Chien, C.-H., Chou, T.-H., Chao, T.-S., and Lei, T.-F., Impact of Channel Dangling Bonds on Reliability Characteristics of Flash Memory on Poly-Si Thin Films; *EDL April 2007 267-269*
- Lin, Y.-T.**, Shieh, J.-M., and Chen, C., Enhanced Hole Mobility and Reliability of Panel Epi-Like Silicon Transistors Using Backside Green Laser Activation; *EDL Sept. 2007 790-792*
- Lindsay, R.**, see Severi, S., *EDL March 2007 198-200*
- Ling, Q. D.**, see Song, Y., *EDL Feb. 2007 107-110*
- Liou, J. C.**, see Wu, W.-C., *EDL March 2007 214-216*
- Liou, J. J.**, see Fu, Y., *EDL Feb. 2007 174-176*
- Liou, J. J.**, see Lou, L., *EDL Dec. 2007 1120-1122*
- Liow, T.-Y.**, see Lee, R. T. P., *EDL Feb. 2007 164-167*
- Liow, T.-Y.**, see Tan, K.-M., *EDL Oct. 2007 905-908*
- Liow, T.-Y.**, Tan, K.-M., Lee, R. T. P., Tung, C.-H., Samudra, G. S., Balasubramanian, N., and Yeo, Y.-C., N-Channel (110)-Sidewall Strained FinFETs With Silicon-Carbon Source and Drain Stressors and Tensile Capping Layer; *EDL Nov. 2007 1014-1017*
- Liu, C. M.**, see Chen, J. F., *EDL Nov. 2007 1033-1035*
- Liu, C. W.**, see Kuo, P.-S., *EDL July 2007 596-598*
- Liu, C.-H.**, and Chiu, F.-C., Electrical Characterization of ZrO_2/Si Interface Properties in MOSFETs With ZrO_2 Gate Dielectrics; *EDL Jan. 2007 62-64*
- Liu, F.**, see Yang, C., *EDL July 2007 652-655*
- Liu, H.**, see Lin, H., *EDL June 2007 506-508*
- Liu, H. G.**, see Zhou, W., *EDL July 2007 539-542*
- Liu, H. G.**, Ostinelli, O., Zeng, Y. P., and Bolognesi, C. R., High-Current-Gain InP/GaInP/GaAsSb/InP DHBTs With $f_T = 436$ GHz; *EDL Oct. 2007 852-855*
- Liu, J.**, see Song, D., *EDL March 2007 189-191*
- Liu, J. C.**, see Chen, Y. H., *EDL Dec. 2007 1111-1113*
- Liu, J.**, and Kwong, D. L., Impacts of Dopant Segregation on the Performance and Interface-State Density of the MOSFET With FUSI NiSi Gate; *EDL Jan. 2007 11-13*
- Liu, L.-T.**, see Yang, C., *EDL July 2007 652-655*
- Liu, P. H.**, see Mei, X. B., *EDL June 2007 470-472*
- Liu, P.-T.**, see Tsai, C.-T., *EDL July 2007 584-586*
- Liu, P.-T.**, see Chen, S.-C., *EDL Sept. 2007 809-811*
- Liu, P.-T.**, Lu, H.-Y., Chen, Y.-C., and Chi, S., Degradation of Laser-Crystallized Laterally Grown Poly-Si TFT under Dynamic Stress; *EDL May 2007 401-403*
- Liu, P.-T.**, and Wu, H.-H., High-Performance Polycrystalline-Silicon TFT by Heat-Retaining Enhanced Lateral Crystallization; *EDL Aug. 2007 722-724*
- Liu, R.**, see Lai, S., *EDL July 2007 643-645*
- Liu, R.**, see Hsu, T.-H., *EDL May 2007 443-445*
- Liu, R.**, see Zhang, Z., *EDL July 2007 565-568*
- Liu, T.-J. K.**, see Choi, W. Y., *EDL Aug. 2007 743-745*
- Liu, W.**, see Mei, X. B., *EDL June 2007 470-472*
- Liu, W. K.**, see Datta, S., *EDL Aug. 2007 685-687*
- Liu, Y.**, see Luo, X., *EDL May 2007 422-424*
- Liu, Y. X.**, see Endo, K., *EDL May 2007 452-454*
- Liu, Y.**, see Feng, J., *EDL July 2007 637-639*
- Liu, Y.**, see Endo, K., *EDL Dec. 2007 1123-1125*
- Liu, Y.**, Matsukawa, T., Endo, K., Masahara, M., O'uchi, S., Ishii, K., Yamauchi, H., Tsukada, J., Ishikawa, Y., and Suzuki, E., Cointegration of High-Performance Tied-Gate Three-Terminal FinFETs and Variable Threshold-Voltage Independent-Gate Four-Terminal FinFETs With Asymmetric Gate-Oxide Thicknesses; *EDL June 2007 517-519*
- Lo, G. Q.**, see Fang, W. W., *EDL March 2007 211-213*
- Lo, G. Q.**, see Wang, X. P., *EDL April 2007 258-260*
- Lo, G. Q.**, see Singh, N., *EDL July 2007 558-561*
- Lo, G. Q.**, see Jiang, Y., *EDL July 2007 603-605*
- Lo, G. Q.**, see Rustagi, S. C., *EDL Oct. 2007 909-912*
- Lo, G. Q.**, see Rustagi, S. C., *EDL Nov. 2007 1021-1024*
- Lo, G. Q.**, see Loh, W. Y., *EDL Nov. 2007 984-986*
- Lo, G. Q.**, see Zang, H., *EDL Dec. 2007 1117-1119*
- Lo, G.-Q.**, see Lee, R. T. P., *EDL Feb. 2007 164-167*
- Locquet, J.-P.**, see Sun, Y., *EDL June 2007 473-475*
- Loh, T. H.**, see Loh, W. Y., *EDL Nov. 2007 984-986*
- Loh, W. Y.**, see Wang, X. P., *EDL April 2007 258-260*
- Loh, W. Y.**, see Jiang, Y., *EDL July 2007 603-605*
- Loh, W. Y.**, see Zang, H., *EDL Dec. 2007 1117-1119*
- Loh, W. Y.**, Wang, J., Ye, J. D., Yang, R., Nguyen, H. S., Chua, K. T., Song, J. F., Loh, T. H., Xiong, Y. Z., Lee, S. J., Yu, M. B., Lo, G. Q., and Kwong, D. L., Impact of Local Strain From Selective Epitaxial Germanium With Thin Si/SiGe Buffer on High-Performance p-i-n Photodetectors With a Low Thermal Budget; *EDL Nov. 2007 984-986*
- Loiko, K.**, see Winstead, B., *EDL Aug. 2007 719-721*
- Loo, R.**, see Collaert, N., *EDL July 2007 646-648*
- Loo, R.**, see Simoen, E., *EDL Nov. 2007 987-989*
- Lou, C.**, see Wei, L., *EDL Aug. 2007 688-690*
- Lou, C.-C.**, see Yang, M.-J., *EDL Oct. 2007 902-904*
- Lou, L.**, and Liou, J. J., An Unassisted, Low Trigger-, and High Holding-Voltage SCR (uSCR) for On-Chip ESD-Protection Applications; *EDL Dec. 2007 1120-1122*
- Loubychev, D.**, see Datta, S., *EDL Aug. 2007 685-687*
- Lousberg, G. P.**, Yu, H. Y., Froment, B., Augendre, E., De Keersgieter, A., Lauwers, A., Li, M.-F., Absil, P., Jurczak, M., and Biesemans, S., Schottky-Barrier Height Lowering by an Increase of the Substrate Doping in PtSi Schottky Barrier Source/Drain FETs; *EDL Feb. 2007 123-125*
- Lu, C.**, see Lai, S., *EDL July 2007 643-645*
- Lu, C.-C.**, see Lu, C.-Y., *EDL May 2007 432-435*
- Lu, C.-Y.**, see Hsu, T.-H., *EDL May 2007 443-445*
- Lu, C.-Y.**, Chang-Liao, K.-S., Lu, C.-C., Tsai, P.-H., and Wang, T.-K., Detection of Border Trap Density and Energy Distribution Along the Gate Dielectric Bulk of High- κ Gated MOS Devices; *EDL May 2007 432-435*
- Lu, C.-Y.**, see Shiu, J.-Y., *EDL June 2007 476-478*
- Lu, C.-Y.**, see Liao, Y.-Y., *EDL Sept. 2007 828-830*
- Lu, H.-Y.**, see Liu, P.-T., *EDL May 2007 401-403*
- Lu, J.**, see Huang, F., *EDL Nov. 2007 1025-1028*
- Lu, T.-C.**, see Liao, Y.-Y., *EDL Sept. 2007 828-830*
- Lu, T.-C.**, Kao, T.-T., Kao, C.-C., Chu, J.-T., Yeh, K.-F., Lin, L.-F., Peng, Y.-C., Huang, H.-W., Kuo, H.-C., and Wang, S.-C., GaN-Based High-Q Vertical-Cavity Light-Emitting Diodes; *EDL Oct. 2007 884-886*
- Lu, W. T.**, see Cheng, C. Y., *EDL May 2007 408-411*
- Lu, Y.-H.**, see Yang, M.-J., *EDL Oct. 2007 902-904*
- Lu, Y.-X.**, see Guo, P., *EDL July 2007 572-574*
- Lu, Z.**, see Fossum, J. G., *EDL June 2007 513-516*
- Lu, Z.**, and Fossum, J. G., Short-Channel Effects in Independent-Gate FinFETs; *EDL Feb. 2007 145-147*
- Lue, H.**, see Lai, S., *EDL July 2007 643-645*
- Lue, H. Y.**, see Hsu, T.-H., *EDL May 2007 443-445*
- Lugli, P.**, see Tedde, S., *EDL Oct. 2007 893-895*
- Luo, G.**, see Lai, S., *EDL July 2007 643-645*
- Luo, G.-L.**, see Yang, M.-J., *EDL Oct. 2007 902-904*
- Luo, X.**, Zhang, B., Li, Z., Guo, Y., Tang, X., and Liu, Y., A Novel 700-V SOI LDMOS With Double-Sided Trench; *EDL May 2007 422-424*

M

Ma, G. H., see Lin, C.-T., *EDL May 2007 376-378*

- Ma, M.**, *see* Lin, C.-T., *EDL Feb. 2007 111-113*
- Ma, M.-W.**, *see* Chen, C.-Y., *EDL May 2007 392-394*
- Ma, M.-W.**, Wu, C.-H., Yang, T.-Y., Kao, K.-H., Wu, W.-C., Wang, S.-J., Chao, T.-S., and Lei, T.-F., Impact of High- κ Offset Spacer in 65-nm Node SOI Devices; *EDL March 2007 238-241*
- Ma, M.**, *see* Huang, Y.-T., *EDL Sept. 2007 815-817*
- Ma, M.**, *see* Lin, C.-T., *EDL Sept. 2007 831-833*
- Ma, Z.**, *see* Yuan, H.-C., *EDL July 2007 590-592*
- Macintyre, D.**, *see* Hill, R. J. W., *EDL Dec. 2007 1080-1082*
- Maclean, J. O.**, *see* Kuball, M., *EDL Feb. 2007 86-89*
- Madan, A.**, *see* Ang, K.-W., *EDL June 2007 509-512*
- Maes, H.**, *see* Shickova, A., *EDL March 2007 242-244*
- Maes, H. E.**, *see* Martens, K., *EDL May 2007 436-439*
- Maes, H.**, *see* Furnemont, A., *EDL April 2007 276-278*
- Maes, H.**, *see* Aoulaiche, M., *EDL July 2007 613-615*
- Maes, J. W.**, *see* Aoulaiche, M., *EDL July 2007 613-615*
- Mahapatra, S.**, *see* Datta, A., *EDL May 2007 446-448*
- Majhi, P.**, *see* Joshi, S., *EDL April 2007 308-311*
- Majhi, P.**, *see* Oh, J., *EDL Nov. 2007 1044-1046*
- Maji, D.**, Duttagupta, S. P., Rao, V. R., Yeo, C. C., and Cho, B.-J., Border-Trap Characterization in High- κ Strained-Si MOSFETs; *EDL Aug. 2007 731-733*
- Makimoto, T.**, *see* Shiu, J.-Y., *EDL June 2007 476-478*
- Mallinger, M.**, *see* Zhao, F., *EDL May 2007 398-400*
- Manoj, C. R.**, and Rao, V. R., Impact of High- k Gate Dielectrics on the Device and Circuit Performance of Nanoscale FinFETs; *EDL April 2007 295-297*
- Mantegazza, D.**, Ielmini, D., Pirovano, A., and Lacaita, A. L., Anomalous Cells With Low Reset Resistance in Phase-Change-Memory Arrays; *EDL Oct. 2007 865-867*
- Mantl, S.**, *see* Zhang, M., *EDL March 2007 223-225*
- Mao, L.**, The Effects of the Injection-Channel Velocity on the Gate Leakage Current of Nanoscale MOSFETs; *EDL Feb. 2007 161-163*
- Marathe, A.**, *see* Yu, C., *EDL Jan. 2007 45-47*
- Marinoni, A.**, *see* Fantini, P., *EDL Dec. 2007 1114-1116*
- Marmioli, A.**, *see* Fantini, P., *EDL Dec. 2007 1114-1116*
- Marshall, J. C.**, Herman, D. L., Vernier, P. T., DeVoe, D. L., and Gaitan, M., Young's Modulus Measurements in Standard IC CMOS Processes Using MEMS Test Structures; *EDL Nov. 2007 960-963*
- Martens, K.**, Rosmeulen, M., Kaczer, B., Groeseneken, G., and Maes, H. E., Electrical Characterization of Leaky Charge-Trapping High- κ MOS Devices Using Pulsed $Q-V$; *EDL May 2007 436-439*
- Martin, M. J.**, *see* Rengel, R., *EDL Feb. 2007 171-173*
- Martin, T.**, *see* Kuball, M., *EDL Feb. 2007 86-89*
- Masahara, M.**, *see* Endo, K., *EDL May 2007 452-454*
- Masahara, M.**, *see* Liu, Y., *EDL June 2007 517-519*
- Masahara, M.**, *see* Endo, K., *EDL Dec. 2007 1123-1125*
- Masahara, M.**, Surdeanu, R., Witters, L., Doornbos, G., Nguyen, V. H., Van den Bosch, G., Vrancken, C., Devriendt, K., Neuilly, F., Kunnen, E., Jurczak, M., and Biesemans, S., Demonstration of Asymmetric Gate-Oxide Thickness Four-Terminal FinFETs Having Flexible Threshold Voltage and Good Subthreshold Slope; *EDL March 2007 217-219*
- Massengill, L. W.**, *see* Warren, K. M., *EDL Feb. 2007 180-182*
- Massoud, Y.**, *see* Nieuwoudt, A., *EDL April 2007 305-307*
- Mathews, K.**, *see* Zaman, R. J., *EDL Oct. 2007 916-918*
- Matsukawa, T.**, *see* Endo, K., *EDL May 2007 452-454*
- Matsukawa, T.**, *see* Liu, Y., *EDL June 2007 517-519*
- Matsukawa, T.**, *see* Endo, K., *EDL Dec. 2007 1123-1125*
- Matthews, K.**, *see* Huang, Y.-T., *EDL Sept. 2007 815-817*
- Mayer, F.**, Le Royer, C., Le Carval, G., Clavelier, L., and Deleonibus, S., Experimental and TCAD Investigation of the Two Components of the Impact Ionization MOSFET (IMOS) Switching; *EDL July 2007 619-621*
- McAlister, S. P.**, *see* Chiang, K. C., *EDL Aug. 2007 694-696*
- McAlister, S. P.**, *see* Yang, H. J., *EDL Oct. 2007 913-915*
- McAlister, S. P.**, *see* Cheng, C. H., *EDL Dec. 2007 1095-1097*
- McAlister, S. P.**, *see* Cheng, C. F., *EDL Dec. 2007 1092-1094*
- McAlister, S. P.**, *see* Lew, K. L., *EDL Dec. 2007 1083-1085*
- McCarthy, L.**, *see* Lian, C., *EDL Jan. 2007 8-10*
- McCarthy, L.**, *see* Chu, R., *EDL Sept. 2007 781-783*
- McIntyre, P. C.**, *see* Wang, Z., *EDL Jan. 2007 14-16*
- McVittie, J.**, *see* Wang, Z., *EDL Jan. 2007 14-16*
- Mei, X. B.**, Yoshida, W., Deal, W. R., Liu, P. H., Lee, J., Uyeda, J., Dang, L., Wang, J., Liu, W., Li, D., Barsky, M., Kim, Y. M., Lange, M., Chin, T. P., Radisic, V., Gaier, T., Fung, A., Samoska, L., and Lai, R., 35-nm InP HEMT SMMIC Amplifier With 4.4-dB Gain at 308 GHz; *EDL June 2007 470-472*
- Meindl, J. D.**, *see* Naeemi, A., *EDL Feb. 2007 135-138*
- Meindl, J. D.**, *see* Naeemi, A., *EDL May 2007 428-431*
- Meindl, J. D.**, *see* Sekar, D. C., *EDL Aug. 2007 767-769*
- Mendenhall, M. H.**, *see* Warren, K. M., *EDL Feb. 2007 180-182*
- Mercha, A.**, *see* Guo, W., *EDL April 2007 288-291*
- Merlos, A.**, *see* Garcia-Canton, J., *EDL Jan. 2007 27-29*
- Mertens, S.**, *see* Yu, H. Y., *EDL Feb. 2007 154-156*
- Meunier-Beillard, P.**, *see* Choi, L. J., *EDL April 2007 270-272*
- Meuris, M.**, *see* Nicholas, G., *EDL Sept. 2007 825-827*
- Mhaisalkar, S. G.**, *see* Tiwari, S. P., *EDL Oct. 2007 880-883*
- Mikhelashvili, V.**, and Eisenstein, G., High- κ Al₂O₃-HfTiO Nanolaminates With Less Than 0.8-nm Equivalent Oxide Thickness; *EDL Jan. 2007 24-26*
- Mimura, A.**, *see* Sugawara, Y., *EDL May 2007 395-397*
- Mishima, T.**, *see* Nomoto, K., *EDL Nov. 2007 939-941*
- Mishra, U. K.**, *see* Chu, R., *EDL Sept. 2007 781-783*
- Mishra, U. K.**, *see* Poblentz, C., *EDL Nov. 2007 945-947*
- Misra, V.**, *see* Lee, B., *EDL July 2007 555-557*
- Mitsubishi, R.**, *see* Yu, H. Y., *EDL July 2007 656-658*
- Miyamoto, Y.**, *see* Chang, C. Y., *EDL Oct. 2007 856-858*
- Mizutani, M.**, *see* Kawahara, T., *EDL Oct. 2007 868-870*
- Mizutani, T.**, Ito, M., Kishimoto, S., and Nakamura, F., AlGaIn/GaN HEMTs With Thin InGaIn Cap Layer for Normally Off Operation; *EDL July 2007 549-551*
- Mo, Y. G.**, *see* Jeong, J. K., *EDL May 2007 389-391*
- Moens, P.**, *see* Bakeroot, B., *EDL May 2007 416-418*
- Mohajerzadeh, S.**, *see* Jamei, M., *EDL March 2007 207-210*
- Mohanraj, S.**, *see* Singh, N., *EDL July 2007 558-561*
- Moon, C.-R.**, Jung, J., Kwon, D.-W., Yoo, J., Lee, D.-H., and Kim, K., Application of Plasma-Doping (PLAD) Technique to Reduce Dark Current of CMOS Image Sensors; *EDL Feb. 2007 114-116*
- Moran, D. A. J.**, *see* Hill, R. J. W., *EDL Dec. 2007 1080-1082*
- Mouthaan, K.**, *see* Sun, S., *EDL March 2007 220-222*
- Muller, C. R.**, Worschech, L., Hopfner, P., Hoffing, S., and Forchel, A., Monolithically Integrated Logic NOR Gate Based on GaAs/AlGaAs Three-Terminal Junctions; *EDL Oct. 2007 859-861*
- Murata, N.**, *see* Kawahara, T., *EDL Oct. 2007 868-870*
- Murthy, J. Y.**, *see* Pimparkar, N., *EDL Feb. 2007 157-160*

N

- Nieuwoudt, A.**, and Massoud, Y., Performance Implications of Inductive Effects for Carbon-Nanotube Bundle Interconnect; *EDL April 2007 305-307*
- Niiyama, Y.**, see Kambayashi, H., *EDL Dec. 2007 1077-1079*
- Ning, J.**, see Li, R., *EDL May 2007 360-362*
- Nirschl, Th.**, Weis, M., Fulde, M., and Schmitt-Landsiedel, D., Correction to "Revision of Tunneling Field-Effect Transistor in Standard CMOS Technologies"; *EDL April 2007 315-315*
- Nishi, Y.**, see Wang, Z., *EDL Jan. 2007 14-16*
- Nishida, T.**, see Suthram, S., *EDL Jan. 2007 58-61*
- Nishida, Y.**, see Kawahara, T., *EDL Oct. 2007 868-870*
- Nishiguchi, K.**, Fujiwara, A., Ono, Y., Inokawa, H., and Takahashi, Y., Long Retention of Gain-Cell Dynamic Random Access Memory With Undoped Memory Node; *EDL Jan. 2007 48-50*
- Nishimura, K.**, see Shigekawa, N., *EDL Feb. 2007 90-92*
- Nitta, T.**, see Saito, W., *EDL Aug. 2007 676-678*
- Nomoto, K.**, Tajima, T., Mishima, T., Satoh, M., and Nakamura, T., Remarkable Reduction of On-Resistance by Ion Implantation in GaN/AlGaIn/GaN HEMTs With Low Gate Leakage Current; *EDL Nov. 2007 939-941*
- Nomura, K.**, see Ofuji, M., *EDL April 2007 273-275*
- Nomura, T.**, see Kambayashi, H., *EDL Dec. 2007 1077-1079*
- Norris, C.**, see Kim, D., *EDL June 2007 520-522*
- Norris, C.**, see Kim, D., *EDL July 2007 616-618*
- Novak, S. R.**, see Lee, B., *EDL July 2007 555-557*

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- O'Sullivan, B. J.**, see Veloso, A., *EDL Nov. 2007 980-983*
- O'uchi, S.**, see Endo, K., *EDL May 2007 452-454*
- O'uchi, S.-I.**, see Endo, K., *EDL Dec. 2007 1123-1125*
- O'uchi, S.**, see Liu, Y., *EDL June 2007 517-519*
- Ofuji, M.**, Abe, K., Shimizu, H., Kaji, N., Hayashi, R., Sano, M., Kumomi, H., Nomura, K., Kamiya, T., and Hosono, H., Fast Thin-Film Transistor Circuits Based on Amorphous Oxide Semiconductor; *EDL April 2007 273-275*
- Oh, J. W.**, see Joshi, S., *EDL April 2007 308-311*
- Oh, J.**, Majhi, P., Lee, H., Yoo, O., Banerjee, S., Kang, C. Y., Yang, J.-W., Harris, R., Tseng, H.-H., and Jammy, R., Improved Electrical Characteristics of Ge-on-Si Field-Effect Transistors With Control EDL Ge Epitaxial Layer Thickness on Si Substrates; *EDL Nov. 2007 1044-1046*
- Ohashi, T.**, Kubota, T., and Nakajima, A., Ar Annealing for Suppression of Gate Oxide Thinning at Shallow Trench Isolation Edge; *EDL July 2007 562-564*
- Ohno, T.**, see Umezawa, N., *EDL May 2007 363-365*
- Ohtou, T.**, Sugii, N., and Hiramoto, T., Impact of Parameter Variations and Random Dopant Fluctuations on Short-Channel Fully Depleted SOI MOS-FETs With Extremely Thin BOX; *EDL Aug. 2007 740-742*
- Ok, I. J.**, see Akbar, M. S., *EDL Feb. 2007 132-134*
- Ok, I. J.**, see Zhang, M. H., *EDL March 2007 195-197*
- Okoniewski, M.**, see Zine-El-Abidine, I., *EDL March 2007 226-228*
- Omampuliyur, S. R.**, see Rustagi, S. C., *EDL Nov. 2007 1021-1024*
- Omura, I.**, see Saito, W., *EDL Aug. 2007 676-678*
- Ono, Y.**, see Nishiguchi, K., *EDL Jan. 2007 48-50*
- Onsia, B.**, see Veloso, A., *EDL Nov. 2007 980-983*
- Onsia, B.**, see Yu, H. Y., *EDL Nov. 2007 957-959*
- Ootomo, S.**, see Kambayashi, H., *EDL Dec. 2007 1077-1079*
- Opsomer, K.**, see Yu, H. Y., *EDL Feb. 2007 154-156*
- Ostinelli, O.**, see Liu, H. G., *EDL Oct. 2007 852-855*
- Ostling, M.**, see Zhang, Z., *EDL July 2007 565-568*
- Ostling, M.**, see Lee, H.-S., *EDL Nov. 2007 1007-1009*
- Oudwan, M.**, see Hatzopoulos, A. T., *EDL Sept. 2007 803-805*
- Ouellet, L.**, see Brassard, D., *EDL April 2007 261-263*

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- Padilla, A.**, Shin, K., King Liu, T.-J., Hyun, J. W., Yoo, I., and Park, Y., Dual-Bit Gate-Sidewall Storage FinFET NVM and New Method of Charge Detection; *EDL June 2007 502-505*
- Paek, K.-K.**, see Shin, K.-S., *EDL July 2007 581-583*
- Pailloncy, G.**, see Kilchytka, V., *EDL May 2007 419-421*
- Palestri, P.**, see Zilli, M., *EDL Nov. 2007 1036-1039*
- Pan, H. C.**, see Chiang, K. C., *EDL March 2007 235-237*

- Pan, H. C.**, see Chiang, K. C., *EDL Aug. 2007 694-696*
- Pan, H. C.**, see Cheng, C. H., *EDL Dec. 2007 1095-1097*
- Pan, J.**, Topol, A., Shao, I., Sung, C.-Y., Iacoponi, J., and Lin, M.-R., Novel Approach to Reduce Source/Drain Series and Contact Resistance in High-Performance UTSOI CMOS Devices Using Selective Electrodeless CoWP or CoB Process; *EDL Aug. 2007 691-693*
- Pan, T.-M.**, Hsieh, C.-I., Huang, T.-Y., Yang, J.-R., and Kuo, P.-S., Good High-Temperature Stability of TiN/Al₂O₃/WN/TiN Capacitors; *EDL Nov. 2007 954-956*
- Pantelides, S. T.**, see Hadjisavvas, G., *EDL Nov. 2007 1018-1020*
- Park, B.-G.**, see Jung, K.-D., *EDL March 2007 204-206*
- Park, B.-G.**, see Choi, W. Y., *EDL Aug. 2007 743-745*
- Park, D.**, see Han, J.-W., *EDL July 2007 625-627*
- Park, D.-W.**, see Jung, K.-D., *EDL March 2007 204-206*
- Park, D.**, see Cho, K. H., *EDL Dec. 2007 1129-1131*
- Park, D.**, Rhee, J., and Joo, Y., A Wide Dynamic-Range CMOS Image Sensor Using Self-Reset Technique; *EDL Oct. 2007 890-892*
- Park, H.**, see Chang, M., *EDL Jan. 2007 21-23*
- Park, J. S.**, see Kim, T. H., *EDL Oct. 2007 874-876*
- Park, J.-H.**, see Cho, W.-S., *EDL May 2007 386-388*
- Park, J.-H.**, see Shin, K.-S., *EDL July 2007 581-583*
- Park, K.-H.**, see Jung, H.-A.-R., *EDL Dec. 2007 1126-1128*
- Park, K.-H.**, and Lee, J.-H., Gate Workfunction Engineering in Bulk FinFETs for Sub-50-nm DRAM Cell Transistors; *EDL Feb. 2007 148-150*
- Park, M.**, Suh, K., Kim, K., Hur, S.-H., Kim, K., and Lee, W.-S., The Effect of Trapped Charge Distributions on Data Retention Characteristics of NAND Flash Memory Cells; *EDL Aug. 2007 750-752*
- Park, S. D.**, see Kim, T.-W., *EDL Dec. 2007 1086-1088*
- Park, S. K.**, Anthony, J. E., and Jackson, T. N., Solution-Processed TIPS-Pentacene Organic Thin-Film-Transistor Circuits; *EDL Oct. 2007 877-879*
- Park, Y.**, see Padilla, A., *EDL June 2007 502-505*
- Parsons, J.**, see Nicholas, G., *EDL Sept. 2007 825-827*
- Partlow, D. P.**, see Jessen, G. H., *EDL May 2007 354-356*
- Pas, M.**, see Lin, C.-T., *EDL Sept. 2007 831-833*
- Pascual, E.**, see Rengel, R., *EDL Feb. 2007 171-173*
- Passlack, M.**, see Rajagopalan, K., *EDL Feb. 2007 100-102*
- Passlack, M.**, see Hill, R. J. W., *EDL Dec. 2007 1080-1082*
- Pawlak, B. J.**, see Severi, S., *EDL March 2007 198-200*
- Pei, Z.**, see Lin, H.-T., *EDL July 2007 569-571*
- Pei, Z.**, see Lin, H.-T., *EDL Nov. 2007 951-953*
- Pellish, J. A.**, see Warren, K. M., *EDL Feb. 2007 180-182*
- Pellizzer, F.**, see Ventrice, D., *EDL Nov. 2007 973-975*
- Penaud, J.**, see Cornu-Frulleux, F., *EDL June 2007 523-526*
- Peng, C.-Y.**, see Kuo, P.-S., *EDL July 2007 596-598*
- Peng, W.-C.**, see Wu, W.-C., *EDL March 2007 214-216*
- Peng, Y.-C.**, see Lu, T.-C., *EDL Oct. 2007 884-886*
- Pey, K. L.**, see Yu, H. P., *EDL Dec. 2007 1098-1101*
- Pham, V.**, see Yu, C., *EDL Jan. 2007 45-47*
- Pichon, L.**, Boukhenoufa, A., Cordier, C., and Cretu, B., Numerical Simulation of Low-Frequency Noise in Polysilicon Thin-Film Transistors; *EDL Aug. 2007 716-718*
- Pilgrim, N. J.**, see Khalid, A., *EDL Oct. 2007 849-851*
- Pimparkar, N.**, Cao, Q., Kumar, S., Murthy, J. Y., Rogers, J., and Alam, M. A., Current-Voltage Characteristics of Long-Channel Nanobundle Thin-Film Transistors: A "Bottom-Up" Perspective; *EDL Feb. 2007 157-160*
- Pimparkar, N.**, Kocabas, C., Kang, S. J., Rogers, J., and Alam, M. A., Limits of Performance Gain of Aligned CNT Over Randomized Network: Theoretical Predictions and Experimental Validation; *EDL July 2007 593-595*
- Pinto, A.**, see Huang, Y.-T., *EDL Sept. 2007 815-817*
- Piontek, A.**, see Choi, L. J., *EDL April 2007 270-272*
- Pirovano, A.**, see Mantegazza, D., *EDL Oct. 2007 865-867*
- Pirovano, A.**, see Ventrice, D., *EDL Nov. 2007 973-975*
- Plouchart, J.-O.**, see Kim, D., *EDL June 2007 520-522*
- Plouchart, J.-O.**, see Kim, D., *EDL July 2007 616-618*
- Plummer, J. D.**, see Feng, J., *EDL July 2007 637-639*
- Poblenz, C.**, Corrión, A. L., Recht, F., Suh, C. S., Chu, R., Shen, L., Speck, J. S., and Mishra, U. K., Power Performance of AlGaIn/GaN HEMTs Grown on SiC by Ammonia-MBE at 4 and 10 GHz; *EDL Nov. 2007 945-947*
- Pomeroy, J. W.**, see Kuball, M., *EDL Feb. 2007 86-89*
- Poortmans, J.**, see Carnel, L., *EDL Oct. 2007 899-901*
- Porter, M. E.**, see Warren, K. M., *EDL Feb. 2007 180-182*
- Pourtois, G.**, see Veloso, A., *EDL Nov. 2007 980-983*

Prost, W., see Do, Q.-T., *EDL Aug. 2007 682-684*

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Rachmady, W., see Datta, S., *EDL Aug. 2007 685-687*

Radisic, V., see Mei, X. B., *EDL June 2007 470-472*

Radosavljevic, M., see Datta, S., *EDL Aug. 2007 685-687*

Radosavljevic, M., see Chang, C. Y., *EDL Oct. 2007 856-858*

Rafhay, Q., see Duane, R., *EDL May 2007 440-442*

Ragnarsson, L.-A., see Yu, H. Y., *EDL July 2007 656-658*

Ragnarsson, L.-A., Chang, V. S., Yu, H. Y., Cho, H.-J., Conard, T., Yin, K. M., Delabie, A., Swerts, J., Schram, T., De Gendt, S., and Biesemans, S., Achieving Conduction Band-Edge Effective Work Functions by La₂O₃ Capping of Hafnium Silicates; *EDL June 2007 486-488*

Rajagopalan, K., see Hill, R. J. W., *EDL Dec. 2007 1080-1082*

Rajagopalan, K., Droopad, R., Abrokwhah, J., Zurcher, P., Fejes, P., and Passlack, M., 1- μ m Enhancement Mode GaAs N-Channel MOSFETs With Transconductance Exceeding 250 mS/mm; *EDL Feb. 2007 100-102*

Ramgopal Rao, V., see Tiwari, S. P., *EDL Oct. 2007 880-883*

Ramin, M., see Huang, Y.-T., *EDL Sept. 2007 815-817*

Ramin, M., see Lin, C.-T., *EDL Sept. 2007 831-833*

Rao, V. R., see Manoj, C. R., *EDL April 2007 295-297*

Rao, V. R., see Maji, D., *EDL Aug. 2007 731-733*

Raskin, J.-P., see Kilchyska, V., *EDL May 2007 419-421*

Raskin, J.-P., see Simoen, E., *EDL Oct. 2007 919-921*

Recht, F., see Poblenz, C., *EDL Nov. 2007 945-947*

Redaelli, A., see Ventrice, D., *EDL Nov. 2007 973-975*

Ree, M., see Kim, M., *EDL Nov. 2007 967-969*

Reed, R. A., see Warren, K. M., *EDL Feb. 2007 180-182*

Regolin, I., see Do, Q.-T., *EDL Aug. 2007 682-684*

Ren, C., see Jiang, Y., *EDL July 2007 603-605*

Ren, T.-L., see Yang, C., *EDL July 2007 652-655*

Rengel, R., Pascual, E., and Martin, M. J., Injected Current and Quantum Transmission Coefficient in Low Schottky Barriers: WKB and Airy Approaches; *EDL Feb. 2007 171-173*

Rhee, J., see Park, D., *EDL Oct. 2007 890-892*

Rhee, J.-K., see Lim, B. O., *EDL July 2007 546-548*

Rhee, J.-K., see Kim, T.-W., *EDL Dec. 2007 1086-1088*

Rhee, S. J., see Akbar, M. S., *EDL Feb. 2007 132-134*

Richard, O., see Yu, H. Y., *EDL Feb. 2007 154-156*

Riedel, G. J., see Kuball, M., *EDL Feb. 2007 86-89*

Rieh, J.-S., see Kim, D., *EDL June 2007 520-522*

Ries, M., see Huang, Y.-T., *EDL Sept. 2007 815-817*

Ristic, S., and Jaeger, N. A. F., Robust Coupled-Quantum-Well Structure for Use in Electrorefraction Modulators; *EDL Jan. 2007 30-32*

Ritenour, A., Hennessy, J., and Antoniadis, D. A., Investigation of Carrier Transport in Germanium MOSFETs With WN/Al₂O₃/AlN Gate Stacks; *EDL Aug. 2007 746-749*

Robertson, M. D., see Jamei, M., *EDL March 2007 207-210*

Rogers, J., see Pimparkar, N., *EDL Feb. 2007 157-160*

Rogers, J., see Pimparkar, N., *EDL July 2007 593-595*

Rooyackers, R., see Collaert, N., *EDL July 2007 646-648*

Rorsman, N., see Shiu, J.-Y., *EDL June 2007 476-478*

Rosmeulen, M., see Furnemont, A., *EDL April 2007 276-278*

Rosmeulen, M., see Martens, K., *EDL May 2007 436-439*

Rossee, E., see Yu, H. Y., *EDL Feb. 2007 154-156*

Routoure, J.-M., see Guo, W., *EDL April 2007 288-291*

Rudenko, T., Kilchyska, V., Collaert, N., Jurczak, M., Nazarov, A., and Flandre, D., Substrate Bias Effect Linked to Parasitic Series Resistance in Multiple-Gate SOI MOSFETs; *EDL Sept. 2007 834-836*

Ruiz, N., see Sun, Y., *EDL June 2007 473-475*

Rustagi, S. C., see Fang, W. W., *EDL March 2007 211-213*

Rustagi, S. C., see Sun, S., *EDL March 2007 220-222*

Rustagi, S. C., see Singh, N., *EDL July 2007 558-561*

Rustagi, S. C., Singh, N., Fang, W. W., Buddharaju, K. D., Omampuliyur, S. R., Teo, S. H. G., Tung, C. H., Lo, G. Q., Balasubramanian, N., and Kwong, D. L., CMOS Inverter Based on Gate-All-Around Silicon-Nanowire MOSFETs Fabricated Using Top-Down Approach; *EDL Nov. 2007 1021-1024*

Rustagi, S. C., Singh, N., Lim, Y. F., Zhang, G., Wang, S., Lo, G. Q., Balasubramanian, N., and Kwong, D.-L., Low-Temperature Transport Characteristics and Quantum-Confinement Effects in Gate-All-Around Si-Nanowire N-MOSFET; *EDL Oct. 2007 909-912*

Ryu, S.-H., see Agarwal, A., *EDL July 2007 587-589*

S

Sadana, D. K., see Sun, Y., *EDL June 2007 473-475*

Sadeghi, M., see Vukusic, J., *EDL May 2007 340-342*

Sadi, T., and Kelsall, R. W., Hot-Phonon Effect on the Electrothermal Behavior of Submicrometer III-V HEMTs; *EDL Sept. 2007 787-789*

Saito, W., Nitta, T., Kakiuchi, Y., Saito, Y., Tsuda, K., Omura, I., and Yamaguchi, M., ON-Resistance Modulation of High Voltage GaN HEMT on Sapphire Substrate Under High Applied Voltage; *EDL Aug. 2007 676-678*

Saito, Y., see Saito, W., *EDL Aug. 2007 676-678*

Saitou, K., see Chow, L. L. W., *EDL June 2007 479-481*

Sakashita, S., see Kawahara, T., *EDL Oct. 2007 868-870*

Samavedam, S. B., see Winstead, B., *EDL Aug. 2007 719-721*

Samoska, L., see Mei, X. B., *EDL June 2007 470-472*

Samudra, G., see Wong, H.-S., *EDL Aug. 2007 703-705*

Samudra, G. S., see Lee, R. T. P., *EDL Feb. 2007 164-167*

Samudra, G. S., see Ang, K.-W., *EDL April 2007 301-304*

Samudra, G. S., see Ang, K.-W., *EDL June 2007 509-512*

Samudra, G. S., see Lim, A. E.-J., *EDL June 2007 482-485*

Samudra, G. S., see Ang, K.-W., *EDL July 2007 609-612*

Samudra, G. S., see Tan, K.-M., *EDL Oct. 2007 905-908*

Samudra, G. S., see Ang, K.-W., *EDL Nov. 2007 996-999*

Samudra, G. S., see Liow, T.-Y., *EDL Nov. 2007 1014-1017*

Samudra, G., see Wong, H.-S., *EDL Dec. 2007 1102-1104*

San Andres, E., see Shickova, A., *EDL March 2007 242-244*

Sanaie, G., and Karim, K., On-Pixel Voltage-Controlled EDL Oscillator in Amorphous-Silicon Technology for Digital Imaging Applications; *EDL Jan. 2007 33-35*

Sano, M., see Ofuji, M., *EDL April 2007 273-275*

Sarkar, J., Dey, S., Shahrjerdi, D., and Banerjee, S. K., Vertical Flash Memory Cell With Nanocrystal Floating Gate for Ultradense Integration and Good Retention; *EDL May 2007 449-451*

Sarua, A., see Kuball, M., *EDL Feb. 2007 86-89*

Sasa, S., Hayafuji, T., Kawasaki, M., Koike, K., Yano, M., and Inoue, M., Improved Stability of High-Performance ZnO/ZnMgO Hetero-MISFETs; *EDL July 2007 543-545*

Satoh, M., see Nomoto, K., *EDL Nov. 2007 939-941*

Satoh, Y., see Kambayashi, H., *EDL Dec. 2007 1077-1079*

Schindler, M., see Abelein, U., *EDL Jan. 2007 65-67*

Schlosser, M., see Abelein, U., *EDL Jan. 2007 65-67*

Schmitt-Landsiedel, D., see Nirschl, Th., *EDL April 2007 315-315*

Schmitz, J., see Hoang, T., *EDL May 2007 383-385*

Schmitz, J., see van der Steen, J.-L. P. J., *EDL Sept. 2007 821-824*

Schneider, O., see Chaji, G. R., *EDL Dec. 2007 1108-1110*

Schram, T., see Ragnarsson, L.-A., *EDL June 2007 486-488*

Schram, T., see Yu, H. Y., *EDL July 2007 656-658*

Schrimpf, R. D., see Warren, K. M., *EDL Feb. 2007 180-182*

Schulman, J. N., see Su, N., *EDL May 2007 336-339*

Seacrist, M., see Huang, Y.-T., *EDL Sept. 2007 815-817*

Sekar, D. C., Dang, B., Davis, J. A., and Meindl, J. D., Electromigration Resistant Power Delivery Systems; *EDL Aug. 2007 767-769*

Sekigawa, T., see Endo, K., *EDL May 2007 452-454*

Selmi, L., see Zilli, M., *EDL Nov. 2007 1036-1039*

Severi, S., Pawlak, B. J., Duffy, R., Augendre, E., Henson, K., Lindsay, R., and De Meyer, K., Arsenic Junction Thermal Stability and High-Dose Boron-Pocket Activation During SPER in nMOS Transistors; *EDL March 2007 198-200*

Shahrjerdi, D., see Sarkar, J., *EDL May 2007 449-451*

Shahrjerdi, D., Garcia-Gutierrez, D. I., and Banerjee, S. K., Fabrication of Ni Nanocrystal Flash Memories Using a Polymeric Self-Assembly Approach; *EDL Sept. 2007 793-796*

Shan, X., see Li, Y., *EDL July 2007 622-624*

Shao, I., see Pan, J., *EDL Aug. 2007 691-693*

Shapira, Y., see Stopel, A., *EDL May 2007 357-359*

Shei, S.-C., Sheu, J.-K., and Shen, C.-F., Improved Reliability and ESD Characteristics of Flip-Chip GaN-Based EDLs With Internal Inverse-Parallel Protection Diodes; *EDL May 2007 346-349*

- Shen, C., *see* Chen, J., *EDL Oct. 2007 862-864*
- Shen, C.-F., *see* Shei, S.-C., *EDL May 2007 346-349*
- Shen, L., *see* Poblenz, C., *EDL Nov. 2007 945-947*
- Shen, T., *see* Xuan, Y., *EDL Nov. 2007 935-938*
- Shen, Z. J., *see* Fu, Y., *EDL Feb. 2007 174-176*
- Sheng, K., *see* Zhang, Y., *EDL May 2007 404-407*
- Sheu, J.-K., *see* Shei, S.-C., *EDL May 2007 346-349*
- Sheu, Y. M., *see* Cheng, C. Y., *EDL May 2007 408-411*
- Sheu, Y.-M., *see* Wang, J.-S., *EDL Nov. 2007 1040-1043*
- Shi, J., *see* Sun, S., *EDL March 2007 220-222*
- Shi, L., *see* Sun, W., *EDL July 2007 631-633*
- Shi, L., *see* Sun, W., *EDL Dec. 2007 1135-1137*
- Shi, T., *see* Zhao, F., *EDL May 2007 398-400*
- Shickova, A., *see* Simoen, E., *EDL Nov. 2007 987-989*
- Shickova, A., Kaczer, B., Verheyen, P., Eneman, G., San Andres, E., Jurczak, M., Absil, P., Maes, H., and Groeseneken, G., Negligible Effect of Process-Induced Strain on Intrinsic NBTI Behavior; *EDL March 2007 242-244*
- Shieh, J.-M., *see* Lin, Y.-T., *EDL Sept. 2007 790-792*
- Shigekawa, N., Nishimura, K., Suemitsu, T., Yokoyama, H., and Hohkawa, K., SAW Filters Composed of Interdigital Schottky and Ohmic Contacts on AlGaIn/GaN Heterostructures; *EDL Feb. 2007 90-92*
- Shih, C.-H., *see* Wang, J.-S., *EDL Nov. 2007 1040-1043*
- Shimizu, H., *see* Ofuji, M., *EDL April 2007 273-275*
- Shin, H., *see* Jung, K.-D., *EDL March 2007 204-206*
- Shin, H. S., *see* Jeong, J. K., *EDL May 2007 389-391*
- Shin, H., *see* Kang, I. M., *EDL May 2007 425-427*
- Shin, K., *see* Padilla, A., *EDL June 2007 502-505*
- Shin, K.-S., Paek, K.-K., Park, J.-H., Kim, T.-S., Ju, B.-K., and Kang, J. Y., Parasitic Bipolar Junction Transistors in a Floating-Gate MOSFET for Fluorescence Detection; *EDL July 2007 581-583*
- Shin, M. W., *see* Kim, L., *EDL July 2007 578-580*
- Shiraishi, K., *see* Umezawa, N., *EDL May 2007 363-365*
- Shiu, J.-Y., Huang, J.-C., Desmaris, V., Chang, C.-T., Lu, C.-Y., Kumakura, K., Makimoto, T., Zirath, H., Rorsman, N., and Chang, E. Y., Oxygen Ion Implantation Isolation Planar Process for AlGaIn/GaN HEMTs; *EDL June 2007 476-478*
- Shiu, K. T., *see* Sun, Y., *EDL June 2007 473-475*
- Shur, M. S., *see* Koudymov, A., *EDL May 2007 332-335*
- Shy, J.-H., *see* Chen, S.-C., *EDL Sept. 2007 809-811*
- Sibaja-Hernandez, A., *see* Choi, L. J., *EDL April 2007 270-272*
- Sierawski, B. D., *see* Warren, K. M., *EDL Feb. 2007 180-182*
- Silva, S. R. P., *see* Guo, X., *EDL Aug. 2007 710-712*
- Silva, S. R. P., *see* Guo, X., *EDL Oct. 2007 887-889*
- Simin, G., *see* Koudymov, A., *EDL Jan. 2007 5-7*
- Simin, G., *see* Adivarahan, V., *EDL March 2007 192-194*
- Simin, G., *see* Koudymov, A., *EDL May 2007 332-335*
- Simin, G., *see* Tipirneni, N., *EDL Sept. 2007 784-786*
- Simin, G., and Yang, Z.-J., RF-Enhanced Contacts to Wide-Bandgap Devices; *EDL Jan. 2007 2-4*
- Simoen, E., *see* Guo, W., *EDL April 2007 288-291*
- Simoen, E., Claeys, C., Chung, T. M., Flandre, D., and Raskin, J.-P., On the Origin of the Excess Low-Frequency Noise in Graded-Channel Silicon-on-Insulator nMOSFETs; *EDL Oct. 2007 919-921*
- Simoen, E., Verheyen, P., Shickova, A., Loo, R., and Claeys, C., On the Low-Frequency Noise of pMOSFETs With Embedded SiGe Source/Drain and Fully Silicided Metal Gate; *EDL Nov. 2007 987-989*
- Singanamalla, R., *see* Yu, H. Y., *EDL Feb. 2007 154-156*
- Singanamalla, R., *see* Yu, H. Y., *EDL July 2007 656-658*
- Singanamalla, R., *see* Veloso, A., *EDL Nov. 2007 980-983*
- Singanamalla, R., Yu, H. Y., Van Daele, B., Kubicek, S., and De Meyer, K., Effective Work-Function Modulation by Aluminum-Ion Implantation for Metal-Gate Technology (Poly-Si/TiN/SiO₂); *EDL Dec. 2007 1089-1091*
- Singh, N., *see* Fang, W. W., *EDL March 2007 211-213*
- Singh, N., *see* Rustagi, S. C., *EDL Oct. 2007 909-912*
- Singh, N., *see* Rustagi, S. C., *EDL Nov. 2007 1021-1024*
- Singh, N., Fang, W. W., Rustagi, S. C., Budharaju, K. D., Teo, S. H. G., Mohanraj, S., Lo, G. Q., Balasubramanian, N., and Kwong, D.-L., Observation of Metal-Layer Stress on Si Nanowires in Gate-All-Around High- κ /Metal-Gate Device Structures; *EDL July 2007 558-561*
- Sivorthaman, S., *see* Farrokhi-Baroughi, M., *EDL July 2007 575-577*
- Skotnicki, T., *see* Cornu-Frueux, F., *EDL June 2007 523-526*
- Smit, G. D. J., *see* van der Steen, J.-L. P. J., *EDL Sept. 2007 821-824*
- Solodky, S., *see* Stopel, A., *EDL May 2007 357-359*
- Song, C. K., *see* Kim, T. H., *EDL Oct. 2007 874-876*
- Song, D., Liu, J., Cheng, Z., Tang, W. C. W., Lau, K. M., and Chen, K. J., Normally Off AlGaIn/GaN Low-Density Drain HEMT (LDD-HEMT) With Enhanced Breakdown Voltage and Reduced Current Collapse; *EDL March 2007 189-191*
- Song, G., Ali, M. Y., and Tao, M., A High Schottky-Barrier of 1.1 eV Between Al and S-Passivated p-Type Si(100) Surface; *EDL Jan. 2007 71-73*
- Song, J. F., *see* Loh, W. Y., *EDL Nov. 2007 984-986*
- Song, J.-I., *see* Kim, T.-W., *EDL Dec. 2007 1086-1088*
- Song, Y., Ling, Q. D., Lim, S. L., Teo, E. Y. H., Tan, Y. P., Li, L., Kang, E. T., Chan, D. S. H., and Zhu, C., Electrically Bistable Thin-Film Device Based on PVK and GNPs Polymer Material; *EDL Feb. 2007 107-110*
- Sousa, M., *see* Sun, Y., *EDL June 2007 473-475*
- Speck, J. S., *see* Chu, R., *EDL Sept. 2007 781-783*
- Speck, J. S., *see* Poblenz, C., *EDL Nov. 2007 945-947*
- Spinelli, A. S., *see* Compagnoni, C. M., *EDL July 2007 628-630*
- Srinidhi, E. R., Jarndal, A., and Kompas, G., A New Method for Identification and Minimization of Distortion Sources in GaN HEMT Devices Based on Volterra Series Analysis; *EDL May 2007 343-345*
- Stager, C., *see* Huang, Y.-T., *EDL Sept. 2007 815-817*
- Stake, J., *see* Vukusic, J., *EDL May 2007 340-342*
- Stanley, C. R., *see* Khalid, A., *EDL Oct. 2007 849-851*
- Stopel, A., Khramtsov, A., Solodky, S., Fainbrun, A., and Shapira, Y., Direct Monitoring of RF Overstress in High-Power Transistors and Amplifiers; *EDL May 2007 357-359*
- Sturm, J. C., *see* Kattamis, A. Z., *EDL July 2007 606-608*
- Sturm, J. C., *see* Cherenack, K. H., *EDL Nov. 2007 1004-1006*
- Su, K.-H., Hsu, W.-C., Lee, C.-S., Wu, T.-Y., Wu, Y.-H., Chang, L., Hsiao, R.-S., Chen, J.-F., and Chi, T.-W., A Novel Dilute Antimony Channel In_{0.2}Ga_{0.8}AsSb/GaAs HEMT; *EDL Feb. 2007 96-99*
- Su, M., *see* Zhang, Y., *EDL May 2007 404-407*
- Su, N. C., *see* Cheng, C. F., *EDL Dec. 2007 1092-1094*
- Su, N., Zhang, Z., Schulman, J. N., and Fay, P., Temperature Dependence of High Frequency and Noise Performance of Sb-Heterostructure Millimeter-Wave Detectors; *EDL May 2007 336-339*
- Su, P., *see* Wang, J.-S., *EDL Nov. 2007 1040-1043*
- Su, P., and Kuo, J. J.-Y., On the Enhanced Impact Ionization in Uniaxial Strained p-MOSFETs; *EDL July 2007 649-651*
- Suemitsu, T., *see* Shigekawa, N., *EDL Feb. 2007 90-92*
- Suemitsu, T., Yokoyama, H., Sugiyama, H., and Tokumitsu, M., Enhanced Gate Swing in InP HEMTs With High Threshold Voltage by Means of InAlAsSb Barrier; *EDL Aug. 2007 669-671*
- Sugawara, Y., Uraoka, Y., Yano, H., Hatayama, T., Fuyuki, T., and Mimura, A., Crystallization of Double-Layered Silicon Thin Films by Solid Green Laser Annealing for High-Performance Thin-Film Transistors; *EDL May 2007 395-397*
- Sugii, N., *see* Ohtou, T., *EDL Aug. 2007 740-742*
- Sugiyama, H., *see* Suemitsu, T., *EDL Aug. 2007 669-671*
- Suh, C. S., *see* Chu, R., *EDL Sept. 2007 781-783*
- Suh, C. S., *see* Poblenz, C., *EDL Nov. 2007 945-947*
- Suh, K., *see* Park, M., *EDL Aug. 2007 750-752*
- Suh, M. C., *see* Kim, T. H., *EDL Oct. 2007 874-876*
- Sui, Y., Wang, X., and Cooper, J. A., High-Voltage Self-Aligned p-Channel DMOS-IGBTs in 4H-SiC; *EDL Aug. 2007 728-730*
- Suk, S. D., *see* Cho, K. H., *EDL Dec. 2007 1129-1131*
- Sulima, T., *see* Abelein, U., *EDL Jan. 2007 65-67*
- Sun, H. F., Alt, A. R., and Bolognesi, C. R., Submicrometer Copper T-Gate AlGaIn/GaN HFETs: The Gate Metal Stack Effect; *EDL May 2007 350-353*
- Sun, H.-J., *see* Jeong, Y. H., *EDL Jan. 2007 17-20*
- Sun, M., and Zhang, Y. P., 100-GHz Quasi-Yagi Antenna in Silicon Technology; *EDL May 2007 455-457*
- Sun, S., Shi, J., Zhu, L., Rustagi, S. C., and Mouthaan, K., Millimeter-Wave Bandpass Filters by Standard 0.18- μ m CMOS Technology; *EDL March 2007 220-222*
- Sun, W., Wu, H., Shi, L., Yi, Y., and Li, H., On-Resistance Degradations for Different Stress Conditions in High-Voltage pEDLMOS Transistor With Thick Gate Oxide; *EDL July 2007 631-633*
- Sun, W., Yi, Y., Li, H., and Shi, L., A Novel Latch-Up Protection for Bulk-Silicon Scan Driver ICs of Shadow-Mask Plasma-Display Panel; *EDL Dec. 2007 1135-1137*
- Sun, Y., *see* Felbinger, J. G., *EDL Nov. 2007 948-950*
- Sun, Y. Y., *see* Wang, X. P., *EDL April 2007 258-260*
- Sun, Y., Kiewra, E. W., Koester, S. J., Ruiz, N., Callegari, A., Fogel, K. E., Sadana, D. K., Fompeyrine, J., Webb, D. J., Locquet, J.-P., Sousa, M., Germann, R., Shiu, K. T., and Forrest, S. R., Enhancement-Mode Buried-

- Channel $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ MOSFETs With High- κ Gate Dielectrics; *EDL June 2007 473-475*
- Sundaram, K. B.**, see Vijayakumar, A., *EDL Aug. 2007 713-715*
- Sung, C.-Y.**, see Pan, J., *EDL Aug. 2007 691-693*
- Surdeanu, R.**, see Masahara, M., *EDL March 2007 217-219*
- Suthram, S.**, Ziegert, J. C., Nishida, T., and Thompson, S. E., Piezoresistance Coefficients of (100) Silicon nMOSFETs Measured at Low and High (~ 1.5 GPa) Channel Stress; *EDL Jan. 2007 58-61*
- Suzuki, E.**, see Endo, K., *EDL May 2007 452-454*
- Suzuki, E.**, see Liu, Y., *EDL June 2007 517-519*
- Suzuki, E.**, see Endo, K., *EDL Dec. 2007 1123-1125*
- Sveinbjornsson, E. O.**, see Lee, H.-S., *EDL Nov. 2007 1007-1009*
- Swerts, J.**, see Ragnarsson, L.-A., *EDL June 2007 486-488*
- Sze, S. M.**, see Chen, S.-C., *EDL Sept. 2007 809-811*

T

- Tajima, T.**, see Nomoto, K., *EDL Nov. 2007 939-941*
- Takahashi, Y.**, see Nishiguchi, K., *EDL Jan. 2007 48-50*
- Tan, K.-M.**, see Lee, R. T. P., *EDL Feb. 2007 164-167*
- Tan, K.-M.**, see Liow, T.-Y., *EDL Nov. 2007 1014-1017*
- Tan, K.-M.**, Liow, T.-Y., Lee, R. T. P., Hoe, K. M., Tung, C.-H., Balasubramanian, N., Samudra, G. S., and Yeo, Y.-C., Strained p-Channel FinFETs With Extended Π -Shaped Silicon-Germanium Source and Drain Stressors; *EDL Oct. 2007 905-908*
- Tan, Y. P.**, see Song, Y., *EDL Feb. 2007 107-110*
- Tang, C. W.**, see Cai, Y., *EDL May 2007 328-331*
- Tang, C. W.**, see Zhou, W., *EDL July 2007 539-542*
- Tang, W. C. W.**, see Song, D., *EDL March 2007 189-191*
- Tang, X.**, see Luo, X., *EDL May 2007 422-424*
- Tao, H. J.**, see Yen, F. Y., *EDL March 2007 201-203*
- Tao, H. J.**, see Wu, C. H., *EDL April 2007 292-294*
- Tao, K.**, see Li, R., *EDL May 2007 360-362*
- Tao, M.**, see Song, G., *EDL Jan. 2007 71-73*
- Tao, N. G.**, see Zhou, W., *EDL July 2007 539-542*
- Tassis, D. H.**, see Hatzopoulos, A. T., *EDL Sept. 2007 803-805*
- Taur, Y.**, Changes to the Editorial Board; *EDL Feb. 2007 81-81*
- Taur, Y.**, Changes to the Editorial Board; *EDL April 2007 257-257*
- Taur, Y.**, Changes in the Editorial Board; *EDL May 2007 327-327*
- Taur, Y.**, Kudos to Our Reviewers; *EDL Dec. 2007 1061-1061*
- Taylor, W. J.**, see Winstead, B., *EDL Aug. 2007 719-721*
- Tedde, S.**, Zaus, E. S., Furst, J., Henseler, D., and Lugli, P., Active Pixel Concept Combined With Organic Photodiode for Imaging Devices; *EDL Oct. 2007 893-895*
- Tegude, F. J.**, see Do, Q.-T., *EDL Aug. 2007 682-684*
- Tekleab, D.**, see Winstead, B., *EDL Aug. 2007 719-721*
- Templier, F.**, see Hatzopoulos, A. T., *EDL Sept. 2007 803-805*
- Teo, E. Y. H.**, see Song, Y., *EDL Feb. 2007 107-110*
- Teo, S. H. G.**, see Singh, N., *EDL July 2007 558-561*
- Teo, S. H. G.**, see Rustagi, S. C., *EDL Nov. 2007 1021-1024*
- Thayne, I. G.**, see Khalid, A., *EDL Oct. 2007 849-851*
- Thayne, I. G.**, see Hill, R. J. W., *EDL Dec. 2007 1080-1082*
- Thompson, S. E.**, see Suthram, S., *EDL Jan. 2007 58-61*
- Thoms, S.**, see Hill, R. J. W., *EDL Dec. 2007 1080-1082*
- Thomson, D. B.**, see Jessen, G. H., *EDL May 2007 354-356*
- Tipirneni, N.**, Adivarahan, V., Simin, G., and Khan, A., Silicon Dioxide-Encapsulated High-Voltage AlGaIn/GaN HFETs for Power-Switching Applications; *EDL Sept. 2007 784-786*
- Tittonen, I.**, see Koskenvuori, M., *EDL Nov. 2007 970-972*
- Tiwari, S.**, see Kim, S., *EDL Aug. 2007 706-709*
- Tiwari, S.**, see Lin, H., *EDL May 2007 412-415*
- Tiwari, S. P.**, Namdas, E. B., Ramgopal Rao, V., Fichou, D., and Mhaisalkar, S. G., Solution-Processed n-Type Organic Field-Effect Transistors With High ON/OFF Current Ratios Based on Fullerene Derivatives; *EDL Oct. 2007 880-883*
- Tiwari, S.**, see Lin, H., *EDL June 2007 506-508*
- Todi, R. M.**, see Guo, W., *EDL April 2007 288-291*
- Todi, R. M.**, see Vijayakumar, A., *EDL Aug. 2007 713-715*
- Tokumitsu, M.**, see Suemitsu, T., *EDL Aug. 2007 669-671*
- Topol, A.**, see Pan, J., *EDL Aug. 2007 691-693*
- Torii, K.**, see Umezawa, N., *EDL May 2007 363-365*
- Torvik, K.**, see Zhao, F., *EDL May 2007 398-400*
- Trivedi, V. P.**, see Fossum, J. G., *EDL June 2007 513-516*

+ Check author entry for coauthors

- Trojman, L.**, see Aoulaiche, M., *EDL July 2007 613-615*
- Trzcinski, R.**, see Kim, D., *EDL June 2007 520-522*
- Trzcinski, R.**, see Kim, D., *EDL July 2007 616-618*
- Tsai, C.-C.**, Chen, H.-H., Chen, B.-T., and Cheng, H.-C., High-Performance Self-Aligned Bottom-Gate Low-Temperature Poly-Silicon Thin-Film Transistors With Excimer Laser Crystallization; *EDL July 2007 599-602*
- Tsai, C.-C.**, Wei, K.-F., Lee, Y.-J., Chen, H.-H., Wang, J.-L., Lee, I.-C., and Cheng, H.-C., High-Performance Short-Channel Double-Gate Low-Temperature Polysilicon Thin-Film Transistors Using Excimer Laser Crystallization; *EDL Nov. 2007 1010-1013*
- Tsai, C.-L.**, see Lee, F.-M., *EDL Feb. 2007 120-122*
- Tsai, C.-T.**, Liu, P.-T., Chang, T.-C., Wang, C.-W., Yang, P.-Y., and Yeh, F.-S., Low-Temperature Passivation of Amorphous-Silicon Thin-Film Transistors With Supercritical Fluids; *EDL July 2007 584-586*
- Tsai, M.-J.**, see Chao, D.-S., *EDL Oct. 2007 871-873*
- Tsai, P.-H.**, see Lu, C.-Y., *EDL May 2007 432-435*
- Tsai, T.-T.**, see Lin, C.-L., *EDL June 2007 489-491*
- Tseng, B.-H.**, see Chen, S.-C., *EDL Sept. 2007 809-811*
- Tseng, C.-W.**, see Hsu, H.-M., *EDL Nov. 2007 1029-1032*
- Tseng, H.-H.**, see Joshi, S., *EDL April 2007 308-311*
- Tseng, H.-H.**, see Oh, J., *EDL Nov. 2007 1044-1046*
- Tseng, T.-Y.**, see Lin, C.-Y., *EDL May 2007 366-368*
- Tsetseris, L.**, see Hadjisavvas, G., *EDL Nov. 2007 1018-1020*
- Tsuda, K.**, see Saito, W., *EDL Aug. 2007 676-678*
- Tsukada, J.**, see Endo, K., *EDL May 2007 452-454*
- Tsukada, J.**, see Liu, Y., *EDL June 2007 517-519*
- Tsukada, J.**, see Endo, K., *EDL Dec. 2007 1123-1125*
- Tung, C. H.**, see Lim, A. E.-J., *EDL June 2007 482-485*
- Tung, C. H.**, see Rustagi, S. C., *EDL Nov. 2007 1021-1024*
- Tung, C.-H.**, see Ang, K.-W., *EDL April 2007 301-304*
- Tung, C.-H.**, see Ang, K.-W., *EDL June 2007 509-512*
- Tung, C.-H.**, see Ang, K.-W., *EDL July 2007 609-612*
- Tung, C.-H.**, see Tan, K.-M., *EDL Oct. 2007 905-908*
- Tung, C.-H.**, see Liow, T.-Y., *EDL Nov. 2007 1014-1017*

U

- Umezawa, N.**, Shiraishi, K., Torii, K., Boero, M., Chikyow, T., Watanabe, H., Yamabe, K., Ohno, T., Yamada, K., and Nara, Y., Role of Nitrogen Atoms in Reduction of Electron Charge Traps in Hf-Based High- κ Dielectrics; *EDL May 2007 363-365*
- Uraoka, Y.**, see Sugawara, Y., *EDL May 2007 395-397*
- Uren, M. J.**, see Kuball, M., *EDL Feb. 2007 86-89*
- Uyeda, J.**, see Mei, X. B., *EDL June 2007 470-472*

V

- Van Daele, B.**, see Singanamalla, R., *EDL Dec. 2007 1089-1091*
- Van Delden, J. S.**, see Lin, H., *EDL June 2007 506-508*
- Van Duuren, M.**, see Duane, R., *EDL May 2007 440-442*
- Van Elshocht, S.**, see Yu, H. Y., *EDL July 2007 656-658*
- Van Elshocht, S.**, see Veloso, A., *EDL Nov. 2007 980-983*
- Van Gestel, D.**, see Carnel, L., *EDL Oct. 2007 899-901*
- Van Houdt, J.**, see Furnemont, A., *EDL April 2007 276-278*
- Van Huylenbroeck, S.**, see Choi, L. J., *EDL April 2007 270-272*
- Van den Bosch, G.**, see Masahara, M., *EDL March 2007 217-219*
- Van der Zanden, K.**, see Furnemont, A., *EDL April 2007 276-278*
- Vanfleteren, J.**, see Brosteaux, D., *EDL July 2007 552-554*
- Vanhaeren, D.**, see Carnel, L., *EDL Oct. 2007 899-901*
- Vanmeerbeek, P.**, see Bakeroot, B., *EDL May 2007 416-418*
- Van Noort, W. D.**, see Choi, L. J., *EDL April 2007 270-272*
- Van der Steen, J.-L. P. J.**, Hueting, R. J. E., Smit, G. D. J., Hoang, T., Holleman, J., and Schmitz, J., Valence Band Offset Measurements on Thin Silicon-on-Insulator MOSFETs; *EDL Sept. 2007 821-824*
- Van der Toorn, R.**, Threshold Current for the Onset of Kirk Effect in Bipolar Transistors With a Fully Depleted Nonuniformly Doped Collector; *EDL Jan. 2007 54-57*
- Varadan, V. K.**, see Ji, T., *EDL Dec. 2007 1105-1107*
- Veloso, A.**, see Chang, S. Z., *EDL July 2007 634-636*
- Veloso, A.**, see Yu, H. Y., *EDL Nov. 2007 957-959*
- Veloso, A.**, Yu, H. Y., Chang, S. Z., Adelman, C., Onsia, B., Brus, S., Demand, M., Lauwers, A., O'Sullivan, B. J., Singanamalla, R., Pourtois, G., Lehnen, P., Van Elshocht, S., De Meyer, K., Jurczak, M., Absil, P. P., and

- Biesemans, S., Achieving Low- V_T Ni-FUSI CMOS by Ultra-Thin Dy_2O_3 Capping of Hafnium Silicate Dielectrics; *EDL Nov. 2007* 980-983
- Ventrice, D., Fantini, P., Redaelli, A., Pirovano, A., Benvenuti, A., and Pelizzier, F., A Phase Change Memory Compact Model for Multilevel Applications; *EDL Nov. 2007* 973-975
- Verheyen, P., see Shickova, A., *EDL March 2007* 242-244
- Verheyen, P., see Simoen, E., *EDL Nov. 2007* 987-989
- Vernier, P. T., see Marshall, J. C., *EDL Nov. 2007* 960-963
- Verret, E., see Winstead, B., *EDL Aug. 2007* 719-721
- Via, G. D., see Jessen, G. H., *EDL May 2007* 354-356
- Vijayakumar, A., Todi, R. M., and Sundaram, K. B., Amorphous-SiCBN-Based Metal-Semiconductor-Metal Photodetector for High-Temperature Applications; *EDL Aug. 2007* 713-715
- Visconti, A., see Fantini, P., *EDL Dec. 2007* 1114-1116
- Volakis, J. L., see Chow, L. L. W., *EDL June 2007* 479-481
- Vrancken, C., see Masahara, M., *EDL March 2007* 217-219
- Vukusic, J., Bryllert, T., Arezoo Emadi, T., Sadeghi, M., and Stake, J., A 0.2-W Heterostructure Barrier Varactor Frequency Tripler at 113 GHz; *EDL May 2007* 340-342
- W**
- Wagner, S., see Kattamis, A. Z., *EDL July 2007* 606-608
- Wagner, S., see Cherenack, K. H., *EDL Nov. 2007* 1004-1006
- Wallis, D. J., see Kuball, M., *EDL Feb. 2007* 86-89
- Wan, C., see Ang, K.-W., *EDL Nov. 2007* 996-999
- Wang, A., see Yang, C., *EDL July 2007* 652-655
- Wang, C., see Li, C., *EDL Aug. 2007* 763-766
- Wang, C. K., see Chiou, Y. Z., *EDL April 2007* 264-266
- Wang, C. S., see Lian, C., *EDL Jan. 2007* 8-10
- Wang, C. X., see Koudymov, A., *EDL Jan. 2007* 5-7
- Wang, C.-D., see Li, R., *EDL May 2007* 360-362
- Wang, C.-W., see Tsai, C.-T., *EDL July 2007* 584-586
- Wang, H., see Lew, K. L., *EDL Dec. 2007* 1083-1085
- Wang, J., see Mei, X. B., *EDL June 2007* 470-472
- Wang, J.-C., see Wu, W.-C., *EDL March 2007* 214-216
- Wang, J.-L., see Tsai, C.-C., *EDL Nov. 2007* 1010-1013
- Wang, J.-S., Chen, W. P.-N., Shih, C.-H., Lien, C., Su, P., Sheu, Y.-M., Chao, D. Y.-S., and Goto, K.-I., Mobility Modeling and Its Extraction Technique for Manufacturing Strained-Si MOSFETs; *EDL Nov. 2007* 1040-1043
- Wang, J., see Loh, W. Y., *EDL Nov. 2007* 984-986
- Wang, J., see Xu, C., *EDL Nov. 2007* 942-944
- Wang, S., see Rustagi, S. C., *EDL Oct. 2007* 909-912
- Wang, S. J., see Wu, C. H., *EDL April 2007* 292-294
- Wang, S. J., see Cheng, C. F., *EDL Dec. 2007* 1092-1094
- Wang, S.-C., see Lu, T.-C., *EDL Oct. 2007* 884-886
- Wang, S.-D., see Chen, C.-Y., *EDL May 2007* 392-394
- Wang, S.-J., see Ma, M.-W., *EDL March 2007* 238-241
- Wang, S.-W., see Lin, D.-W., *EDL Dec. 2007* 1132-1134
- Wang, S.-Y., see Chen, S.-H., *EDL Aug. 2007* 679-681
- Wang, T., see Liao, Y.-Y., *EDL Sept. 2007* 828-830
- Wang, T.-K., see Lu, C.-Y., *EDL May 2007* 432-435
- Wang, W., see Haruehanroengra, S., *EDL Aug. 2007* 756-759
- Wang, X., see Sui, Y., *EDL Aug. 2007* 728-730
- Wang, X. P., see Wu, C. H., *EDL April 2007* 292-294
- Wang, X. P., see Lim, A. E.-J., *EDL June 2007* 482-485
- Wang, X. P., see Chen, J., *EDL Oct. 2007* 862-864
- Wang, X. P., Yu, H. Y., Li, M.-F., Zhu, C. X., Biesemans, S., Chin, A., Sun, Y. Y., Feng, Y. P., Lim, A., Yeo, Y.-C., Loh, W. Y., Lo, G. Q., and Kwong, D.-L., Wide V_{fb} and V_{th} Tunability for Metal-Gated MOS Devices With HfLaO Gate Dielectrics; *EDL April 2007* 258-260
- Wang, X., see Huang, F., *EDL Nov. 2007* 1025-1028
- Wang, Y., see Li, Y., *EDL July 2007* 622-624
- Wang, Y. P., Wu, S. L., and Chang, S. J., Low-Frequency Noise Characteristics in Strained-Si nMOSFETs; *EDL Jan. 2007* 36-38
- Wang, Y., Cheung, K. P., Choi, R., Brown, G. A., and Lee, B.-H., Time-Domain-Reflectometry for Capacitance-Voltage Measurement With Very High Leakage Current; *EDL Jan. 2007* 51-53
- Wang, Y., Cheung, K. P., Choi, R., Brown, G. A., and Lee, B.-H., Error and Correction in Capacitance-Voltage Measurement Due to the Presence of Source and Drain; *EDL July 2007* 640-642
- Wang, Y., Cheung, K. P., Choi, R., Brown, G. A., and Lee, B.-H., Accurate Series-Resistance Extraction From Capacitor Using Time Domain Reflectometry; *EDL April 2007* 279-281
- Wang, Y., see Li, C., *EDL Aug. 2007* 763-766
- Wang, Z., Griffin, P. B., McVittie, J., Wong, S., McIntyre, P. C., and Nishi, Y., Resistive Switching Mechanism in $Zn_xCd_{1-x}S$ Nonvolatile Memory Devices; *EDL Jan. 2007* 14-16
- Ward, C. S., see Jessen, G. H., *EDL May 2007* 354-356
- Warren, K. M., Sierawski, B. D., Weller, R. A., Reed, R. A., Mendenhall, M. H., Pellish, J. A., Schrimpf, R. D., Massengill, L. W., Porter, M. E., and Wilkinson, J. D., Predicting Thermal Neutron-Induced Soft Errors in Static Memories Using TCAD and Physics-Based Monte Carlo Simulation Tools; *EDL Feb. 2007* 180-182
- Wasserbauer, J., see Felbinger, J. G., *EDL Nov. 2007* 948-950
- Watanabe, H., see Umezawa, N., *EDL May 2007* 363-365
- Webb, D. J., see Sun, Y., *EDL June 2007* 473-475
- Weerakoon, P., see Culurciello, E., *EDL Feb. 2007* 117-119
- Wei, C. S., see Chen, Y. H., *EDL Dec. 2007* 1111-1113
- Wei, K.-F., see Tsai, C.-C., *EDL Nov. 2007* 1010-1013
- Wei, L., Zhang, X., Lou, C., and Zhu, Z., An Improved Planar Triode With ZnO Nanopin Field Emitters; *EDL Aug. 2007* 688-690
- Weis, M., see Nirschl, Th., *EDL April 2007* 315-315
- Weller, R. A., see Warren, K. M., *EDL Feb. 2007* 180-182
- Wen, C. P., see Xu, C., *EDL Nov. 2007* 942-944
- Werner, A., see Chaji, G. R., *EDL Dec. 2007* 1108-1110
- Wicaksono, S., see Lew, K. L., *EDL Dec. 2007* 1083-1085
- Wilkinson, J. D., see Warren, K. M., *EDL Feb. 2007* 180-182
- Wilks, B., see Huang, Y.-T., *EDL Sept. 2007* 815-817
- Winstead, B., Taylor, W. J., Verret, E., Loiko, K., Tekleab, D., Capasso, C., Foisy, M., and Samavedam, S. B., SiGe-Channel Confinement Effects for Short-Channel PFETs With Nonbandedge Gate Workfunctions; *EDL Aug. 2007* 719-721
- Wise, R., see Huang, Y.-T., *EDL Sept. 2007* 815-817
- Wise, R., see Lin, C.-T., *EDL Sept. 2007* 831-833
- Witters, L., see Masahara, M., *EDL March 2007* 217-219
- Wong, H.-S., Chan, L., Samudra, G., and Yeo, Y.-C., Sub-0.1-eV Effective Schottky-Barrier Height for NiSi on n-Type Si (100) Using Antimony Segregation; *EDL Aug. 2007* 703-705
- Wong, H.-S., Chan, L., Samudra, G., and Yeo, Y.-C., Effective Schottky Barrier Height Reduction Using Sulfur or Selenium at the NiSi/n-Si (100) Interface for Low Resistance Contacts; *EDL Dec. 2007* 1102-1104
- Wong, H.-S.P., see Kim, S., *EDL Aug. 2007* 697-699
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 Yu, H. P., Pey, K. L., Choi, W. K., Dawood, M. K., Chew, H.G., Antoniadis, D. A., Fitzgerald, E. A., and Chi, D. Z., The Effect of an Yttrium Interlayer on a Nitrogenated Metal Gate Workfunction in SiO₂/HfO₂; *EDL Dec. 2007 1098-1101*
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Analytical models

Effect of Load Distribution on the Voltage Drop and the Luminance Variation in an AC-PDP. *Kim, J.-S.*, +, *EDL Oct. 2007 896-898*

Annealing

Effect of F₂ Postmetallization Annealing on the Electrical and Reliability Characteristics of HfSiO Gate Dielectric. *Chang, M.*, +, *EDL Jan. 2007 21-23*
 A Novel Approach in Separating the Roles of Electrons and Holes in Causing Degradation in Hf-Based MOSFET Devices by Using Stress-Anneal Technique. *Akbar, M. S.*, +, *EDL Feb. 2007 132-134*
 Ar Annealing for Suppression of Gate Oxide Thinning at Shallow Trench Isolation Edge. *Ohashi, T.*, +, *EDL July 2007 562-564*
 Effect of Gate Sinking on the Device Performance of the InGaP/AlGaAs/InGaAs Enhancement-Mode PHEMT. *Chu, L. H.*, +, *EDL Feb. 2007 82-85*
 Effects of Sulfur Passivation on Germanium MOS Capacitors With HfON Gate Dielectric. *Xie, R.*, +, *EDL Nov. 2007 976-979*
 Good High-Temperature Stability of TiN/Al₂O₃/WN/TiN Capacitors. *Pan, T.-M.*, +, *EDL Nov. 2007 954-956*
 High- κ Al₂O₃-HfTiO Nanolaminates With Less Than 0.8-nm Equivalent Oxide Thickness. *Mikhelashvili, V.*, +, *EDL Jan. 2007 24-26*
 Metal-Oxide-High- κ Dielectric-Oxide-Semiconductor (MOHOS) Capacitors and Field-Effect Transistors for Memory Applications. *Hsu, H.*, +, *EDL Nov. 2007 964-966*
 NMOS Compatible Work Function of TaN Metal Gate With Erbium-Oxide-Doped Hafnium Oxide Gate Dielectric. *Chen, J.*, +, *EDL Oct. 2007 862-864*
 Nitrogen Incorporation in HfSiO(N)/TaN Gate Stacks: Impact on Performances and NBTI. *Aoulaiche, M.*, +, *EDL July 2007 613-615*
 Schottky-Barrier Height Tuning by Means of Ion Implantation Into Preformed Silicide Films Followed by Drive-In Anneal. *Zhang, Z.*, +, *EDL July 2007 565-568*
 The Investigation of Post-Annealing-Induced Defects Behavior on 90-nm In Halo nMOSFETs With Low-Frequency Noise and Charge-Pumping Measuring. *Lai, C.-M.*, +, *EDL Feb. 2007 142-144*
 The Preparation of Nanocrystalline Silicon by Plasma-Enhanced Hydrogenation for the Fabrication of Light-Emitting Diodes. *Jamei, M.*, +, *EDL March 2007 207-210*
 Threshold Voltage Shift Due to Mechanical Stress-Enhanced Plasma Process-Induced Damage in 0.13- μ m pMOSFET. *Li, R.*, +, *EDL May 2007 360-362*

Trigate FET Device Characteristics Improvement Using a Hydrogen Anneal Process With a Novel Hard Mask Approach. *Zaman, R. J.*, +, *EDL Oct. 2007 916-918*

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Sub-0.1-eV Effective Schottky-Barrier Height for NiSi on n-Type Si (100) Using Antimony Segregation. *Wong, H.-S.*, +, *EDL Aug. 2007 703-705*

Antimony compounds

Enhanced Gate Swing in InP HEMTs With High Threshold Voltage by Means of InAlAsSb Barrier. *Suemitsu, T.*, +, *EDL Aug. 2007 669-671*

Antireflection coatings

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Ar Annealing for Suppression of Gate Oxide Thinning at Shallow Trench Isolation Edge. *Ohashi, T.*, +, *EDL July 2007 562-564*

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Arsenic Junction Thermal Stability and High-Dose Boron-Pocket Activation During SPER in nMOS Transistors. *Severi, S.*, +, *EDL March 2007 198-200*

Arsenic compounds

Enhanced Gate Swing in InP HEMTs With High Threshold Voltage by Means of InAlAsSb Barrier. *Suemitsu, T.*, +, *EDL Aug. 2007 669-671*
 Schottky-Barrier Height Tuning by Means of Ion Implantation Into Preformed Silicide Films Followed by Drive-In Anneal. *Zhang, Z.*, +, *EDL July 2007 565-568*

Atomic force microscopy

Performance Improvement of Organic Thin-Film Transistors by Electrode/Pentacene Interface Treatment Using a Hydrogen Plasma. *Lee, J.-W.*, +, *EDL May 2007 379-382*
 Effect of Gate Dopant Diffusion on Leakage Current in n⁺Poly-Si/HfO₂ and Examination of Leakage Paths by Conducting Atomic Force Microscopy. *Yu, X.*, +, *EDL May 2007 373-375*
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Achieving Conduction Band-Edge Effective Work Functions by La₂O₃ Capping of Hafnium Silicates. *Ragnarsson, L.-A.*, +, *EDL June 2007 486-488*
 Effect of a Two-Step Recess Process Using Atomic Layer Etching on the Performance of In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As p-HEMTs. *Kim, T.-W.*, +, *EDL Dec. 2007 1086-1088*
 Effective Work-Function Modulation by Aluminum-Ion Implantation for Metal-Gate Technology (Poly-Si/TiN/SiO₂). *Singanamalla, R.*, +, *EDL Dec. 2007 1089-1091*

Nitrogen Incorporation in HfSiO(N)/TaN Gate Stacks: Impact on Performances and NBTI. *Aoulaiche, M.*, +, *EDL July 2007 613-615*

The Application of an Ultrathin ALD HfSiON Cap Layer on SiON Dielectrics for Ni-FUSI CMOS Technology Targeting at Low-Power Applications. *Chang, S. Z.*, +, *EDL July 2007 634-636*

Avalanche breakdown

Experimental and TCAD Investigation of the Two Components of the Impact Ionization MOSFET (IMOS) Switching. *Mayer, F.*, +, *EDL July 2007 619-621*
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B

Ball grid arrays

Lifetime Extension of RF MEMS Direct Contact Switches in Hot Switching Operations by Ball Grid Array Dimple Design. *Chow, L. L. W.*, +, *EDL June 2007 479-481*

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Barium compounds

High-Performance Metal–Insulator–Metal Capacitors Using Amorphous BaSm₂Ti₄O₁₂ Thin Film. *Jeong, Y. H.*, +, *EDL Jan. 2007 17-20*

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High-Responsivity Photodetector in Standard SiGe BiCMOS Technology. *Lai, K.-S.*, +, *EDL Sept. 2007 800-802*

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Threshold Current for the Onset of Kirk Effect in Bipolar Transistors With a Fully Depleted Nonuniformly Doped Collector. *van der Toorn, R.*, *EDL Jan. 2007 54-57*

High-Gain Low Turn-On Voltage AlGaAs/GaAsNSb/GaAs Heterojunction Bipolar Transistors Grown by Molecular Beam Epitaxy. *Lew, K. L.*, +, *EDL Dec. 2007 1083-1085*

Parasitic Bipolar Junction Transistors in a Floating-Gate MOSFET for Fluorescence Detection. *Shin, K.-S.*, +, *EDL July 2007 581-583*

Bismuth compounds

Ferrite-Integrated On-Chip Inductors for RF ICs. *Yang, C.*, +, *EDL July 2007 652-655*

Boron

Arsenic Junction Thermal Stability and High-Dose Boron-Pocket Activation During SPER in nMOS Transistors. *Severi, S.*, +, *EDL March 2007 198-200*

Schottky-Barrier Height Tuning by Means of Ion Implantation Into Preformed Silicide Films Followed by Drive-In Anneal. *Zhang, Z.*, +, *EDL July 2007 565-568*

The Effect of Trapped Charge Distributions on Data Retention Characteristics of NAND Flash Memory Cells. *Park, M.*, +, *EDL Aug. 2007 750-752*

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1200-V 5.2-mΩ · cm² 4H-SiC BJTs With a High Common-Emitter Current Gain. *Lee, H.-S.*, +, *EDL Nov. 2007 1007-1009*

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Metamorphic Heterostructure InP/GaAsSb/InP HBTs on GaAs Substrates by MOCVD. *Zhou, W.*, +, *EDL July 2007 539-542*

Impact of Local Strain From Selective Epitaxial Germanium With Thin Si/SiGe Buffer on High-Performance p-i-n Photodetectors With a Low Thermal Budget. *Loh, W. Y.*, +, *EDL Nov. 2007 984-986*

Ultrahigh-Speed 0.5 V Supply Voltage In_{0.7}Ga_{0.3}As Quantum-Well Transistors on Silicon Substrate. *Datta, S.*, +, *EDL Aug. 2007 685-687*

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Effect of Gate Sinking on the Device Performance of the InGaP/AlGaAs/InGaAs Enhancement-Mode PHEMT. *Chu, L. H.*, +, *EDL Feb. 2007 82-85*

A Novel 700-V SOI LDMOS With Double-Sided Trench. *Luo, X.*, +, *EDL May 2007 422-424*

Observation of Threshold-Voltage Instability in Single-Crystal Silicon TFTs on Flexible Plastic Substrate. *Yuan, H.-C.*, +, *EDL July 2007 590-592*

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Sub-1-V Supply Self-Adaptive CMOS Image Sensor Cell With 86-dB Dynamic Range. *Lee, S.*, +, *EDL June 2007 492-494*

CMOS integrated circuits

Bond Pad Design With Low Capacitance in CMOS Technology for RF Applications. *Hsiao, Y.-W.*, +, *EDL Jan. 2007 68-70*

100-GHz Quasi-Yagi Antenna in Silicon Technology. *Sun, M.*, +, *EDL May 2007 455-457*

A 20-V CMOS-Based Monolithic Bidirectional Power Switch. *Fu, Y.*, +, *EDL Feb. 2007 174-176*

A Dynamical Power-Management Demonstration Using Four-Terminal Separated-Gate FinFETs. *Endo, K.*, +, *EDL May 2007 452-454*

A New Lateral-IGBT Structure With a Wider Safe Operating Area. *Bake-root, B.*, +, *EDL May 2007 416-418*

A Novel Strain Method for Enhancement of 90-nm Node and Beyond FUSI-Gated CMOS Performance. *Lin, C.-T.*, +, *EDL Feb. 2007 111-113*

A Wide Dynamic-Range CMOS Image Sensor Using Self-Reset Technique. *Park, D.*, +, *EDL Oct. 2007 890-892*

Achieving Low- V_T Ni-FUSI CMOS by Ultra-Thin Dy₂O₃ Capping of Hafnium Silicate Dielectrics. *Veloso, A.*, +, *EDL Nov. 2007 980-983*

CMOS Dual-Work-Function Engineering by Using Implanted Ni-FUSI. *Lin, C.-T.*, +, *EDL Sept. 2007 831-833*

CMOS Inverter Based on Gate-All-Around Silicon-Nanowire MOSFETs Fabricated Using Top-Down Approach. *Rustagi, S. C.*, +, *EDL Nov. 2007 1021-1024*

CMOS-Compatible Micromachined Toroid and Solenoid Inductors With High Q -Factors. *Zine-El-Abidine, I.*, +, *EDL March 2007 226-228*

Correction to "Revision of Tunneling Field-Effect Transistor in Standard CMOS Technologies". *Nirschl, Th.*, +, *EDL April 2007 315-315*

Frequency Variation of the Small-Signal Output Conductance of Decanometer MOSFETs Due to Substrate Crosstalk. *Kilchytka, V.*, +, *EDL May 2007 419-421*

High- Q Integrated Inductor Using Post-CMOS Selectively Grown Porous Silicon (SGPS) Technique for RFIC Applications. *Li, C.*, +, *EDL Aug. 2007 763-766*

Investigation and Localization of the SiGe Source/Drain (S/D) Strain-Induced Defects in PMOSFET With 45-nm CMOS Technology. *Cheng, C. Y.*, +, *EDL May 2007 408-411*

Millimeter-Wave Bandpass Filters by Standard 0.18- μ m CMOS Technology. *Sun, S.*, +, *EDL March 2007 220-222*

Parasitic Bipolar Junction Transistors in a Floating-Gate MOSFET for Fluorescence Detection. *Shin, K.-S.*, +, *EDL July 2007 581-583*

Predicting Thermal Neutron-Induced Soft Errors in Static Memories Using TCAD and Physics-Based Monte Carlo Simulation Tools. *Warren, K. M.*, +, *EDL Feb. 2007 180-182*

SiGe-Channel Confinement Effects for Short-Channel PFETs With Non-bandedge Gate Workfunctions. *Winstead, B.*, +, *EDL Aug. 2007 719-721*

Sub-0.1-eV Effective Schottky-Barrier Height for NiSi on n-Type Si (100) Using Antimony Segregation. *Wong, H.-S.*, +, *EDL Aug. 2007 703-705*

Symmetric Vertical Parallel Plate Capacitors for On-Chip RF Circuits in 65-nm SOI Technology. *Kim, D.*, +, *EDL July 2007 616-618*

Tensile-Strained Germanium CMOS Integration on Silicon. *Zang, H.*, +, *EDL Dec. 2007 1117-1119*

The Application of an Ultrathin ALD HfSiON Cap Layer on SiON Dielectrics for Ni-FUSI CMOS Technology Targeting at Low-Power Applications. *Chang, S. Z.*, +, *EDL July 2007 634-636*

Three-Dimensional Photodetectors in 3-D Silicon-On-Insulator Technology. *Curciello, E.*, +, *EDL Feb. 2007 117-119*

Vertically Stacked SiGe Nanowire Array Channel CMOS Transistors. *Fang, W. W.*, +, *EDL March 2007 211-213*

Young's Modulus Measurements in Standard IC CMOS Processes Using MEMS Test Structures. *Marshall, J. C.*, +, *EDL Nov. 2007 960-963*

CMOS logic circuits

A 0.26- μ m² U-Shaped Nitride-Based Programming Cell on Pure 90-nm CMOS Technology. *Lai, H.-C.*, +, *EDL Sept. 2007 837-839*

CMOS memory circuits

A Novel Dual-Polarity Nonvolatile Memory. *Lin, H.*, +, *EDL May 2007 412-415*

A Novel Dual-Doping Floating-Gate (DDFG) Flash Memory Featuring Low Power and High Reliability Application. *Li, Y.*, +, *EDL July 2007 622-624*

CVD coatings

Vertical Flash Memory Cell With Nanocrystal Floating Gate for Ultradense Integration and Good Retention. *Sarkar, J.*, +, *EDL May 2007 449-451*

Cadmium alloys

Resistive Switching Mechanism in Zn_xCd_{1-x}S Nonvolatile Memory Devices. *Wang, Z.*, +, *EDL Jan. 2007 14-16*

Cameras

Direct Monitoring of RF Overstress in High-Power Transistors and Amplifiers. *Stoppel, A.*, +, *EDL May 2007 357-359*

Capacitance

A Quantum-Mechanical View on the Capacitance of a Silicon p-n Junction. *Hurkx, G. A. M.*, +, *EDL April 2007 312-314*

Capacitance measurement

A High Schottky-Barrier of 1.1 eV Between Al and S-Passivated p-Type Si(100) Surface. *Song, G.*, +, *EDL Jan. 2007 71-73*

Accurate Series-Resistance Extraction From Capacitor Using Time Domain Reflectometry. *Wang, Y.*, +, *EDL April 2007 279-281*

- Electrical Characterization of Leaky Charge-Trapping High- κ MOS Devices Using Pulsed $Q-V$. *Martens, K.*, +, *EDL May 2007 436-439*
- Evaluation of RF Capacitance Extraction for Ultrathin Ultraleaky SOI MOS Devices. *Yu, C.*, +, *EDL Jan. 2007 45-47*
- Time-Domain-Reflectometry for Capacitance-Voltage Measurement With Very High Leakage Current. *Wang, Y.*, +, *EDL Jan. 2007 51-53*
- A Simple and Effective Approach to Improve the Output Linearity of Switched-Current AMOEDL Pixel Circuitry. *Guo, X.*, +, *EDL Oct. 2007 887-889*
- Active Pixel Concept Combined With Organic Photodiode for Imaging Devices. *Tedde, S.*, +, *EDL Oct. 2007 893-895*
- Improved Electrical Characteristics of Ge-on-Si Field-Effect Transistors With ControlEDL Ge Epitaxial Layer Thickness on Si Substrates. *Oh, J.*, +, *EDL Nov. 2007 1044-1046*
- Mobility Modeling and Its Extraction Technique for Manufacturing Strained-Si MOSFETs. *Wang, J.-S.*, +, *EDL Nov. 2007 1040-1043*
- Nonvolatile Multilevel Conductance and Memory Effect in Molecule-Based Devices. *Guo, P.*, +, *EDL July 2007 572-574*
- Capacitors**
- High-Temperature Leakage Improvement in Metal-Insulator-Metal Capacitors by Work-Function Tuning. *Chiang, K. C.*, +, *EDL March 2007 235-237*
- A Novel Single Polysilicon EEPROM Cell With a Polyfinger Capacitor. *Na, K.-Y.*, +, *EDL Nov. 2007 1047-1049*
- A Program-Erasable High- κ $\text{Hf}_{0.3}\text{N}_{0.2}\text{O}_{0.5}$ MIS Capacitor With Good Retention. *Yang, H. J.*, +, *EDL Oct. 2007 913-915*
- Accurate Series-Resistance Extraction From Capacitor Using Time Domain Reflectometry. *Wang, Y.*, +, *EDL April 2007 279-281*
- Good High-Temperature Stability of TiN/ Al_2O_3 /WN/TiN Capacitors. *Pan, T.-M.*, +, *EDL Nov. 2007 954-956*
- Metal-Oxide-High- κ Dielectric-Oxide-Semiconductor (MOHOS) Capacitors and Field-Effect Transistors for Memory Applications. *Hsu, H.*, +, *EDL Nov. 2007 964-966*
- Room-Temperature Deposited Titanium Silicate Thin Films for MIM Capacitor Applications. *Brassard, D.*, +, *EDL April 2007 261-263*
- Symmetric Vertical Parallel Plate Capacitors for On-Chip RF Circuits in 65-nm SOI Technology. *Kim, D.*, +, *EDL July 2007 616-618*
- Use of a High-Work-Function Ni Electrode to Improve the Stress Reliability of Analog SrTiO₃ Metal-Insulator-Metal Capacitors. *Chiang, K. C.*, +, *EDL Aug. 2007 694-696*
- Carbon**
- Fermi-Level Pinning in Nanocrystal Memories. *Hou, T.-H.*, +, *EDL Feb. 2007 103-106*
- Carbon nanotubes**
- Physical Modeling of Temperature Coefficient of Resistance for Single- and Multi-Wall Carbon Nanotube Interconnects. *Naeemi, A.*, +, *EDL Feb. 2007 135-138*
- An Efficient Macromodeling Approach for Simulating Carbon-Nanotube Field-Emission Triode Devices in Display Applications. *Guo, X.*, +, *EDL Aug. 2007 710-712*
- Analyzing Conductance of Mixed Carbon-Nanotube Bundles for Interconnect Applications. *Haruehanroengra, S.*, +, *EDL Aug. 2007 756-759*
- Carbon Nanotube-Based Triode Field Emission Lamps Using Metal Meshes With Spacers. *Cho, W.-S.*, +, *EDL May 2007 386-388*
- Conductance Modeling for Graphene Nanoribbon (GNR) Interconnects. *Naeemi, A.*, +, *EDL May 2007 428-431*
- Limits of Performance Gain of Aligned CNT Over Randomized Network: Theoretical Predictions and Experimental Validation. *Pimparkar, N.*, +, *EDL July 2007 593-595*
- Performance Implications of Inductive Effects for Carbon-Nanotube Bundle Interconnect. *Nieuwoudt, A.*, +, *EDL April 2007 305-307*
- Simulation of Graphene Nanoribbon Field-Effect Transistors. *Fiori, G.*, +, *EDL Aug. 2007 760-762*
- A Graphene Field-Effect Device. *Lemme, M. C.*, +, *EDL April 2007 282-284*
- Carrier density**
- Detection of Border Trap Density and Energy Distribution Along the Gate Dielectric Bulk of High- κ Gated MOS Devices. *Lu, C.-Y.*, +, *EDL May 2007 432-435*
- Carrier mobility**
- A Graphene Field-Effect Device. *Lemme, M. C.*, +, *EDL April 2007 282-284*
- Impacts of Notched-Gate Structure on Contact Etch Stop Layer (CESL) Stressed 90-nm nMOSFET. *Lin, C.-T.*, +, *EDL May 2007 376-378*
- Nitrogen Incorporation in HfSiO(N)/TaN Gate Stacks: Impact on Performances and NBTI. *Aoulaiche, M.*, +, *EDL July 2007 613-615*
- Stress Hybridization for Multigate Devices Fabricated on Supercritical Strained-SOI (SC-SSOI). *Collaert, N.*, +, *EDL July 2007 646-648*
- Cathodes**
- Carbon Nanotube-Based Triode Field Emission Lamps Using Metal Meshes With Spacers. *Cho, W.-S.*, +, *EDL May 2007 386-388*
- An Improved Planar Triode With ZnO Nanopin Field Emitters. *Wei, L.*, +, *EDL Aug. 2007 688-690*
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- Cavity resonators**
- GaN-Based High- Q Vertical-Cavity Light-Emitting Diodes. *Lu, T.-C.*, +, *EDL Oct. 2007 884-886*
- Channel separation**
- n^+ / p^+ Gate Bulk FinFETs With Locally Separated Channel Structure for Sub-50-nm DRAM Cell Transistors. *Jung, H.-A.-R.*, +, *EDL Dec. 2007 1126-1128*
- Charge carrier processes**
- A Program-Erasable High- κ $\text{Hf}_{0.3}\text{N}_{0.2}\text{O}_{0.5}$ MIS Capacitor With Good Retention. *Yang, H. J.*, +, *EDL Oct. 2007 913-915*
- Current-Dependent Switching Characteristics of PI-Diphenyl Carbamyl Films. *Kim, M.*, +, *EDL Nov. 2007 967-969*
- Charge injection**
- New Operating Mode Based on Electron/Hole Profile Matching in Nitride-Based Nonvolatile Memories. *Furnemont, A.*, +, *EDL April 2007 276-278*
- Charge pumps**
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- Chemical sensors**
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- Circuit bistability**
- Electrically Bistable Thin-Film Device Based on PVK and GNPs Polymer Material. *Song, Y.*, +, *EDL Feb. 2007 107-110*
- Circuit feedback**
- A Novel LTPS-TFT Pixel Circuit Compensating for TFT Threshold-Voltage Shift and OEDL Degradation for AMOEDL. *Lin, C.-L.*, +, *EDL Feb. 2007 129-131*
- Cobalt compounds**
- Ferrite-Integrated On-Chip Inductors for RF ICs. *Yang, C.*, +, *EDL July 2007 652-655*
- Coils**
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- Vertically Stacked SiGe Nanowire Array Channel CMOS Transistors. *Fang, W. W.*, +, *EDL March 2007 211-213*
- Conduction bands**
- Achieving Conduction Band-Edge Effective Work Functions by La_2O_3 Capping of Hafnium Silicates. *Ragnarsson, L.-A.*, +, *EDL June 2007 486-488*
- Enhanced Gate Swing in InP HEMTs With High Threshold Voltage by Means of InAlAsSb Barrier. *Suemitsu, T.*, +, *EDL Aug. 2007 669-671*
- Contact resistance**
- Novel Approach to Reduce Source/Drain Series and Contact Resistance in High-Performance UTSSOI CMOS Devices Using Selective Electrodeless CoWP or CoB Process. *Pan, J.*, +, *EDL Aug. 2007 691-693*
- Effective Schottky Barrier Height Reduction Using Sulfur or Selenium at the NiSi/n-Si (100) Interface for Low Resistance Contacts. *Wong, H.-S.*, +, *EDL Dec. 2007 1102-1104*
- Sub-0.1-eV Effective Schottky-Barrier Height for NiSi on n-Type Si (100) Using Antimony Segregation. *Wong, H.-S.*, +, *EDL Aug. 2007 703-705*

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Crosstalk

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Crystallisation

Degradation of Laser-Crystallized Laterally Grown Poly-Si TFT under Dynamic Stress. *Liu, P.-T.*, +, *EDL May 2007 401-403*

Crystallization of Double-Layered Silicon Thin Films by Solid Green Laser Annealing for High-Performance Thin-Film Transistors. *Sugawara, Y.*, +, *EDL May 2007 395-397*

Crystallization

High-Performance Short-Channel Double-Gate Low-Temperature Polysilicon Thin-Film Transistors Using Excimer Laser Crystallization. *Tsai, C.-C.*, +, *EDL Nov. 2007 1010-1013*

A Phase Change Memory Compact Model for Multilevel Applications. *Ventrice, D.*, +, *EDL Nov. 2007 973-975*

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A Planar Gunn Diode Operating Above 100 GHz. *Khalid, A.*, +, *EDL Oct. 2007 849-851*

Submicrometer Inversion-Type Enhancement-Mode InGaAs MOSFET With Atomic-Layer-Deposited Al₂O₃ as Gate Dielectric. *Xuan, Y.*, +, *EDL Nov. 2007 935-938*

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Long Retention of Gain-Cell Dynamic Random Access Memory With Undoped Memory Node. *Nishiguchi, K.*, +, *EDL Jan. 2007 48-50*

Gate Workfunction Engineering in Bulk FinFETs for Sub-50-nm DRAM Cell Transistors. *Park, K.-H.*, +, *EDL Feb. 2007 148-150*

New Insights on "Capacitorless" Floating-Body DRAM Cells. *Fossum, J. G.*, +, *EDL June 2007 513-516*

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OFF-State Avalanche-Breakdown-Induced ON-Resistance Degradation in Lateral DMOS Transistors. *Chen, J. F.*, +, *EDL Nov. 2007 1033-1035*

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Performance Implications of Inductive Effects for Carbon-Nanotube Bundle Interconnect. *Nieuwoudt, A.*, +, *EDL April 2007 305-307*

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Border-Trap Characterization in High- κ Strained-Si MOSFETs. *Maji, D.*, +, *EDL Aug. 2007 731-733*

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Electrical Characterization of ZrO₂/Si Interface Properties in MOSFETs With ZrO₂ Gate Dielectrics. *Liu, C.-H.*, +, *EDL Jan. 2007 62-64*

Charge Trapping and TDDB Characteristics of Ultrathin MOCVD HfO₂ Gate Dielectric on Nitrided Germanium. *Bai, W.*, +, *EDL May 2007 369-372*

Fermi-Level Pinning in Nanocrystal Memories. *Hou, T.-H.*, +, *EDL Feb. 2007 103-106*

High Transconductance MISFET With a Single InAs Nanowire Channel. *Do, Q.-T.*, +, *EDL Aug. 2007 682-684*

Low-Frequency Noise Assessment of Silicon Passivated Ge pMOSFETs With TiN/TaN/HfO₂ Gate Stack. *Guo, W.*, +, *EDL April 2007 288-291*

Observation of Metal-Layer Stress on Si Nanowires in Gate-All-Around High- κ /Metal-Gate Device Structures. *Singh, N.*, +, *EDL July 2007 558-561*

Observation of Threshold-Voltage Instability in Single-Crystal Silicon TFTs on Flexible Plastic Substrate. *Yuan, H.-C.*, +, *EDL July 2007 590-592*

Role of Nitrogen Atoms in Reduction of Electron Charge Traps in Hf-Based High- κ Dielectrics. *Umezawa, N.*, +, *EDL May 2007 363-365*

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Demonstration of Metal-Gated Low V_t n-MOSFETs Using a Poly-Si/TaN/Dy₂O₃/SiON Gate Stack With a ScaEDL EOT Value. *Yu, H. Y.*, +, *EDL July 2007 656-658*

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High-Performance Metal-Insulator-Metal Capacitors Using Amorphous BaSm₂Ti₄O₁₂ Thin Film. *Jeong, Y. H.*, +, *EDL Jan. 2007 17-20*

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High- κ Al₂O₃-HfTiO Nanolaminates With Less Than 0.8-nm Equivalent Oxide Thickness. *Mikheleshvili, V.*, +, *EDL Jan. 2007 24-26*

Yttrium- and Terbium-Based Interlayer on SiO₂ and HfO₂ Gate Dielectrics for Work Function Modulation of Nickel Fully Silicided Gate in nMOSFET. *Lim, A. E.-J.*, +, *EDL June 2007 482-485*

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Effect of SiN_x Gate Dielectric Deposition Power and Temperature on a-Si:H TFT Stability. *Kattamis, A. Z.*, +, *EDL July 2007 606-608*

A Novel Single Polysilicon EEPROM Cell With a Polyfinger Capacitor. *Na, K.-Y.*, +, *EDL Nov. 2007 1047-1049*

A Program-Erasable High- κ Hf_{0.3}N_{0.2}O_{0.5} MIS Capacitor With Good Retention. *Yang, H. J.*, +, *EDL Oct. 2007 913-915*

Achieving Low- V_T Ni-FUSI CMOS by Ultra-Thin Dy₂O₃ Capping of Hafnium Silicate Dielectrics. *Veloso, A.*, +, *EDL Nov. 2007 980-983*

Constant Bias Stress Effects on Threshold Voltage of Pentacene Thin-Film Transistors Employing Polyvinylphenol Gate Dielectric. *Kim, T. H.*, +, *EDL Oct. 2007 874-876*

Demonstration of Low V_t Ni-FUSI N-MOSFETs With SiON Dielectrics by Using a Dy₂O₃ Cap Layer. *Yu, H. Y.*, +, *EDL Nov. 2007 957-959*

Demonstration of Metal-Gated Low V_t n-MOSFETs Using a Poly-Si/TaN/Dy₂O₃/SiON Gate Stack With a ScaEDL EOT Value. *Yu, H. Y.*, +, *EDL July 2007 656-658*

Effects of Sulfur Passivation on Germanium MOS Capacitors With HfON Gate Dielectric. *Xie, R.*, +, *EDL Nov. 2007 976-979*

Good High-Temperature Stability of TiN/Al₂O₃/WN/TiN Capacitors. *Pan, T.-M.*, +, *EDL Nov. 2007 954-956*

High-Performance and Low-Temperature-Compatible p-Channel Polycrystalline-Silicon TFTs Using Hafnium-Silicate Gate Dielectric. *Yang, M.-J.*, +, *EDL Oct. 2007 902-904*

Improved Stability of High-Performance ZnO/ZnMgO Hetero-MISFETs. *Sasa, S.*, +, *EDL July 2007 543-545*

Investigation of Carrier Transport in Germanium MOSFETs With WN/Al₂O₃/AlN Gate Stacks. *Ritenour, A.*, +, *EDL Aug. 2007 746-749*

NMOS Compatible Work Function of TaN Metal Gate With Erbium-Oxide-Doped Hafnium Oxide Gate Dielectric. *Chen, J.*, +, *EDL Oct. 2007 862-864*

Submicrometer Inversion-Type Enhancement-Mode InGaAs MOSFET With Atomic-Layer-Deposited Al₂O₃ as Gate Dielectric. *Xuan, Y.*, +, *EDL Nov. 2007 935-938*

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GaN-Based High- Q Vertical-Cavity Light-Emitting Diodes. *Lu, T.-C., +, EDL Oct. 2007 884-886*

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Experimental Evaluation of Effects of Channel Doping on Characteristics of FinFETs. *Endo, K., +, EDL Dec. 2007 1123-1125*

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Impacts of Dopant Segregation on the Performance and Interface-State Density of the MOSFET With FUSI NiSi Gate. *Liu, J., +, EDL Jan. 2007 11-13*

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High-Current-Gain InP/GaInP/GaAsSb/InP DHBTs With $f_T = 436$ GHz. *Liu, H. G., +, EDL Oct. 2007 852-855*

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Flexible Full-Color AMOEDL on Ultrathin Metal Foil. *Jeong, J. K., +, EDL May 2007 389-391*

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A Quantum-Mechanical View on the Capacitance of a Silicon p-n Junction. *Hurkx, G. A. M., +, EDL April 2007 312-314*

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Conductance Modeling for Graphene Nanoribbon (GNR) Interconnects. *Naeemi, A., +, EDL May 2007 428-431*

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Analyzing Conductance of Mixed Carbon-Nanotube Bundles for Interconnect Applications. *Haruehanroengra, S., +, EDL Aug. 2007 756-759*

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A Novel Approach in Separating the Roles of Electrons and Holes in Causing Degradation in Hf-Based MOSFET Devices by Using Stress-Anneal Technique. *Akbar, M. S., +, EDL Feb. 2007 132-134*

A Novel 700-V SOI LDMOS With Double-Sided Trench. *Luo, X., +, EDL May 2007 422-424*

Duration of the High Breakdown Voltage Phase in Deep Depletion SOI LDMOS. *Napoli, E., EDL Aug. 2007 753-755*

High Transconductance MISFET With a Single InAs Nanowire Channel. *Do, Q.-T., +, EDL Aug. 2007 682-684*

Thickness Scaling and Reliability Comparison for the Inter-Poly High- κ Dielectrics. *Chen, Y.-Y., +, EDL Aug. 2007 700-702*

Electric current

Valence Band Offset Measurements on Thin Silicon-on-Insulator MOSFETs. *van der Steen, J.-L. P. J., +, EDL Sept. 2007 821-824*

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Measurement of Channel Stress Using Gate Direct Tunneling Current in Uniaxially Stressed nMOSFETs. *Hsieh, C.-Y., +, EDL Sept. 2007 818-820*

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Impact of High- κ Offset Spacer in 65-nm Node SOI Devices. *Ma, M.-W., +, EDL March 2007 238-241*

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Body Thickness Dependence of Impact Ionization in a Multiple-Gate FinFET. *Han, J.-W., +, EDL July 2007 625-627*

OFF-State Avalanche-Breakdown-Induced ON-Resistance Degradation in Lateral DMOS Transistors. *Chen, J. F., +, EDL Nov. 2007 1033-1035*

Current-Dependent Switching Characteristics of PI-Diphenyl Carbamyl Films. *Kim, M., +, EDL Nov. 2007 967-969*

The Leakage Current of the Schottky Contact on the Mesa Edge of AlGaIn/GaN Heterostructure. *Xu, C., +, EDL Nov. 2007 942-944*

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Physical Modeling of Temperature Coefficient of Resistance for Single- and Multi-Wall Carbon Nanotube Interconnects. *Naeemi, A., +, EDL Feb. 2007 135-138*

Electric resistance measurement

Accurate Series-Resistance Extraction From Capacitor Using Time Domain Reflectometry. *Wang, Y., +, EDL April 2007 279-281*

Extraction of π -Type Substrate Resistance Based on Three-Port Measurement and the Model Verification up to 110 GHz. *Kang, I. M., +, EDL May 2007 425-427*

On-Resistance Degradations for Different Stress Conditions in High-Voltage pEDLMOS Transistor With Thick Gate Oxide. *Sun, W., +, EDL July 2007 631-633*

Electrical conductivity

Physical Modeling of Temperature Coefficient of Resistance for Single- and Multi-Wall Carbon Nanotube Interconnects. *Naeemi, A., +, EDL Feb. 2007 135-138*

Analyzing Conductance of Mixed Carbon-Nanotube Bundles for Interconnect Applications. *Haruehanroengra, S., +, EDL Aug. 2007 756-759*

Electrical resistance measurement

Body Thickness Dependence of Impact Ionization in a Multiple-Gate FinFET. *Han, J.-W., +, EDL July 2007 625-627*

Anomalous Cells With Low Reset Resistance in Phase-Change-Memory Arrays. *Mantegazza, D., +, EDL Oct. 2007 865-867*

Design of On-Chip Transformer With Various Coil Widths to Achieve Minimal Metal Resistance. *Hsu, H.-M., +, EDL Nov. 2007 1029-1032*

Electrical resistivity

Resistive Switching Mechanism in $Zn_xCd_{1-x}S$ Nonvolatile Memory Devices. *Wang, Z., +, EDL Jan. 2007 14-16*

Electrodes

Electrical Properties of nMOSFETs Using the NiSi:Yb FUSI Electrode. *Yu, H. Y., +, EDL Feb. 2007 154-156*

Current-Dependent Switching Characteristics of PI-Diphenyl Carbamyl Films. *Kim, M., +, EDL Nov. 2007 967-969*

Demonstration of Low V_t Ni-FUSI N-MOSFETs With SiON Dielectrics by Using a Dy_2O_3 Cap Layer. *Yu, H. Y., +, EDL Nov. 2007 957-959*

Effect of Load Distribution on the Voltage Drop and the Luminance Variation in an AC-PDP. *Kim, J.-S., +, EDL Oct. 2007 896-898*

Effect of Top Electrode Material on Resistive Switching Properties of ZrO_2 Film Memory Devices. *Lin, C.-Y., +, EDL May 2007 366-368*

Good High-Temperature Stability of $TiN/Al_2O_3/WN/TiN$ Capacitors. *Pan, T.-M., +, EDL Nov. 2007 954-956*

Improvement of the Conversion Performance of a Resonating Multimode Microelectromechanical Mixer-Filter Through Parametric Amplification. *Koskenvuori, M., +, EDL Nov. 2007 970-972*

Nonvolatile Multilevel Conductance and Memory Effect in Molecule-Based Devices. *Guo, P., +, EDL July 2007 572-574*

SiGe-Channel Confinement Effects for Short-Channel PFETs With Non-bandedge Gate Workfunctions. *Winstead, B., +, EDL Aug. 2007 719-721*

Solution-Processed n-Type Organic Field-Effect Transistors With High ON/OFF Current Ratios Based on Fullerene Derivatives. *Tiwari, S. P., +, EDL Oct. 2007 880-883*

Use of a High-Work-Function Ni Electrode to Improve the Stress Reliability of Analog SrTiO₃ Metal-Insulator-Metal Capacitors. *Chiang, K. C., +, EDL Aug. 2007 694-696*

Electrolytic capacitors

High-Quality Factor Electrolyte Insulator Silicon Capacitor for Wireless Chemical Sensing. *Garcia-Canton, J., +, EDL Jan. 2007 27-29*

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Robust Coupled-Quantum-Well Structure for Use in Electrorefraction Modulators. *Ristic, S., +, EDL Jan. 2007 30-32*

Electromigration

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Temperature-Oriented Experiment and Simulation as Corroborating Evidence of MOSFET Backscattering Theory. *Chen, M.-J., +, EDL Feb. 2007 177-179*

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High- κ Al_2O_3 -HfTiO Nanolaminates With Less Than 0.8-nm Equivalent Oxide Thickness. *Mikhelashvili, V., +, EDL Jan. 2007 24-26*

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Conductance Modeling for Graphene Nanoribbon (GNR) Interconnects. *Naeemi, A., +, EDL May 2007 428-431*

Electron devices

Improved Electrical Characteristics and Reliability of MILC Poly-Si TFTs Using Fluorine-Ion Implantation. *Chang, C.-P., +, EDL Nov. 2007 990-992*

Electron impact ionisation

Improved Reliability by Reduction of Hot-Electron Damage in the Vertical Impact-Ionization MOSFET (I-MOS). *Abelein, U.*, +, *EDL Jan. 2007 65-67*

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Achieving Conduction Band-Edge Effective Work Functions by La_2O_3 Capping of Hafnium Silicates. *Ragnarsson, L.-A.*, +, *EDL June 2007 486-488*
Effect of a Two-Step Recess Process Using Atomic Layer Etching on the Performance of $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ p-HEMTs. *Kim, T.-W.*, +, *EDL Dec. 2007 1086-1088*

Electron Transport in Strained-Silicon Directly on Insulator Ultrathin-Body n-MOSFETs With Body Thickness Ranging From 2 to 25 nm. *Gomez, L.*, +, *EDL April 2007 285-287*

Enhanced Strain Effects in 25-nm Gate-Length Thin-Body nMOSFETs With Silicon-Carbon Source/Drain and Tensile-Stress Liner. *Ang, K.-W.*, +, *EDL April 2007 301-304*

HfLaON n-MOSFETs Using a Low Work Function HfSi_x Gate. *Cheng, C. F.*, +, *EDL Dec. 2007 1092-1094*

Investigation of Carrier Transport in Germanium MOSFETs With $\text{WN}/\text{Al}_2\text{O}_3/\text{AlN}$ Gate Stacks. *Ritenour, A.*, +, *EDL Aug. 2007 746-749*

Passivation Effects of Aluminum on Polycrystalline Silicon Thin-Film Transistor With Metal-Replaced Junctions. *Zhang, D.*, +, *EDL Feb. 2007 126-128*

Strained n-Channel Transistors With Silicon Source and Drain Regions and Embedded Silicon/Germanium as Strain-Transfer Structure. *Ang, K.-W.*, +, *EDL July 2007 609-612*

The Origin of Electron Mobility Enhancement in Strained MOSFETs. *Hadjisavvas, G.*, +, *EDL Nov. 2007 1018-1020*

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A Novel Dilute Antimony Channel $\text{In}_{0.2}\text{Ga}_{0.8}\text{AsSb}/\text{GaAs}$ HEMT. *Su, K.-H.*, +, *EDL Feb. 2007 96-99*

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Charge Trapping and TDDB Characteristics of Ultrathin MOCVD HfO_2 Gate Dielectric on Nitrided Germanium. *Bai, W.*, +, *EDL May 2007 369-372*

On-Resistance Degradations for Different Stress Conditions in High-Voltage pEDLMOS Transistor With Thick Gate Oxide. *Sun, W.*, +, *EDL July 2007 631-633*

Profiling of Nitride-Trap-Energy Distribution in SONOS Flash Memory by Using a Variable-Amplitude Low-Frequency Charge-Pumping Technique. *Liao, Y.-Y.*, +, *EDL Sept. 2007 828-830*

Role of Nitrogen Atoms in Reduction of Electron Charge Traps in Hf-Based High- κ Dielectrics. *Umezawa, N.*, +, *EDL May 2007 363-365*

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CMOS-Compatible Micromachined Toroid and Solenoid Inductors With High Q -Factors. *Zine-El-Abidine, I.*, +, *EDL March 2007 226-228*

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Improved Reliability and ESD Characteristics of Flip-Chip GaN-Based EDLs With Internal Inverse-Parallel Protection Diodes. *Shei, S.-C.*, +, *EDL May 2007 346-349*

An Unassisted, Low Trigger-, and High Holding-Voltage SCR (uSCR) for On-Chip ESD-Protection Applications. *Lou, L.*, +, *EDL Dec. 2007 1120-1122*

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Substrate Bias Effect Linked to Parasitic Series Resistance in Multiple-Gate SOI MOSFETs. *Rudenko, T.*, +, *EDL Sept. 2007 834-836*

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A High Schottky-Barrier of 1.1 eV Between Al and S-Passivated p-Type Si(100) Surface. *Song, G.*, +, *EDL Jan. 2007 71-73*

A Novel Nanowire Channel Poly-Si TFT Functioning as Transistor and Non-volatile SONOS Memory. *Chen, S.-C.*, +, *EDL Sept. 2007 809-811*

A Quantum-Mechanical View on the Capacitance of a Silicon p-n Junction. *Hurkx, G. A. M.*, +, *EDL April 2007 312-314*

Charge Trapping and TDDB Characteristics of Ultrathin MOCVD HfO_2 Gate Dielectric on Nitrided Germanium. *Bai, W.*, +, *EDL May 2007 369-372*

Defect Passivation by Selenium-Ion Implantation for Poly-Si Thin Film Transistors. *Lai, J.*, +, *EDL Aug. 2007 725-727*

High-Temperature Leakage Improvement in Metal-Insulator-Metal Capacitors by Work-Function Tuning. *Chiang, K. C.*, +, *EDL March 2007 235-237*

Low-Temperature Polymer-Based Three-Dimensional Silicon Integration. *Kim, S.*, +, *EDL Aug. 2007 706-709*

Negligible Effect of Process-Induced Strain on Intrinsic NBTI Behavior. *Shickova, A.*, +, *EDL March 2007 242-244*

Numerical Simulation of Low-Frequency Noise in Polysilicon Thin-Film Transistors. *Pichon, L.*, +, *EDL Aug. 2007 716-718*

Observation of Metal-Layer Stress on Si Nanowires in Gate-All-Around High- κ /Metal-Gate Device Structures. *Singh, N.*, +, *EDL July 2007 558-561*

Piezoresistance Coefficients of (100) Silicon nMOSFETs Measured at Low and High (~ 1.5 GPa) Channel Stress. *Suthram, S.*, +, *EDL Jan. 2007 58-61*

The Preparation of Nanocrystalline Silicon by Plasma-Enhanced Hydrogenation for the Fabrication of Light-Emitting Diodes. *Jamei, M.*, +, *EDL March 2007 207-210*

Transport Mechanism of SiGe Dot MOS Tunneling Diodes. *Kuo, P.-S.*, +, *EDL July 2007 596-598*

Ultrahigh-Speed 0.5 V Supply Voltage $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ Quantum-Well Transistors on Silicon Substrate. *Datta, S.*, +, *EDL Aug. 2007 685-687*

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Embedded TFT NAND-Type Nonvolatile Memory in Panel. *Chen, H.-T.*, +, *EDL June 2007 499-501*

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Silicon Dioxide-Encapsulated High-Voltage AlGaIn/GaN HFETs for Power-Switching Applications. *Tipirneni, N.*, +, *EDL Sept. 2007 784-786*

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Improved Electrical Characteristics of Ge-on-Si Field-Effect Transistors With Control EDL Ge Epitaxial Layer Thickness on Si Substrates. *Oh, J.*, +, *EDL Nov. 2007 1044-1046*

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Low-Temperature Transport Characteristics and Quantum-Confinement Effects in Gate-All-Around Si-Nanowire N-MOSFET. *Rustagi, S. C.*, +, *EDL Oct. 2007 909-912*

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AlGaIn/GaN HEMTs With Thin InGaIn Cap Layer for Normally Off Operation. *Mizutani, T.*, +, *EDL July 2007 549-551*

Demonstration of Asymmetric Gate-Oxide Thickness Four-Terminal Fin-FETs Having Flexible Threshold Voltage and Good Subthreshold Slope. *Masahara, M.*, +, *EDL March 2007 217-219*

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High-Performance Polycrystalline-Silicon TFT by Heat-Retaining Enhanced Lateral Crystallization. *Liu, P.-T.*, +, *EDL Aug. 2007 722-724*

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- Conductance Modeling for Graphene Nanoribbon (GNR) Interconnects. *Naeemi, A.*, +, *EDL May 2007 428-431*

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- Effective Work-Function Modulation by Aluminum-Ion Implantation for Metal-Gate Technology (Poly-Si/TiN/SiO₂). *Singanamalla, R.*, +, *EDL Dec. 2007 1089-1091*

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- High-Temperature Operation of AlGaIn/GaN HEMTs Direct-Coupled FET Logic (DCFL) Integrated Circuits. *Cai, Y.*, +, *EDL May 2007 328-331*
- Impact of CF₄ Plasma Treatment on GaN. *Chu, R.*, +, *EDL Sept. 2007 781-783*
- SiGe-Channel Confinement Effects for Short-Channel PFETs With Non-bandedge Gate Workfunctions. *Winstead, B.*, +, *EDL Aug. 2007 719-721*
- Simulation of Graphene Nanoribbon Field-Effect Transistors. *Fiori, G.*, +, *EDL Aug. 2007 760-762*
- Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec. *Choi, W. Y.*, +, *EDL Aug. 2007 743-745*

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- Carbon Nanotube-Based Triode Field Emission Lamps Using Metal Meshes With Spacers. *Cho, W.-S.*, +, *EDL May 2007 386-388*

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- An Efficient Macromodeling Approach for Simulating Carbon-Nanotube Field-Emission Triode Devices in Display Applications. *Guo, X.*, +, *EDL Aug. 2007 710-712*
- An Improved Planar Triode With ZnO Nanopin Field Emitters. *Wei, L.*, +, *EDL Aug. 2007 688-690*

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- Nonvolatile Multilevel Conductance and Memory Effect in Molecule-Based Devices. *Guo, P.*, +, *EDL July 2007 572-574*
- Current-Dependent Switching Characteristics of PI-Diphenyl Carbamyl Films. *Kim, M.*, +, *EDL Nov. 2007 967-969*
- Enhanced Thermal Efficiency in Phase-Change Memory Cell by Double GST Thermally Confined Structure. *Chao, D.-S.*, +, *EDL Oct. 2007 871-873*
- Good High-Temperature Stability of TiN/Al₂O₃/WN/TiN Capacitors. *Pan, T.-M.*, +, *EDL Nov. 2007 954-956*
- High-Performance and Low-Temperature-Compatible p-Channel Polycrystalline-Silicon TFTs Using Hafnium-Silicate Gate Dielectric. *Yang, M.-J.*, +, *EDL Oct. 2007 902-904*
- Impact of Local Strain From Selective Epitaxial Germanium With Thin Si/SiGe Buffer on High-Performance p-i-n Photodetectors With a Low Thermal Budget. *Loh, W. Y.*, +, *EDL Nov. 2007 984-986*
- Improved Electrical Characteristics and Reliability of MILC Poly-Si TFTs Using Fluorine-Ion Implantation. *Chang, C.-P.*, +, *EDL Nov. 2007 990-992*
- Improving the Electrical Properties of NILC Poly-Si Films Using a Gettering Substrate. *Hu, C.-M.*, +, *EDL Nov. 2007 1000-1003*
- Low-Temperature Passivation of Amorphous-Silicon Thin-Film Transistors With Supercritical Fluids. *Tsai, C.-T.*, +, *EDL July 2007 584-586*
- Reduction of Threshold Voltage by Diffusion Control Technique in p-MISFETs Using Poly-Si/TiN/HfSiON Gate Stacks. *Kawahara, T.*, +, *EDL Oct. 2007 868-870*

FinFETs

- Body Thickness Dependence of Impact Ionization in a Multiple-Gate FinFET. *Han, J.-W.*, +, *EDL July 2007 625-627*
- N-Channel (110)-Sidewall Strained FinFETs With Silicon-Carbon Source and Drain Stressors and Tensile Capping Layer. *Liow, T.-Y.*, +, *EDL Nov. 2007 1014-1017*
- Strained p-Channel FinFETs With Extended II-Shaped Silicon-Germanium Source and Drain Stressors. *Tan, K.-M.*, +, *EDL Oct. 2007 905-908*

Flash memories

- Electrically Bistable Thin-Film Device Based on PVK and GNPs Polymer Material. *Song, Y.*, +, *EDL Feb. 2007 107-110*
- A High-Performance Body-Tied FinFET Bandgap Engineered SONOS (BE-SONOS) for NAND-Type Flash Memory. *Hsu, T.-H.*, +, *EDL May 2007 443-445*
- A Novel Dual-Doping Floating-Gate (DDFG) Flash Memory Featuring Low Power and High Reliability Application. *Li, Y.*, +, *EDL July 2007 622-624*
- Dual-Bit/Cell SONOS Flash EEPROMs: Impact of Channel Engineering on Programming Speed and Bit Coupling Effect. *Datta, A.*, +, *EDL May 2007 446-448*
- Fabrication of Ni Nanocrystal Flash Memories Using a Polymeric Self-Assembly Approach. *Shahrjerdi, D.*, +, *EDL Sept. 2007 793-796*
- Impact of Channel Dangling Bonds on Reliability Characteristics of Flash Memory on Poly-Si Thin Films. *Lin, Y.-H.*, +, *EDL April 2007 267-269*
- Profiling of Nitride-Trap-Energy Distribution in SONOS Flash Memory by Using a Variable-Amplitude Low-Frequency Charge-Pumping Technique. *Liao, Y.-Y.*, +, *EDL Sept. 2007 828-830*
- The Effect of Trapped Charge Distributions on Data Retention Characteristics of NAND Flash Memory Cells. *Park, M.*, +, *EDL Aug. 2007 750-752*
- Thickness Scaling and Reliability Comparison for the Inter-Poly High- κ Dielectrics. *Chen, Y.-Y.*, +, *EDL Aug. 2007 700-702*
- Giant Random Telegraph Signals in Nanoscale Floating-Gate Devices. *Fantini, P.*, +, *EDL Dec. 2007 1114-1116*
- Vertical Flash Memory Cell With Nanocrystal Floating Gate for Ultradense Integration and Good Retention. *Sarkar, J.*, +, *EDL May 2007 449-451*

Flexible electronics

- Observation of Threshold-Voltage Instability in Single-Crystal Silicon TFTs on Flexible Plastic Substrate. *Yuan, H.-C.*, +, *EDL July 2007 590-592*

Flicker noise

- Flicker Noise and Its Degradation Characteristics Under Electrical Stress in MOSFETs With Thin Strained-Si/SiGe Dual-Quantum Well. *Jiang, Y.*, +, *EDL July 2007 603-605*

Flip-chip devices

- Improved Reliability and ESD Characteristics of Flip-Chip GaN-Based EDLs With Internal Inverse-Parallel Protection Diodes. *Shei, S.-C.*, +, *EDL May 2007 346-349*
- A 0.2-W Heterostructure Barrier Varactor Frequency Tripler at 113 GHz. *Vukusic, J.*, +, *EDL May 2007 340-342*
- Electromigration Resistant Power Delivery Systems. *Sekar, D. C.*, +, *EDL Aug. 2007 767-769*

Fluids

- Low-Temperature Passivation of Amorphous-Silicon Thin-Film Transistors With Supercritical Fluids. *Tsai, C.-T.*, +, *EDL July 2007 584-586*

Fluorescence

- Parasitic Bipolar Junction Transistors in a Floating-Gate MOSFET for Fluorescence Detection. *Shin, K.-S.*, +, *EDL July 2007 581-583*

Fluorine

- Effect of F₂ Postmetallization Annealing on the Electrical and Reliability Characteristics of HfSiO Gate Dielectric. *Chang, M.*, +, *EDL Jan. 2007 21-23*
- Fluorine Passivation in Gate Stacks of Poly-Si/TaN/HfO₂ (and HfSiON/HfO₂)/Si Through Gate Ion Implantation. *Zhang, M. H.*, +, *EDL March 2007 195-197*

Flux pinning

- Effective Work-Function Modulation by Aluminum-Ion Implantation for Metal-Gate Technology (Poly-Si/TiN/SiO₂). *Singanamalla, R.*, +, *EDL Dec. 2007 1089-1091*

Frequency measurement

- Young's Modulus Measurements in Standard IC CMOS Processes Using MEMS Test Structures. *Marshall, J. C.*, +, *EDL Nov. 2007 960-963*

Frequency multipliers

- A 0.2-W Heterostructure Barrier Varactor Frequency Tripler at 113 GHz. *Vukusic, J.*, +, *EDL May 2007 340-342*

G

Gadolinium

Characteristics of Ni/Gd FUSI for NMOS Gate Electrode Applications. *Lee, B.*, +, *EDL July 2007 555-557*

Gadolinium compounds

Improved Reliability and ESD Characteristics of Flip-Chip GaN-Based EDLs With Internal Inverse-Parallel Protection Diodes. *Shei, S.-C.*, +, *EDL May 2007 346-349*

A New Method for Identification and Minimization of Distortion Sources in GaN HEMT Devices Based on Volterra Series Analysis. *Srinidhi, E. R.*, +, *EDL May 2007 343-345*

Gain

50-nm T-Gate InAlAs/InGaAs Metamorphic HEMTs With Low Noise and High f_T Characteristics. *Lim, B. O.*, +, *EDL July 2007 546-548*

1200-V 5.2-mΩ · cm² 4H-SiC BJTs With a High Common-Emitter Current Gain. *Lee, H.-S.*, +, *EDL Nov. 2007 1007-1009*

35-nm Zigzag T-Gate In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As Metamorphic GaAs HEMTs With an Ultrahigh f_{max} of 520 GHz. *Lee, K.-S.*, +, *EDL Aug. 2007 672-675*

Active Pixel Concept Combined With Organic Photodiode for Imaging Devices. *Tedde, S.*, +, *EDL Oct. 2007 893-895*

CMOS Inverter Based on Gate-All-Around Silicon-Nanowire MOSFETs Fabricated Using Top-Down Approach. *Rustagi, S. C.*, +, *EDL Nov. 2007 1021-1024*

High-Current-Gain InP/GaInP/GaAsSb/InP DHBTs With $f_T = 436$ GHz. *Liu, H. G.*, +, *EDL Oct. 2007 852-855*

High-Gain Low Turn-On Voltage AlGaAs/GaAsNSb/GaAs Heterojunction Bipolar Transistors Grown by Molecular Beam Epitaxy. *Lew, K. L.*, +, *EDL Dec. 2007 1083-1085*

Improvement of the Conversion Performance of a Resonating Multimode Microelectromechanical Mixer-Filter Through Parametric Amplification. *Koskenvuori, M.*, +, *EDL Nov. 2007 970-972*

Monolithically Integrated Logic NOR Gate Based on GaAs/AlGaAs Three-Terminal Junctions. *Muller, C. R.*, +, *EDL Oct. 2007 859-861*

Gallium

CMOS Dual-Work-Function Engineering by Using Implanted Ni-FUSI. *Lin, C.-T.*, +, *EDL Sept. 2007 831-833*

Gallium arsenide

DC Characteristics of AlGaAs/GaAs/GaN HBTs Formed by Direct Wafer Fusion. *Lian, C.*, +, *EDL Jan. 2007 8-10*

35-nm Zigzag T-Gate In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As Metamorphic GaAs HEMTs With an Ultrahigh f_{max} of 520 GHz. *Lee, K.-S.*, +, *EDL Aug. 2007 672-675*

InGaAsSb/InP Double Heterojunction Bipolar Transistors Grown by Solid-Source Molecular Beam Epitaxy. *Chen, S.-H.*, +, *EDL Aug. 2007 679-681*

A 0.2-W Heterostructure Barrier Varactor Frequency Tripler at 113 GHz. *Vukusic, J.*, +, *EDL May 2007 340-342*

A Planar Gunn Diode Operating Above 100 GHz. *Khalid, A.*, +, *EDL Oct. 2007 849-851*

High-Current-Gain InP/GaInP/GaAsSb/InP DHBTs With $f_T = 436$ GHz. *Liu, H. G.*, +, *EDL Oct. 2007 852-855*

High-Speed InGaP/GaAs p-i-n Photodiodes With Wide Spectral Range. *Wu, M.-C.*, +, *EDL Sept. 2007 797-799*

Hot-Phonon Effect on the Electrothermal Behavior of Submicrometer III-V HEMTs. *Sadi, T.*, +, *EDL Sept. 2007 787-789*

Metamorphic Heterostructure InP/GaAsSb/InP HBTs on GaAs Substrates by MOCVD. *Zhou, W.*, +, *EDL July 2007 539-542*

Monolithically Integrated Logic NOR Gate Based on GaAs/AlGaAs Three-Terminal Junctions. *Muller, C. R.*, +, *EDL Oct. 2007 859-861*

Robust CoupEDL-Quantum-Well Structure for Use in Electrorefraction Modulators. *Ristic, S.*, +, *EDL Jan. 2007 30-32*

Ultrahigh-Speed 0.5 V Supply Voltage In_{0.7}Ga_{0.3}As Quantum-Well Transistors on Silicon Substrate. *Datta, S.*, +, *EDL Aug. 2007 685-687*

Gallium compounds

Power Stability of AlGaIn/GaN HFETs at 20 W/mm in the Pinched-Off Operation Mode. *Koudymov, A.*, +, *EDL Jan. 2007 5-7*

1- μ m Enhancement Mode GaAs N-Channel MOSFETs With Transconductance Exceeding 250 mS/mm. *Rajagopalan, K.*, +, *EDL Feb. 2007 100-102*

1.3- μ m GaInAsN Vertical-Cavity Surface-Emitting Lasers by Oxide-Planarized and Surface-Relief Processes for Single-Mode Operation. *Lee, F.-M.*, +, *EDL Feb. 2007 120-122*

A Novel Dilute Antimony Channel In_{0.2}Ga_{0.8}AsSb/GaAs HEMT. *Su, K.-H.*, +, *EDL Feb. 2007 96-99*

AlGaIn/GaN HEMTs With Thin InGaIn Cap Layer for Normally Off Operation. *Mizutani, T.*, +, *EDL July 2007 549-551*

Compact Model of Current Collapse in Heterostructure Field-Effect Transistors. *Koudymov, A.*, +, *EDL May 2007 332-335*

DC Characteristics of AlGaAs/GaAs/GaN HBTs Formed by Direct Wafer Fusion. *Lian, C.*, +, *EDL Jan. 2007 8-10*

Effect of Gate Sinking on the Device Performance of the InGaP/AlGaAs/InGaAs Enhancement-Mode PHEMT. *Chu, L. H.*, +, *EDL Feb. 2007 82-85*

Enhancement-Mode GaAs MOSFETs With an In_{0.3}Ga_{0.7}As Channel, a Mobility of Over 5000 cm²/V · s, and Transconductance of Over 475 μ S/ μ m. *Hill, R. J. W.*, +, *EDL Dec. 2007 1080-1082*

Fabrication of 0.15- μ m Γ -Shaped Gate In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As Metamorphic HEMTs Using DUV Lithography and Tilt Dry-Etching Technique. *Lien, Y.-C.*, +, *EDL Feb. 2007 93-95*

High-Gain Low Turn-On Voltage AlGaAs/GaAsNSb/GaAs Heterojunction Bipolar Transistors Grown by Molecular Beam Epitaxy. *Lew, K. L.*, +, *EDL Dec. 2007 1083-1085*

High-Speed InGaP/GaAs p-i-n Photodiodes With Wide Spectral Range. *Wu, M.-C.*, +, *EDL Sept. 2007 797-799*

High-Temperature Operation of AlGaIn/GaN HEMTs Direct-CoupEDL FET Logic (DCFL) Integrated Circuits. *Cai, Y.*, +, *EDL May 2007 328-331*

Impact of CF₄ Plasma Treatment on GaN. *Chu, R.*, +, *EDL Sept. 2007 781-783*

Normally Off AlGaIn/GaN Low-Density Drain HEMT (LDD-HEMT) With Enhanced Breakdown Voltage and Reduced Current Collapse. *Song, D.*, +, *EDL March 2007 189-191*

ON-Resistance Modulation of High Voltage GaN HEMT on Sapphire Substrate Under High Applied Voltage. *Saito, W.*, +, *EDL Aug. 2007 676-678*

RF Power Measurements of InAlN/GaN Unstrained HEMTs on SiC Substrates at 10 GHz. *Jessen, G. H.*, +, *EDL May 2007 354-356*

SAW Filters Composed of Interdigital Schottky and Ohmic Contacts on AlGaIn/GaN Heterostructures. *Shigekawa, N.*, +, *EDL Feb. 2007 90-92*

Selectively Doped High-Power AlGaIn/GaN MOS-DHFET. *Adivarahan, V.*, +, *EDL March 2007 192-194*

Silicon Dioxide-Encapsulated High-Voltage AlGaIn/GaN HFETs for Power-Switching Applications. *Tipirneni, N.*, +, *EDL Sept. 2007 784-786*

Submicrometer Copper T-Gate AlGaIn/GaN HFETs: The Gate Metal Stack Effect. *Sun, H. F.*, +, *EDL May 2007 350-353*

Time-Resolved Temperature Measurement of AlGaIn/GaN Electronic Devices Using Micro-Raman Spectroscopy. *Kuball, M.*, +, *EDL Feb. 2007 86-89*

Gallium nitride

GaN-Based High-Q Vertical-Cavity Light-Emitting Diodes. *Lu, T.-C.*, +, *EDL Oct. 2007 884-886*

Comparison of GaN HEMTs on Diamond and SiC Substrates. *Felbinger, J. G.*, +, *EDL Nov. 2007 948-950*

Normally Off n-Channel GaN MOSFETs on Si Substrates Using an SAG Technique and Ion Implantation. *Kambayashi, H.*, +, *EDL Dec. 2007 1077-1079*

Power Performance of AlGaIn/GaN HEMTs Grown on SiC by Ammonia-MBE at 4 and 10 GHz. *Poblentz, C.*, +, *EDL Nov. 2007 945-947*

Remarkable Reduction of On-Resistance by Ion Implantation in GaN/AlGaIn/GaN HEMTs With Low Gate Leakage Current. *Nomoto, K.*, +, *EDL Nov. 2007 939-941*

The Leakage Current of the Schottky Contact on the Mesa Edge of AlGaIn/GaN Heterostructure. *Xu, C.*, +, *EDL Nov. 2007 942-944*

Gate leakage

Demonstration of Metal-Gated Low V_t n-MOSFETs Using a Poly-Si/TaN/Dy₂O₃/SiON Gate Stack With a ScaEDL EOT Value. *Yu, H. Y.*, +, *EDL July 2007 656-658*

High-Performance and Low-Temperature-Compatible p-Channel Polycrystalline-Silicon TFTs Using Hafnium-Silicate Gate Dielectric. *Yang, M.-J.*, +, *EDL Oct. 2007 902-904*

Ge-Si alloys

Low-Frequency Noise Characteristics in Strained-Si nMOSFETs. *Wang, Y. P.*, +, *EDL Jan. 2007 36-38*

High Mobility Strained Ge pMOSFETs With High- κ /Metal Gate. *Nicholas, G.*, +, *EDL Sept. 2007 825-827*

High-Responsivity Photodetector in Standard SiGe BiCMOS Technology. *Lai, K.-S.*, +, *EDL Sept. 2007 800-802*

Investigation and Localization of the SiGe Source/Drain (S/D) Strain-Induced Defects in PMOSFET With 45-nm CMOS Technology. *Cheng, C. Y.*, +, *EDL May 2007 408-411*

Negligible Effect of Process-Induced Strain on Intrinsic NBTI Behavior. *Shickova, A.*, +, *EDL March 2007 242-244*

On the Use of a SiGe Spike in the Emitter to Improve the $f_T \times BV_{CEO}$ Product of High-Speed SiGe HBTs. *Choi, L. J.*, +, *EDL April 2007 270-272*

SiGe-Channel Confinement Effects for Short-Channel PFETs With Non-bandedge Gate Workfunctions. *Winstead, B.*, +, *EDL Aug. 2007 719-721*

Transport Mechanism of SiGe Dot MOS Tunneling Diodes. *Kuo, P.-S.*, +, *EDL July 2007 596-598*

Vertical Flash Memory Cell With Nanocrystal Floating Gate for Ultradense Integration and Good Retention. *Sarkar, J.*, +, *EDL May 2007 449-451*

Vertically Stacked SiGe Nanowire Array Channel CMOS Transistors. *Fang, W. W.*, +, *EDL March 2007 211-213*

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Vertically Stacked SiGe Nanowire Array Channel CMOS Transistors. *Fang, W. W.*, +, *EDL March 2007 211-213*

Charge Trapping and TDDDB Characteristics of Ultrathin MOCVD HfO₂ Gate Dielectric on Nitrided Germanium. *Bai, W.*, +, *EDL May 2007 369-372*

Improved Ge Surface Passivation With Ultrathin SiO_x Enabling High-Mobility Surface Channel pMOSFETs Featuring a HfSiO/WN Gate Stack. *Joshi, S.*, +, *EDL April 2007 308-311*

Investigation of Carrier Transport in Germanium MOSFETs With WN/Al₂O₃/AlN Gate Stacks. *Ritenour, A.*, +, *EDL Aug. 2007 746-749*

Low-Frequency Noise Assessment of Silicon Passivated Ge pMOSFETs With TiN/TaN/ HfO₂ Gate Stack. *Guo, W.*, +, *EDL April 2007 288-291*

P-Channel Germanium FinFET Based on Rapid Melt Growth. *Feng, J.*, +, *EDL July 2007 637-639*

Gettering

Improving the Electrical Properties of NILC Poly-Si Films Using a Gettering Substrate. *Hu, C.-M.*, +, *EDL Nov. 2007 1000-1003*

Glass

HgTe Nanocrystal-Based Thin-Film Transistors Fabricated on Glass Substrates. *Kim, H.*, +, *EDL Jan. 2007 42-44*

Amorphous-Silicon Thin-Film Transistors Fabricated at 300 °C on a Free-Standing Foil Substrate of Clear Plastic. *Cherenack, K. H.*, +, *EDL Nov. 2007 1004-1006*

Gold

Fermi-Level Pinning in Nanocrystal Memories. *Hou, T.-H.*, +, *EDL Feb. 2007 103-106*

Gold alloys

Effect of Gate Sinking on the Device Performance of the InGaP/AlGaAs/InGaAs Enhancement-Mode PHEMT. *Chu, L. H.*, +, *EDL Feb. 2007 82-85*

Electrically Bistable Thin-Film Device Based on PVK and GNPs Polymer Material. *Song, Y.*, +, *EDL Feb. 2007 107-110*

Grain boundaries

Impact of Preferential P-Diffusion Along the Grain Boundaries on Fine-Grained Polysilicon Solar Cells. *Carnel, L.*, +, *EDL Oct. 2007 899-901*

A Simple Spacer Technique to Fabricate Poly-Si TFTs With 50-nm Nanowire Channels. *Chang, C.-W.*, +, *EDL Nov. 2007 993-995*

Green's function methods

Simulation of Graphene Nanoribbon Field-Effect Transistors. *Fiori, G.*, +, *EDL Aug. 2007 760-762*

H

HEMT integrated circuits

Effect of a Two-Step Recess Process Using Atomic Layer Etching on the Performance of In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As p-HEMTs. *Kim, T.-W.*, +, *EDL Dec. 2007 1086-1088*

High-Temperature Operation of AlGaIn/GaN HEMTs Direct-Coupled FET Logic (DCFL) Integrated Circuits. *Cai, Y.*, +, *EDL May 2007 328-331*

HEMTs

50-nm T-Gate InAlAs/InGaAs Metamorphic HEMTs With Low Noise and High f_T Characteristics. *Lim, B. O.*, +, *EDL July 2007 546-548*

35-nm Zigzag T-Gate In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As Metamorphic GaAs HEMTs With an Ultrahigh f_{max} of 520 GHz. *Lee, K.-S.*, +, *EDL Aug. 2007 672-675*

Comparison of GaN HEMTs on Diamond and SiC Substrates. *Felbinger, J. G.*, +, *EDL Nov. 2007 948-950*

Investigation of Impact Ionization in InAs-Channel HEMT for High-Speed and Low-Power Applications. *Chang, C. Y.*, +, *EDL Oct. 2007 856-858*

Power Performance of AlGaIn/GaN HEMTs Grown on SiC by Ammonia-MBE at 4 and 10 GHz. *Poblenz, C.*, +, *EDL Nov. 2007 945-947*

Remarkable Reduction of On-Resistance by Ion Implantation in GaN/AlGaIn/GaN HEMTs With Low Gate Leakage Current. *Nomoto, K.*, +, *EDL Nov. 2007 939-941*

The Leakage Current of the Schottky Contact on the Mesa Edge of AlGaIn/GaN Heterostructure. *Xu, C.*, +, *EDL Nov. 2007 942-944*

Hafnium compounds

Effect of F₂ Postmetallization Annealing on the Electrical and Reliability Characteristics of HfSiO Gate Dielectric. *Chang, M.*, +, *EDL Jan. 2007 21-23*

A Novel Approach in Separating the Roles of Electrons and Holes in Causing Degradation in Hf-Based MOSFET Devices by Using Stress-Anneal Technique. *Akbar, M. S.*, +, *EDL Feb. 2007 132-134*

Achieving Conduction Band-Edge Effective Work Functions by La₂O₃ Capping of Hafnium Silicates. *Ragnarsson, L.-A.*, +, *EDL June 2007 486-488*

Border-Trap Characterization in High- κ Strained-Si MOSFETs. *Maji, D.*, +, *EDL Aug. 2007 731-733*

Characteristics of Ni/Gd FUSI for NMOS Gate Electrode Applications. *Lee, B.*, +, *EDL July 2007 555-557*

Charge Trapping and TDDDB Characteristics of Ultrathin MOCVD HfO₂ Gate Dielectric on Nitrided Germanium. *Bai, W.*, +, *EDL May 2007 369-372*

Demonstration of Asymmetric Gate-Oxide Thickness Four-Terminal FinFETs Having Flexible Threshold Voltage and Good Subthreshold Slope. *Masahara, M.*, +, *EDL March 2007 217-219*

Detection of Border Trap Density and Energy Distribution Along the Gate Dielectric Bulk of High- κ Gated MOS Devices. *Lu, C.-Y.*, +, *EDL May 2007 432-435*

Effect of Gate Dopant Diffusion on Leakage Current in n⁺Poly-Si/HfO₂ and Examination of Leakage Paths by Conducting Atomic Force Microscopy. *Yu, X.*, +, *EDL May 2007 373-375*

Effective Work Function Engineering of Ta_xC_y Metal Gate on Hf-Based Dielectrics. *Yen, F. Y.*, +, *EDL March 2007 201-203*

Electrical Properties of nMOSFETs Using the NiSi:Yb FUSI Electrode. *Yu, H. Y.*, +, *EDL Feb. 2007 154-156*

Fluorine Passivation in Gate Stacks of Poly-Si/TaN/HfO₂ (and HfSiO/HfO₂)/Si Through Gate Ion Implantation. *Zhang, M. H.*, +, *EDL March 2007 195-197*

High Mobility Strained Ge pMOSFETs With High- κ /Metal Gate. *Nicholas, G.*, +, *EDL Sept. 2007 825-827*

High- κ Al₂O₃-HfTiO Nanolaminates With Less Than 0.8-nm Equivalent Oxide Thickness. *Mikhelashvili, V.*, +, *EDL Jan. 2007 24-26*

High-Temperature Stable HfLaON p-MOSFETs With High-Work-Function Ir₃Si Gate. *Wu, C. H.*, +, *EDL April 2007 292-294*

Improved Ge Surface Passivation With Ultrathin SiO_x Enabling High-Mobility Surface Channel pMOSFETs Featuring a HfSiO/WN Gate Stack. *Joshi, S.*, +, *EDL April 2007 308-311*

Low-Frequency Noise Assessment of Silicon Passivated Ge pMOSFETs With TiN/TaN/ HfO₂ Gate Stack. *Guo, W.*, +, *EDL April 2007 288-291*

NMOS Compatible Work Function of TaN Metal Gate With Erbium-Oxide-Doped Hafnium Oxide Gate Dielectric. *Chen, J.*, +, *EDL Oct. 2007 862-864*

Nitrogen Incorporation in HfSiO(N)/TaN Gate Stacks: Impact on Performances and NBTI. *Aoulaiche, M.*, +, *EDL July 2007 613-615*

Observation of Metal-Layer Stress on Si Nanowires in Gate-All-Around High- κ /Metal-Gate Device Structures. *Singh, N.*, +, *EDL July 2007 558-561*

Role of Nitrogen Atoms in Reduction of Electron Charge Traps in Hf-Based High- κ Dielectrics. *Umezawa, N.*, +, *EDL May 2007 363-365*

The Application of an Ultrathin ALD HfSiON Cap Layer on SiON Dielectrics for Ni-FUSI CMOS Technology Targeting at Low-Power Applications. *Chang, S. Z.*, +, *EDL July 2007 634-636*

Thickness Scaling and Reliability Comparison for the Inter-Poly High- κ Dielectrics. *Chen, Y.-Y.*, +, *EDL Aug. 2007 700-702*

Yttrium- and Terbium-Based Interlayer on SiO₂ and HfO₂ Gate Dielectrics for Work Function Modulation of Nickel Fully Silicided Gate in nMOSFET. *Lim, A. E.-J.*, +, *EDL June 2007 482-485*

Harmonic analysis

A Planar Gunn Diode Operating Above 100 GHz. *Khalid, A.*, +, *EDL Oct. 2007 849-851*

Heat treatment

Fabrication of Ni Nanocrystal Flash Memories Using a Polymeric Self-Assembly Approach. *Shahrjerdi, D.*, +, *EDL Sept. 2007 793-796*

Heating

Enhanced Thermal Efficiency in Phase-Change Memory Cell by Double GST Thermally Confined Structure. *Chao, D.-S.*, +, *EDL Oct. 2007* 871-873

Heterojunction bipolar transistors

DC Characteristics of AlGaAs/GaAs/GaN HBTs Formed by Direct Wafer Fusion. *Lian, C.*, +, *EDL Jan. 2007* 8-10

InGaAsSb/InP Double Heterojunction Bipolar Transistors Grown by Solid-Source Molecular Beam Epitaxy. *Chen, S.-H.*, +, *EDL Aug. 2007* 679-681

High-Current-Gain InP/GaInP/GaAsSb/InP DHBTs With $f_T = 436$ GHz. *Liu, H. G.*, +, *EDL Oct. 2007* 852-855

Metamorphic Heterostructure InP/GaAsSb/InP HBTs on GaAs Substrates by MOCVD. *Zhou, W.*, +, *EDL July 2007* 539-542

On the Use of a SiGe Spike in the Emitter to Improve the $f_T \times BV_{CEO}$ Product of High-Speed SiGe HBTs. *Choi, L. J.*, +, *EDL April 2007* 270-272

Heterojunctions

Impact of Preferential P-Diffusion Along the Grain Boundaries on Fine-Grained Polysilicon Solar Cells. *Carnel, L.*, +, *EDL Oct. 2007* 899-901

High-Current-Gain InP/GaInP/GaAsSb/InP DHBTs With $f_T = 436$ GHz. *Liu, H. G.*, +, *EDL Oct. 2007* 852-855

High electron mobility transistors

RF-Enhanced Contacts to Wide-Bandgap Devices. *Simin, G.*, +, *EDL Jan. 2007* 2-4

A New Method for Identification and Minimization of Distortion Sources in GaN HEMT Devices Based on Volterra Series Analysis. *Srinidhi, E. R.*, +, *EDL May 2007* 343-345

A Novel Dilute Antimony Channel In_{0.2}Ga_{0.8}AsSb/GaAs HEMT. *Su, K.-H.*, +, *EDL Feb. 2007* 96-99

AlGaIn/GaN HEMTs With Thin InGaIn Cap Layer for Normally Off Operation. *Mizutani, T.*, +, *EDL July 2007* 549-551

Compact Model of Current Collapse in Heterostructure Field-Effect Transistors. *Koudymov, A.*, +, *EDL May 2007* 332-335

Effect of Gate Sinking on the Device Performance of the InGaP/AlGaAs/InGaAs Enhancement-Mode PHEMT. *Chu, L. H.*, +, *EDL Feb. 2007* 82-85

Effect of a Two-Step Recess Process Using Atomic Layer Etching on the Performance of In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As p-HEMTs. *Kim, T.-W.*, +, *EDL Dec. 2007* 1086-1088

Enhanced Gate Swing in InP HEMTs With High Threshold Voltage by Means of InAlAsSb Barrier. *Suemitsu, T.*, +, *EDL Aug. 2007* 669-671

Fabrication of 0.15- μ m Γ -Shaped Gate In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As Metamorphic HEMTs Using DUV Lithography and Tilt Dry-Etching Technique. *Lien, Y.-C.*, +, *EDL Feb. 2007* 93-95

Hot-Phonon Effect on the Electrothermal Behavior of Submicrometer III-V HEMTs. *Sadi, T.*, +, *EDL Sept. 2007* 787-789

Normally Off AlGaIn/GaN Low-Density Drain HEMT (LDD-HEMT) With Enhanced Breakdown Voltage and Reduced Current Collapse. *Song, D.*, +, *EDL March 2007* 189-191

RF Power Measurements of InAlIn/GaN Unstrained HEMTs on SiC Substrates at 10 GHz. *Jessen, G. H.*, +, *EDL May 2007* 354-356

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Selectively Doped High-Power AlGaIn/InGaIn/GaN MOS-DHFET. *Adivarahan, V.*, +, *EDL March 2007* 192-194

Submicrometer Copper T-Gate AlGaIn/GaN HFETs: The Gate Metal Stack Effect. *Sun, H. F.*, +, *EDL May 2007* 350-353

Time-Resolved Temperature Measurement of AlGaIn/GaN Electronic Devices Using Micro-Raman Spectroscopy. *Kuball, M.*, +, *EDL Feb. 2007* 86-89

Ultrahigh-Speed 0.5 V Supply Voltage In_{0.7}Ga_{0.3}As Quantum-Well Transistors on Silicon Substrate. *Datta, S.*, +, *EDL Aug. 2007* 685-687

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Effect of F₂ Postmetallization Annealing on the Electrical and Reliability Characteristics of HfSiO Gate Dielectric. *Chang, M.*, +, *EDL Jan. 2007* 21-23

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Effective Work Function Engineering of Ta_xC_y Metal Gate on Hf-Based Dielectrics. *Yen, F. Y.*, +, *EDL March 2007* 201-203

Electrical Characterization of ZrO₂/Si Interface Properties in MOSFETs With ZrO₂ Gate Dielectrics. *Liu, C.-H.*, +, *EDL Jan. 2007* 62-64

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High Mobility Strained Ge pMOSFETs With High- κ /Metal Gate. *Nicholas, G.*, +, *EDL Sept. 2007* 825-827

Improved Ge Surface Passivation With Ultrathin SiO_x Enabling High-Mobility Surface Channel pMOSFETs Featuring a HfSiO/WN Gate Stack. *Joshi, S.*, +, *EDL April 2007* 308-311

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Hot-Carrier Effects in Strained n-Channel Transistor With Silicon-Carbon (Si_{1-y}C_y) Source/Drain Stressors and Its Orientation Dependence. *Ang, K.-W.*, +, *EDL Nov. 2007* 996-999

New Operating Mode Based on Electron/Hole Profile Matching in Nitride-Based Nonvolatile Memories. *Furnemont, A.*, +, *EDL April 2007* 276-278

Novel Single Polysilicon EEPROM Cell With Dual Work Function Floating Gate. *Na, K.-Y.*, +, *EDL Feb. 2007* 151-153

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On-Resistance Degradations for Different Stress Conditions in High-Voltage pEDLMOS Transistor With Thick Gate Oxide. *Sun, W.*, +, *EDL July 2007* 631-633

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The Preparation of Nanocrystalline Silicon by Plasma-Enhanced Hydrogenation for the Fabrication of Light-Emitting Diodes. *Jamei, M.*, +, *EDL March 2007 207-210*

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Improved Stability of High-Performance ZnO/ZnMgO Hetero-MISFETs. *Sasa, S.*, +, *EDL July 2007 543-545*

I**IEEE**

2007 Golden List of Reviewers. , *EDL Dec. 2007 1062-1075*

II-VI semiconductors

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Power Stability of AlGaIn/GaN HFETs at 20 W/mm in the Pinched-Off Operation Mode. *Koudymov, A.*, +, *EDL Jan. 2007 5-7*

1- μm Enhancement Mode GaAs N-Channel MOSFETs With Transconductance Exceeding 250 mS/mm. *Rajagopalan, K.*, +, *EDL Feb. 2007 100-102*

1.3- μm GaInAsN Vertical-Cavity Surface-Emitting Lasers by Oxide-Planarized and Surface-Relief Processes for Single-Mode Operation. *Lee, F.-M.*, +, *EDL Feb. 2007 120-122*

InGaAsSb/InP Double Heterojunction Bipolar Transistors Grown by Solid-Source Molecular Beam Epitaxy. *Chen, S.-H.*, +, *EDL Aug. 2007 679-681*

A 0.2-W Heterostructure Barrier Varactor Frequency Tripler at 113 GHz. *Vukusic, J.*, +, *EDL May 2007 340-342*

A New Method for Identification and Minimization of Distortion Sources in GaN HEMT Devices Based on Volterra Series Analysis. *Srinidhi, E. R.*, +, *EDL May 2007 343-345*

A Novel Dilute Antimony Channel In_{0.2}Ga_{0.8}AsSb/GaAs HEMT. *Su, K.-H.*, +, *EDL Feb. 2007 96-99*

AlGaIn Photodetectors Prepared on Si Substrates. *Chiu, Y. Z.*, +, *EDL April 2007 264-266*

AlGaIn/GaN HEMTs With Thin InGaIn Cap Layer for Normally Off Operation. *Mizutani, T.*, +, *EDL July 2007 549-551*

Compact Model of Current Collapse in Heterostructure Field-Effect Transistors. *Koudymov, A.*, +, *EDL May 2007 332-335*

DC Characteristics of AlGaAs/GaAs/GaN HBTs Formed by Direct Wafer Fusion. *Lian, C.*, +, *EDL Jan. 2007 8-10*

Fabrication of 0.15- μm Γ -Shaped Gate In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As Metamorphic HEMTs Using DUV Lithography and Tilt Dry-Etching Technique. *Lien, Y.-C.*, +, *EDL Feb. 2007 93-95*

High-Speed InGaP/GaAs p-i-n Photodiodes With Wide Spectral Range. *Wu, M.-C.*, +, *EDL Sept. 2007 797-799*

High-Temperature Operation of AlGaIn/GaN HEMTs Direct-Coupled FET Logic (DCFL) Integrated Circuits. *Cai, Y.*, +, *EDL May 2007 328-331*

Hot-Phonon Effect on the Electrothermal Behavior of Submicrometer III-V HEMTs. *Sadi, T.*, +, *EDL Sept. 2007 787-789*

Improved Reliability and ESD Characteristics of Flip-Chip GaN-Based EDLs With Internal Inverse-Parallel Protection Diodes. *Shei, S.-C.*, +, *EDL May 2007 346-349*

Metamorphic Heterostructure InP/GaAsSb/InP HBTs on GaAs Substrates by MOCVD. *Zhou, W.*, +, *EDL July 2007 539-542*

Normally Off AlGaIn/GaN Low-Density Drain HEMT (LDD-HEMT) With Enhanced Breakdown Voltage and Reduced Current Collapse. *Song, D.*, +, *EDL March 2007 189-191*

ON-Resistance Modulation of High Voltage GaN HEMT on Sapphire Substrate Under High Applied Voltage. *Saito, W.*, +, *EDL Aug. 2007 676-678*

RF Power Measurements of InAlIn/GaN Unstrained HEMTs on SiC Substrates at 10 GHz. *Jessen, G. H.*, +, *EDL May 2007 354-356*

Robust Coupled-Quantum-Well Structure for Use in Electrorefraction Modulators. *Ristic, S.*, +, *EDL Jan. 2007 30-32*

Selectively Doped High-Power AlGaIn/GaN MOS-DHFET. *Adivarahan, V.*, +, *EDL March 2007 192-194*

Silicon Dioxide-Encapsulated High-Voltage AlGaIn/GaN HFETs for Power-Switching Applications. *Tipirneni, N.*, +, *EDL Sept. 2007 784-786*

Submicrometer Copper T-Gate AlGaIn/GaN HFETs: The Gate Metal Stack Effect. *Sun, H. F.*, +, *EDL May 2007 350-353*

Time-Resolved Temperature Measurement of AlGaIn/GaN Electronic Devices Using Micro-Raman Spectroscopy. *Kuball, M.*, +, *EDL Feb. 2007 86-89*

Ultrahigh-Speed 0.5 V Supply Voltage In_{0.7}Ga_{0.3}As Quantum-Well Transistors on Silicon Substrate. *Datta, S.*, +, *EDL Aug. 2007 685-687*

Image sensors

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Improved Reliability by Reduction of Hot-Electron Damage in the Vertical Impact-Ionization MOSFET (I-MOS). *Abelein, U.*, +, *EDL Jan. 2007 65-67*

Experimental and TCAD Investigation of the Two Components of the Impact Ionization MOSFET (IMOS) Switching. *Mayer, F.*, +, *EDL July 2007 619-621*

Impact ionization

Body Thickness Dependence of Impact Ionization in a Multiple-Gate FinFET. *Han, J.-W.*, +, *EDL July 2007 625-627*

Hot-Carrier Effects in Strained n-Channel Transistor With Silicon-Carbon (Si_{1-y}C_y) Source/Drain Stressors and Its Orientation Dependence. *Ang, K.-W.*, +, *EDL Nov. 2007 996-999*

Investigation of Impact Ionization in InAs-Channel HEMT for High-Speed and Low-Power Applications. *Chang, C. Y.*, +, *EDL Oct. 2007 856-858*

On the Enhanced Impact Ionization in Uniaxial Strained p-MOSFETs. *Su, P.*, +, *EDL July 2007 649-651*

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Impacts of Dopant Segregation on the Performance and Interface-State Density of the MOSFET With FUSI NiSi Gate. *Liu, J.*, +, *EDL Jan. 2007 11-13*

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Robust Coupled-Quantum-Well Structure for Use in Electrorefraction Modulators. *Ristic, S.*, +, *EDL Jan. 2007 30-32*

1.3- μm GaInAsN Vertical-Cavity Surface-Emitting Lasers by Oxide-Planarized and Surface-Relief Processes for Single-Mode Operation. *Lee, F.-M.*, +, *EDL Feb. 2007 120-122*

InGaAsSb/InP Double Heterojunction Bipolar Transistors Grown by Solid-Source Molecular Beam Epitaxy. *Chen, S.-H.*, +, *EDL Aug. 2007 679-681*

A 0.2-W Heterostructure Barrier Varactor Frequency Tripler at 113 GHz. *Vukusic, J.*, +, *EDL May 2007 340-342*

A Novel Dilute Antimony Channel In_{0.2}Ga_{0.8}AsSb/GaAs HEMT. *Su, K.-H.*, +, *EDL Feb. 2007 96-99*

Effect of Gate Sinking on the Device Performance of the InGaP/AlGaAs/InGaAs Enhancement-Mode PHEMT. *Chu, L. H.*, +, *EDL Feb. 2007 82-85*

Enhanced Gate Swing in InP HEMTs With High Threshold Voltage by Means of InAlAsSb Barrier. *Suemitsu, T.*, +, *EDL Aug. 2007 669-671*

Fabrication of 0.15- μm Γ -Shaped Gate In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As Metamorphic HEMTs Using DUV Lithography and Tilt Dry-Etching Technique. *Lien, Y.-C.*, +, *EDL Feb. 2007 93-95*

Fast Thin-Film Transistor Circuits Based on Amorphous Oxide Semiconductor. *Ofuji, M.*, +, *EDL April 2007 273-275*

High Transconductance MISFET With a Single InAs Nanowire Channel. *Do, Q.-T.*, +, *EDL Aug. 2007 682-684*

High-Speed InGaP/GaAs p-i-n Photodiodes With Wide Spectral Range. *Wu, M.-C.*, +, *EDL Sept. 2007 797-799*

Metamorphic Heterostructure InP/GaAsSb/InP HBTs on GaAs Substrates by MOCVD. *Zhou, W.*, +, *EDL July 2007 539-542*

Observation of Threshold-Voltage Instability in Single-Crystal Silicon TFTs on Flexible Plastic Substrate. *Yuan, H.-C.*, +, *EDL July 2007 590-592*

RF Power Measurements of InAlIn/GaN Unstrained HEMTs on SiC Substrates at 10 GHz. *Jessen, G. H.*, +, *EDL May 2007 354-356*

Selectively Doped High-Power AlGaIn/GaN MOS-DHFET. *Adivarahan, V.*, +, *EDL March 2007 192-194*

The Preparation of Nanocrystalline Silicon by Plasma-Enhanced Hydrogenation for the Fabrication of Light-Emitting Diodes. *Jamei, M.*, +, *EDL March 2007 207-210*

- Ultrahigh-Speed 0.5 V Supply Voltage $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ Quantum-Well Transistors on Silicon Substrate. *Datta, S.*, +, *EDL Aug. 2007 685-687*
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- Indium phosphide**
Investigation of Impact Ionization in InAs-Channel HEMT for High-Speed and Low-Power Applications. *Chang, C. Y.*, +, *EDL Oct. 2007 856-858*
High-Current-Gain InP/GaInP/GaAsSb/InP DHBTs With $f_T = 436$ GHz. *Liu, H. G.*, +, *EDL Oct. 2007 852-855*
- Indium tin oxide**
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- Inductors**
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Effect of Substrate Parasitic Inductance on Silicon-Based Transmission Lines and On-Chip Inductors. *Huang, F.*, +, *EDL Nov. 2007 1025-1028*
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- Infrared sources**
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Effect of Substrate Parasitic Inductance on Silicon-Based Transmission Lines and On-Chip Inductors. *Huang, F.*, +, *EDL Nov. 2007 1025-1028*
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Border-Trap Characterization in High- κ Strained-Si MOSFETs. *Maji, D.*, +, *EDL Aug. 2007 731-733*
Detection of Border Trap Density and Energy Distribution Along the Gate Dielectric Bulk of High- κ Gated MOS Devices. *Lu, C.-Y.*, +, *EDL May 2007 432-435*
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Investigation of Carrier Transport in Germanium MOSFETs With $\text{WN}/\text{Al}_2\text{O}_3/\text{AlN}$ Gate Stacks. *Ritenour, A.*, +, *EDL Aug. 2007 746-749*
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- Ion implantation**
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Defect Passivation by Selenium-Ion Implantation for Poly-Si Thin Film Transistors. *Lai, J.*, +, *EDL Aug. 2007 725-727*
Dual-Bit/Cell SONOS Flash EEPROMs: Impact of Channel Engineering on Programming Speed and Bit Coupling Effect. *Datta, A.*, +, *EDL May 2007 446-448*
Fluorine Passivation in Gate Stacks of Poly-Si/TaN/HfO₂ (and HfSiON/HfO₂)/Si Through Gate Ion Implantation. *Zhang, M. H.*, +, *EDL March 2007 195-197*
High-Temperature Stable HfLaON p-MOSFETs With High-Work-Function Ir_3Si Gate. *Wu, C. H.*, +, *EDL April 2007 292-294*

Impacts of Notched-Gate Structure on Contact Etch Stop Layer (CESL) Stressed 90-nm nMOSFET. *Lin, C.-T.*, +, *EDL May 2007 376-378*

Reduction of Threshold Voltage by Diffusion Control Technique in p-MISFETs Using Poly-Si/TiN/HfSiON Gate Stacks. *Kawahara, T.*, +, *EDL Oct. 2007 868-870*

Remarkable Reduction of On-Resistance by Ion Implantation in GaN/AlGaIn/GaN HEMTs With Low Gate Leakage Current. *Nomoto, K.*, +, *EDL Nov. 2007 939-941*

Schottky-Barrier Height Tuning by Means of Ion Implantation Into Preformed Silicide Films Followed by Drive-In Anneal. *Zhang, Z.*, +, *EDL July 2007 565-568*

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High-Temperature Stable HfLaON p-MOSFETs With High-Work-Function Ir₃Si Gate. *Wu, C. H.*, +, *EDL April 2007 292-294*

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A New Lateral-IGBT Structure With a Wider Safe Operating Area. *Bake-root, B.*, +, *EDL May 2007 416-418*

Ar Annealing for Suppression of Gate Oxide Thinning at Shallow Trench Isolation Edge. *Ohashi, T.*, +, *EDL July 2007 562-564*

The Effect of Trapped Charge Distributions on Data Retention Characteristics of NAND Flash Memory Cells. *Park, M.*, +, *EDL Aug. 2007 750-752*

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Junction gate field effect transistors

1000-V 9.1-mΩ · cm² Normally Off 4H-SiC Lateral RESURF JFET for Power Integrated Circuit Applications. *Zhang, Y.*, +, *EDL May 2007 404-407*

Pinch-Off Voltage-Adjustable High-Voltage Junction Field-Effect Transistor. *Liauw, C.-W.*, +, *EDL Aug. 2007 737-739*

Junctions

Impact of Preferential P-Diffusion Along the Grain Boundaries on Fine-Grained Polysilicon Solar Cells. *Carnel, L.*, +, *EDL Oct. 2007 899-901*

1200-V 5.2-mΩ · cm² 4H-SiC BJTs With a High Common-Emitter Current Gain. *Lee, H.-S.*, +, *EDL Nov. 2007 1007-1009*

Improved Electrical Characteristics of Ge-on-Si Field-Effect Transistors With ControlEDL Ge Epitaxial Layer Thickness on Si Substrates. *Oh, J.*, +, *EDL Nov. 2007 1044-1046*

Monolithically Integrated Logic NOR Gate Based on GaAs/AlGaAs Three-Terminal Junctions. *Muller, C. R.*, +, *EDL Oct. 2007 859-861*

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EDL displays

Flexible Full-Color AMOEDL on Ultrathin Metal Foil. *Jeong, J. K.*, +, *EDL May 2007 389-391*

Laminates

High-κ Al₂O₃-HfTiO Nanolaminates With Less Than 0.8-nm Equivalent Oxide Thickness. *Mikhelashvili, V.*, +, *EDL Jan. 2007 24-26*

Lanthanum compounds

High-Temperature Stable HfLaON p-MOSFETs With High-Work-Function Ir₃Si Gate. *Wu, C. H.*, +, *EDL April 2007 292-294*

Achieving Conduction Band-Edge Effective Work Functions by La₂O₃ Capping of Hafnium Silicates. *Ragnarsson, L.-A.*, +, *EDL June 2007 486-488*

Laser beam annealing

Crystallization of Double-Layered Silicon Thin Films by Solid Green Laser Annealing for High-Performance Thin-Film Transistors. *Sugawara, Y.*, +, *EDL May 2007 395-397*

Laser materials processing

Enhanced Hole Mobility and Reliability of Panel Epi-Like Silicon Transistors Using Backside Green Laser Activation. *Lin, Y.-T.*, +, *EDL Sept. 2007 790-792*

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High-Performance Self-Aligned Bottom-Gate Low-Temperature Poly-Silicon Thin-Film Transistors With Excimer Laser Crystallization. *Tsai, C.-C.*, +, *EDL July 2007 599-602*

High-Performance Short-Channel Double-Gate Low-Temperature Polysilicon Thin-Film Transistors Using Excimer Laser Crystallization. *Tsai, C.-C.*, +, *EDL Nov. 2007 1010-1013*

Layout

Active Pixel Concept Combined With Organic Photodiode for Imaging Devices. *Tedde, S.*, +, *EDL Oct. 2007 893-895*

Design of On-Chip Transformer With Various Coil Widths to Achieve Minimal Metal Resistance. *Hsu, H.-M.*, +, *EDL Nov. 2007 1029-1032*

Leakage current

A New Degradation Mechanism in High-Voltage SiC Power MOSFETs. *Agarwal, A.*, +, *EDL July 2007 587-589*

High-Performance and Low-Temperature-Compatible p-Channel Polycrystalline-Silicon TFTs Using Hafnium-Silicate Gate Dielectric. *Yang, M.-J.*, +, *EDL Oct. 2007 902-904*

Improving the Electrical Properties of NILC Poly-Si Films Using a Gettering Substrate. *Hu, C.-M.*, +, *EDL Nov. 2007 1000-1003*

Metal-Oxide-High-κ Dielectric-Oxide-Semiconductor (MOHOS) Capacitors and Field-Effect Transistors for Memory Applications. *Hsu, H.*, +, *EDL Nov. 2007 964-966*

NMOS Compatible Work Function of TaN Metal Gate With Erbium-Oxide-Doped Hafnium Oxide Gate Dielectric. *Chen, J.*, +, *EDL Oct. 2007 862-864*

The Leakage Current of the Schottky Contact on the Mesa Edge of AlGaIn/GaN Heterostructure. *Xu, C.*, +, *EDL Nov. 2007 942-944*

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Long Retention of Gain-Cell Dynamic Random Access Memory With Undoped Memory Node. *Nishiguchi, K.*, +, *EDL Jan. 2007 48-50*

Accurate Series-Resistance Extraction From Capacitor Using Time Domain Reflectometry. *Wang, Y.*, +, *EDL April 2007 279-281*

Charge Trapping and TDDB Characteristics of Ultrathin MOCVD HfO₂ Gate Dielectric on Nitrided Germanium. *Bai, W.*, +, *EDL May 2007 369-372*

Effect of Gate Dopant Diffusion on Leakage Current in n⁺Poly-Si/HfO₂ and Examination of Leakage Paths by Conducting Atomic Force Microscopy. *Yu, X.*, +, *EDL May 2007 373-375*

Effect of Gate Sinking on the Device Performance of the InGaP/AlGaAs/InGaAs Enhancement-Mode PHEMT. *Chu, L. H.*, +, *EDL Feb. 2007 82-85*

Experimental Study of Data Retention in Nitride Memories by Temperature and Field Acceleration. *Compagnoni, C. M.*, +, *EDL July 2007 628-630*

High Mobility Strained Ge pMOSFETs With High-κ /Metal Gate. *Nicholas, G.*, +, *EDL Sept. 2007 825-827*

High-Temperature Leakage Improvement in Metal-Insulator-Metal Capacitors by Work-Function Tuning. *Chiang, K. C.*, +, *EDL March 2007 235-237*

High-Temperature Stable HfLaON p-MOSFETs With High-Work-Function Ir₃Si Gate. *Wu, C. H.*, +, *EDL April 2007 292-294*

Impact of CF₄ Plasma Treatment on GaN. *Chu, R.*, +, *EDL Sept. 2007 781-783*

Impact of High-κ Offset Spacer in 65-nm Node SOI Devices. *Ma, M.-W.*, +, *EDL March 2007 238-241*

Impact of High-κ Gate Dielectrics on the Device and Circuit Performance of Nanoscale FinFETs. *Manoj, C. R.*, +, *EDL April 2007 295-297*

Investigation and Localization of the SiGe Source/Drain (S/D) Strain-Induced Defects in PMOSFET With 45-nm CMOS Technology. *Cheng, C. Y.*, +, *EDL May 2007 408-411*

P-Channel Germanium FinFET Based on Rapid Melt Growth. *Feng, J.*, +, *EDL July 2007 637-639*

Submicrometer Copper T-Gate AlGaIn/GaN HFETs: The Gate Metal Stack Effect. *Sun, H. F.*, +, *EDL May 2007 350-353*

The Effects of the Injection-Channel Velocity on the Gate Leakage Current of Nanoscale MOSFETs. *Mao, L.*, *EDL Feb. 2007 161-163*

Thickness Scaling and Reliability Comparison for the Inter-Poly High-κ Dielectrics. *Chen, Y.-Y.*, +, *EDL Aug. 2007 700-702*

Time-Domain-Reflectometry for Capacitance-Voltage Measurement With Very High Leakage Current. *Wang, Y.*, +, *EDL Jan. 2007 51-53*

Life testing

Lifetime Extension of RF MEMS Direct Contact Switches in Hot Switching Operations by Ball Grid Array Dimple Design. *Chow, L. L. W.*, +, *EDL June 2007 479-481*

Light absorption

High-Responsivity Photodetector in Standard SiGe BiCMOS Technology. *Lai, K.-S.*, +, *EDL Sept. 2007 800-802*

Light emitting diodes

The Preparation of Nanocrystalline Silicon by Plasma-Enhanced Hydrogenation for the Fabrication of Light-Emitting Diodes. *Jamei, M.*, +, *EDL March 2007 207-210*

- A Simple and Effective Approach to Improve the Output Linearity of Switched-Current AMOEDL Pixel Circuitry. *Guo, X.*, +, *EDL Oct. 2007 887-889*
- Electrical Compensation of OEDL Luminance Degradation. *Chaji, G. R.*, +, *EDL Dec. 2007 1108-1110*
- Implementation of Side Effects in Thermal Characterization of RGB Full-Color EDLs. *Kim, L.*, +, *EDL July 2007 578-580*
- Improved Reliability and ESD Characteristics of Flip-Chip GaN-Based EDLs With Internal Inverse-Parallel Protection Diodes. *Shei, S.-C.*, +, *EDL May 2007 346-349*
- Strong Efficiency Improvement of SOI-EDLs Through Carrier Confinement. *Hoang, T.*, +, *EDL May 2007 383-385*
- Linearity**
- A Simple and Effective Approach to Improve the Output Linearity of Switched-Current AMOEDL Pixel Circuitry. *Guo, X.*, +, *EDL Oct. 2007 887-889*
- Lithography**
- High-Performance Self-Aligned Bottom-Gate Low-Temperature Poly-Silicon Thin-Film Transistors With Excimer Laser Crystallization. *Tsai, C.-C.*, +, *EDL July 2007 599-602*
- Logic circuits**
- High-Temperature Operation of AlGaIn/GaN HEMTs Direct-Coupled FET Logic (DCFL) Integrated Circuits. *Cai, Y.*, +, *EDL May 2007 328-331*
- Logic gates**
- 1000-V $9.1\text{-m}\Omega \cdot \text{cm}^2$ Normally Off 4H-SiC Lateral RESURF JFET for Power Integrated Circuit Applications. *Zhang, Y.*, +, *EDL May 2007 404-407*
- 35-nm Zigzag T-Gate $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ Metamorphic GaAs HEMTs With an Ultrahigh f_{max} of 520 GHz. *Lee, K.-S.*, +, *EDL Aug. 2007 672-675*
- 50-nm T-Gate InAlAs/InGaAs Metamorphic HEMTs With Low Noise and High f_T Characteristics. *Lim, B. O.*, +, *EDL July 2007 546-548*
- OFF-State Avalanche-Breakdown-Induced ON-Resistance Degradation in Lateral DMOS Transistors. *Chen, J. F.*, +, *EDL Nov. 2007 1033-1035*
- A New Degradation Mechanism in High-Voltage SiC Power MOSFETs. *Agarwal, A.*, +, *EDL July 2007 587-589*
- A Novel Single Polysilicon EEPROM Cell With a Polyfinger Capacitor. *Na, K.-Y.*, +, *EDL Nov. 2007 1047-1049*
- A Simple Spacer Technique to Fabricate Poly-Si TFTs With 50-nm Nanowire Channels. *Chang, C.-W.*, +, *EDL Nov. 2007 993-995*
- A Simple and Effective Approach to Improve the Output Linearity of Switched-Current AMOEDL Pixel Circuitry. *Guo, X.*, +, *EDL Oct. 2007 887-889*
- Achieving Low- V_T Ni-FUSI CMOS by Ultra-Thin Dy_2O_3 Capping of Hafnium Silicate Dielectrics. *Velooso, A.*, +, *EDL Nov. 2007 980-983*
- Active Pixel Concept Combined With Organic Photodiode for Imaging Devices. *Tedde, S.*, +, *EDL Oct. 2007 893-895*
- Amorphous-Silicon Thin-Film Transistors Fabricated at 300 °C on a Free-Standing Foil Substrate of Clear Plastic. *Cherenack, K. H.*, +, *EDL Nov. 2007 1004-1006*
- CMOS Inverter Based on Gate-All-Around Silicon-Nanowire MOSFETs Fabricated Using Top-Down Approach. *Rustagi, S. C.*, +, *EDL Nov. 2007 1021-1024*
- Constant Bias Stress Effects on Threshold Voltage of Pentacene Thin-Film Transistors Employing Polyvinylphenol Gate Dielectric. *Kim, T. H.*, +, *EDL Oct. 2007 874-876*
- Demonstration of Low V_i Ni-FUSI N-MOSFETs With SiON Dielectrics by Using a Dy_2O_3 Cap Layer. *Yu, H. Y.*, +, *EDL Nov. 2007 957-959*
- Demonstration of Metal-Gated Low V_i n-MOSFETs Using a Poly-Si/TaN/ Dy_2O_3 /SiON Gate Stack With a ScaEDL EOT Value. *Yu, H. Y.*, +, *EDL July 2007 656-658*
- Effect of SiN_x Gate Dielectric Deposition Power and Temperature on a-Si:H TFT Stability. *Kattamis, A. Z.*, +, *EDL July 2007 606-608*
- Effects of Sulfur Passivation on Germanium MOS Capacitors With HfON Gate Dielectric. *Xie, R.*, +, *EDL Nov. 2007 976-979*
- High-Performance Self-Aligned Bottom-Gate Low-Temperature Poly-Silicon Thin-Film Transistors With Excimer Laser Crystallization. *Tsai, C.-C.*, +, *EDL July 2007 599-602*
- High-Performance Short-Channel Double-Gate Low-Temperature Polysilicon Thin-Film Transistors Using Excimer Laser Crystallization. *Tsai, C.-C.*, +, *EDL Nov. 2007 1010-1013*
- High-Performance and Low-Temperature-Compatible p-Channel Polycrystalline-Silicon TFTs Using Hafnium-Silicate Gate Dielectric. *Yang, M.-J.*, +, *EDL Oct. 2007 902-904*
- Hot-Carrier Effects in Strained n-Channel Transistor With Silicon-Carbon ($\text{Si}_{1-y}\text{C}_y$) Source/Drain Stressors and Its Orientation Dependence. *Ang, K.-W.*, +, *EDL Nov. 2007 996-999*
- Improved Electrical Characteristics of Ge-on-Si Field-Effect Transistors With Controlled Ge Epitaxial Layer Thickness on Si Substrates. *Oh, J.*, +, *EDL Nov. 2007 1044-1046*
- Improved Stability of High-Performance ZnO/ZnMgO Hetero-MISFETs. *Sasa, S.*, +, *EDL July 2007 543-545*
- Investigation of Carrier Transport in Germanium MOSFETs With $\text{WN}/\text{Al}_2\text{O}_3/\text{AlN}$ Gate Stacks. *Ritenour, A.*, +, *EDL Aug. 2007 746-749*
- Investigation of Impact Ionization in InAs-Channel HEMT for High-Speed and Low-Power Applications. *Chang, C. Y.*, +, *EDL Oct. 2007 856-858*
- Low-Temperature Passivation of Amorphous-Silicon Thin-Film Transistors With Supercritical Fluids. *Tsai, C.-T.*, +, *EDL July 2007 584-586*
- Low-Temperature Transport Characteristics and Quantum-Confinement Effects in Gate-All-Around Si-Nanowire N-MOSFET. *Rustagi, S. C.*, +, *EDL Oct. 2007 909-912*
- Mobility Modeling and Its Extraction Technique for Manufacturing Strained-Si MOSFETs. *Wang, J.-S.*, +, *EDL Nov. 2007 1040-1043*
- Monolithically Integrated Logic NOR Gate Based on GaAs/AlGaAs Three-Terminal Junctions. *Muller, C. R.*, +, *EDL Oct. 2007 859-861*
- N-Channel (110)-Sidewall Strained FinFETs With Silicon-Carbon Source and Drain Stressors and Tensile Capping Layer. *Liow, T.-Y.*, +, *EDL Nov. 2007 1014-1017*
- NMOS Compatible Work Function of TaN Metal Gate With Erbium-Oxide-Doped Hafnium Oxide Gate Dielectric. *Chen, J.*, +, *EDL Oct. 2007 862-864*
- On the Enhanced Impact Ionization in Uniaxial Strained p-MOSFETs. *Su, P.*, +, *EDL July 2007 649-651*
- On the Low-Frequency Noise of pMOSFETs With Embedded SiGe Source/Drain and Fully Silicided Metal Gate. *Simoen, E.*, +, *EDL Nov. 2007 987-989*
- On the Origin of the Excess Low-Frequency Noise in Graded-Channel Silicon-on-Insulator nMOSFETs. *Simoen, E.*, +, *EDL Oct. 2007 919-921*
- Reduction of Threshold Voltage by Diffusion Control Technique in p-MISFETs Using Poly-Si/TiN/HfSiON Gate Stacks. *Kawahara, T.*, +, *EDL Oct. 2007 868-870*
- Solution-Processed TIPS-Pentacene Organic Thin-Film-Transistor Circuits. *Park, S. K.*, +, *EDL Oct. 2007 877-879*
- Solution-Processed n-Type Organic Field-Effect Transistors With High ON/OFF Current Ratios Based on Fullerene Derivatives. *Tiwari, S. P.*, +, *EDL Oct. 2007 880-883*
- Strained n-Channel Transistors With Silicon Source and Drain Regions and Embedded Silicon/Germanium as Strain-Transfer Structure. *Ang, K.-W.*, +, *EDL July 2007 609-612*
- Strained p-Channel FinFETs With Extended Π -Shaped Silicon-Germanium Source and Drain Stressors. *Tan, K.-M.*, +, *EDL Oct. 2007 905-908*
- Submicrometer Inversion-Type Enhancement-Mode InGaAs MOSFET With Atomic-Layer-Deposited Al_2O_3 as Gate Dielectric. *Xuan, Y.*, +, *EDL Nov. 2007 935-938*
- The Origin of Electron Mobility Enhancement in Strained MOSFETs. *Hadjisavvas, G.*, +, *EDL Nov. 2007 1018-1020*
- Trigate FET Device Characteristics Improvement Using a Hydrogen Anneal Process With a Novel Hard Mask Approach. *Zaman, R. J.*, +, *EDL Oct. 2007 916-918*
- Low-power electronics**
- Source/Drain Extension Region Engineering in FinFETs for Low-Voltage Analog Applications. *Kranti, A.*, +, *EDL Feb. 2007 139-141*
- 1000-V $9.1\text{-m}\Omega \cdot \text{cm}^2$ Normally Off 4H-SiC Lateral RESURF JFET for Power Integrated Circuit Applications. *Zhang, Y.*, +, *EDL May 2007 404-407*
- A Novel Dual-Doping Floating-Gate (DDFG) Flash Memory Featuring Low Power and High Reliability Application. *Li, Y.*, +, *EDL July 2007 622-624*
- Cointegration of High-Performance Tied-Gate Three-Terminal FinFETs and Variable Threshold-Voltage Independent-Gate Four-Terminal FinFETs With Asymmetric Gate-Oxide Thicknesses. *Liu, Y.*, +, *EDL June 2007 517-519*
- Sub-1-V Supply Self-Adaptive CMOS Image Sensor Cell With 86-dB Dynamic Range. *Lee, S.*, +, *EDL June 2007 492-494*
- The Application of an Ultrathin ALD HfSiON Cap Layer on SiON Dielectrics for Ni-FUSI CMOS Technology Targeting at Low-Power Applications. *Chang, S. Z.*, +, *EDL July 2007 634-636*
- Luminescent devices**
- Strong Efficiency Improvement of SOI-EDLs Through Carrier Confinement. *Hoang, T.*, +, *EDL May 2007 383-385*

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50-nm T-Gate InAlAs/InGaAs Metamorphic HEMTs With Low Noise and High f_T Characteristics. *Lim, B. O.*, +, *EDL July 2007 546-548*

35-nm Zigzag T-Gate In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As Metamorphic GaAs HEMTs With an Ultrahigh f_{max} of 520 GHz. *Lee, K.-S.*, +, *EDL Aug. 2007 672-675*

MIM devices

High-Performance Metal-Insulator-Metal Capacitors Using Amorphous BaSm₂Ti₄O₁₂ Thin Film. *Jeong, Y. H.*, +, *EDL Jan. 2007 17-20*

Electrically Bistable Thin-Film Device Based on PVK and GNPs Polymer Material. *Song, Y.*, +, *EDL Feb. 2007 107-110*

High-Temperature Leakage Improvement in Metal-Insulator-Metal Capacitors by Work-Function Tuning. *Chiang, K. C.*, +, *EDL March 2007 235-237*
Improved High-Temperature Leakage in High-Density MIM Capacitors by Using a TiLaO Dielectric and an Ir Electrode. *Cheng, C. H.*, +, *EDL Dec. 2007 1095-1097*

Room-Temperature Deposited Titanium Silicate Thin Films for MIM Capacitor Applications. *Brassard, D.*, +, *EDL April 2007 261-263*

Use of a High-Work-Function Ni Electrode to Improve the Stress Reliability of Analog SrTiO₃ Metal-Insulator-Metal Capacitors. *Chiang, K. C.*, +, *EDL Aug. 2007 694-696*

MIS devices

Evaluation of RF Capacitance Extraction for Ultrathin Ultraleaky SOI MOS Devices. *Yu, C.*, +, *EDL Jan. 2007 45-47*

A Novel 700-V SOI LDMOS With Double-Sided Trench. *Luo, X.*, +, *EDL May 2007 422-424*

Duration of the High Breakdown Voltage Phase in Deep Depletion SOI LDMOS. *Napoli, E.*, *EDL Aug. 2007 753-755*

Embedded TFT NAND-Type Nonvolatile Memory in Panel. *Chen, H.-T.*, +, *EDL June 2007 499-501*

Study of the Erase Mechanism of MANOS (Metal/Al₂O₃/SiN/SiO₂/Si) Device. *Lai, S.*, +, *EDL July 2007 643-645*

Wide V_{fb} and V_{th} Tunability for Metal-Gated MOS Devices With HfLaO Gate Dielectrics. *Wang, X. P.*, +, *EDL April 2007 258-260*

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A Graphene Field-Effect Device. *Lemme, M. C.*, +, *EDL April 2007 282-284*
Role of Nitrogen Atoms in Reduction of Electron Charge Traps in Hf-Based High- κ Dielectrics. *Umezawa, N.*, +, *EDL May 2007 363-365*

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High Transconductance MISFET With a Single InAs Nanowire Channel. *Do, Q.-T.*, +, *EDL Aug. 2007 682-684*

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Fabrication of 0.15- μ m Γ -Shaped Gate In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As Metamorphic HEMTs Using DUV Lithography and Tilt Dry-Etching Technique. *Lien, Y.-C.*, +, *EDL Feb. 2007 93-95*

MOCVD

Charge Trapping and TDDB Characteristics of Ultrathin MOCVD HfO₂ Gate Dielectric on Nitrided Germanium. *Bai, W.*, +, *EDL May 2007 369-372*

Metamorphic Heterostructure InP/GaAsSb/InP HBTs on GaAs Substrates by MOCVD. *Zhou, W.*, +, *EDL July 2007 539-542*

Thickness Scaling and Reliability Comparison for the Inter-Poly High- κ Dielectrics. *Chen, Y.-Y.*, +, *EDL Aug. 2007 700-702*

MODFETs

50-nm T-Gate InAlAs/InGaAs Metamorphic HEMTs With Low Noise and High f_T Characteristics. *Lim, B. O.*, +, *EDL July 2007 546-548*

35-nm Zigzag T-Gate In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As Metamorphic GaAs HEMTs With an Ultrahigh f_{max} of 520 GHz. *Lee, K.-S.*, +, *EDL Aug. 2007 672-675*

A Planar Gunn Diode Operating Above 100 GHz. *Khalid, A.*, +, *EDL Oct. 2007 849-851*

Comparison of GaN HEMTs on Diamond and SiC Substrates. *Felbinger, J. G.*, +, *EDL Nov. 2007 948-950*

Power Performance of AlGaIn/GaN HEMTs Grown on SiC by Ammonia-MBE at 4 and 10 GHz. *Poblenz, C.*, +, *EDL Nov. 2007 945-947*

Remarkable Reduction of On-Resistance by Ion Implantation in GaN/AlGaIn/GaN HEMTs With Low Gate Leakage Current. *Nomoto, K.*, +, *EDL Nov. 2007 939-941*

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Source/Drain Extension Region Engineering in FinFETs for Low-Voltage Analog Applications. *Kranti, A.*, +, *EDL Feb. 2007 139-141*

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Time-Domain-Reflectometry for Capacitance-Voltage Measurement With Very High Leakage Current. *Wang, Y.*, +, *EDL Jan. 2007 51-53*

A Novel Latch-Up Protection for Bulk-Silicon Scan Driver ICs of Shadow-Mask Plasma-Display Panel. *Sun, W.*, +, *EDL Dec. 2007 1135-1137*

Ar Annealing for Suppression of Gate Oxide Thinning at Shallow Trench Isolation Edge. *Ohashi, T.*, +, *EDL July 2007 562-564*

Effect of Gate Dopant Diffusion on Leakage Current in n⁺Poly-Si/HfO₂ and Examination of Leakage Paths by Conducting Atomic Force Microscopy. *Yu, X.*, +, *EDL May 2007 373-375*

Electrical Characterization of Leaky Charge-Trapping High- κ MOS Devices Using Pulsed $Q-V$. *Martens, K.*, +, *EDL May 2007 436-439*

Error and Correction in Capacitance-Voltage Measurement Due to the Presence of Source and Drain. *Wang, Y.*, +, *EDL July 2007 640-642*

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Achieving Low- V_T Ni-FUSI CMOS by Ultra-Thin Dy₂O₃ Capping of Hafnium Silicate Dielectrics. *Veloso, A.*, +, *EDL Nov. 2007 980-983*

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Duration of the High Breakdown Voltage Phase in Deep Depletion SOI LDMOS. *Napoli, E.*, *EDL Aug. 2007 753-755*

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Improved Reliability by Reduction of Hot-Electron Damage in the Vertical Impact-Ionization MOSFET (I-MOS). *Abelein, U.*, +, *EDL Jan. 2007 65-67*

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Source/Drain Extension Region Engineering in FinFETs for Low-Voltage Analog Applications. *Kranti, A.*, +, *EDL Feb. 2007 139-141*

Body Thickness Dependence of Impact Ionization in a Multiple-Gate FinFET. *Han, J.-W.*, +, *EDL July 2007 625-627*

Demonstration of Low V_i Ni-FUSI N-MOSFETs With SiON Dielectrics by Using a Dy₂O₃ Cap Layer. *Yu, H. Y.*, +, *EDL Nov. 2007 957-959*

Demonstration of Metal-Gated Low V_i n-MOSFETs Using a Poly-Si/TaN/Dy₂O₃/SiON Gate Stack With a ScaEDL EOT Value. *Yu, H. Y.*, +, *EDL July 2007 656-658*

Low-Temperature Transport Characteristics and Quantum-Confinement Effects in Gate-All-Around Si-Nanowire N-MOSFET. *Rustagi, S. C.*, +, *EDL Oct. 2007 909-912*

On the Apparent Mobility in Nanometric n-MOSFETs. *Zilli, M.*, +, *EDL Nov. 2007 1036-1039*

On the Enhanced Impact Ionization in Uniaxial Strained p-MOSFETs. *Su, P.*, +, *EDL July 2007 649-651*

Submicrometer Inversion-Type Enhancement-Mode InGaAs MOSFET With Atomic-Layer-Deposited Al₂O₃ as Gate Dielectric. *Xuan, Y.*, +, *EDL Nov. 2007 935-938*

1- μ m Enhancement Mode GaAs N-Channel MOSFETs With Transconductance Exceeding 250 mS/mm. *Rajagopalan, K.*, +, *EDL Feb. 2007 100-102*

A Constant-Mobility Method to Enable MOSFET Series-Resistance Extraction. *Lin, D.-W.*, +, *EDL Dec. 2007 1132-1134*

A Graphene Field-Effect Device. *Lemme, M. C.*, +, *EDL April 2007 282-284*
A High-Performance Body-Tied FinFET Bandgap Engineered SONOS (BE-SONOS) for NAND-Type Flash Memory. *Hsu, T.-H.*, +, *EDL May 2007 443-445*

A Novel Approach in Separating the Roles of Electrons and Holes in Causing Degradation in Hf-Based MOSFET Devices by Using Stress-Anneal Technique. *Akbar, M. S.*, +, *EDL Feb. 2007 132-134*

Achieving Conduction Band-Edge Effective Work Functions by La₂O₃ Capping of Hafnium Silicates. *Ragnarsson, L.-A.*, +, *EDL June 2007 486-488*

Ar Annealing for Suppression of Gate Oxide Thinning at Shallow Trench Isolation Edge. *Ohashi, T.*, +, *EDL July 2007 562-564*

Arsenic Junction Thermal Stability and High-Dose Boron-Pocket Activation During SPER in nMOS Transistors. *Severi, S.*, +, *EDL March 2007 198-200*

Border-Trap Characterization in High- κ Strained-Si MOSFETs. *Maji, D.*, +, *EDL Aug. 2007 731-733*

CMOS Dual-Work-Function Engineering by Using Implanted Ni-FUSI. *Lin, C.-T.*, +, *EDL Sept. 2007 831-833*

Characteristics of Ni/Gd FUSI for NMOS Gate Electrode Applications. *Lee, B.*, +, *EDL July 2007 555-557*

Charge Trapping and TDDB Characteristics of Ultrathin MOCVD HfO₂ Gate Dielectric on Nitrided Germanium. *Bai, W.*, +, *EDL May 2007 369-372*

Cointegration of High-Performance Tied-Gate Three-Terminal FinFETs and Variable Threshold-Voltage Independent-Gate Four-Terminal FinFETs With Asymmetric Gate-Oxide Thicknesses. *Liu, Y.*, +, *EDL June 2007 517-519*

- Comparison of On-The-Fly, DC I_d-V_g , and Single-Pulse Methods for Evaluating Threshold Voltage Instability in High- κ nMOSFETs. *Heh, D.*, +, *EDL March 2007 245-247*
- Correction to "Revision of Tunneling Field-Effect Transistor in Standard CMOS Technologies". *Nirschl, Th.*, +, *EDL April 2007 315-315*
- Demonstration of Asymmetric Gate-Oxide Thickness Four-Terminal FinFETs Having Flexible Threshold Voltage and Good Subthreshold Slope. *Masahara, M.*, +, *EDL March 2007 217-219*
- Detection of Border Trap Density and Energy Distribution Along the Gate Dielectric Bulk of High- κ Gated MOS Devices. *Lu, C.-Y.*, +, *EDL May 2007 432-435*
- Direct Measurement of Top and Sidewall Interface Trap Density in SOI FinFETs. *Kapila, G.*, +, *EDL March 2007 232-234*
- Effect of F₂ Postmetallization Annealing on the Electrical and Reliability Characteristics of HfSiO Gate Dielectric. *Chang, M.*, +, *EDL Jan. 2007 21-23*
- Effective Work Function Engineering of Ta_xC_y Metal Gate on Hf-Based Dielectrics. *Yen, F. Y.*, +, *EDL March 2007 201-203*
- Effects of Measurement Temperature on NBTI. *Zhang, J. F.*, +, *EDL April 2007 298-300*
- Electrical Characterization of ZrO₂/Si Interface Properties in MOSFETs With ZrO₂ Gate Dielectrics. *Liu, C.-H.*, +, *EDL Jan. 2007 62-64*
- Electrical Characterization of Leaky Charge-Trapping High- κ MOS Devices Using Pulsed $Q-V$. *Martens, K.*, +, *EDL May 2007 436-439*
- Electrical Properties of nMOSFETs Using the NiSi:Yb FUSI Electrode. *Yu, H. Y.*, +, *EDL Feb. 2007 154-156*
- Electron Transport in Strained-Silicon Directly on Insulator Ultrathin-Body n-MOSFETs With Body Thickness Ranging From 2 to 25 nm. *Gomez, L.*, +, *EDL April 2007 285-287*
- Enhanced Strain Effects in 25-nm Gate-Length Thin-Body nMOSFETs With Silicon-Carbon Source/Drain and Tensile-Stress Liner. *Ang, K.-W.*, +, *EDL April 2007 301-304*
- Enhancement-Mode GaAs MOSFETs With an In_{0.3}Ga_{0.7}As Channel, a Mobility of Over 5000 cm²/V · s, and Transconductance of Over 475 μ S/ μ m. *Hill, R. J. W.*, +, *EDL Dec. 2007 1080-1082*
- Evaluation of RF Capacitance Extraction for Ultrathin Ultraleaky SOI MOS Devices. *Yu, C.*, +, *EDL Jan. 2007 45-47*
- Experimental Evaluation of Effects of Channel Doping on Characteristics of FinFETs. *Endo, K.*, +, *EDL Dec. 2007 1123-1125*
- Experimental and TCAD Investigation of the Two Components of the Impact Ionization MOSFET (IMOS) Switching. *Mayer, F.*, +, *EDL July 2007 619-621*
- Extraction of π -Type Substrate Resistance Based on Three-Port Measurement and the Model Verification up to 110 GHz. *Kang, I. M.*, +, *EDL May 2007 425-427*
- Extraction of the Threshold-Voltage Shift by the Single-Pulse Technique. *Heh, D.*, +, *EDL Aug. 2007 734-736*
- Flicker Noise and Its Degradation Characteristics Under Electrical Stress in MOSFETs With Thin Strained-Si/SiGe Dual-Quantum Well. *Jiang, Y.*, +, *EDL July 2007 603-605*
- Fluorine Passivation in Gate Stacks of Poly-Si/TaN/HfO₂ (and HfSiON/HfO₂)/Si Through Gate Ion Implantation. *Zhang, M. H.*, +, *EDL March 2007 195-197*
- Frequency Variation of the Small-Signal Output Conductance of Decanometer MOSFETs Due to Substrate Crosstalk. *Kilchyska, V.*, +, *EDL May 2007 419-421*
- Gate Voltage Dependence of MOSFET 1/ f Noise Statistics. *Erturk, M.*, +, *EDL Sept. 2007 812-814*
- Gate Workfunction Engineering in Bulk FinFETs for Sub-50-nm DRAM Cell Transistors. *Park, K.-H.*, +, *EDL Feb. 2007 148-150*
- HfLaON n-MOSFETs Using a Low Work Function HfSi_x Gate. *Cheng, C. F.*, +, *EDL Dec. 2007 1092-1094*
- High Mobility Strained Ge pMOSFETs With High- κ /Metal Gate. *Nicholas, G.*, +, *EDL Sept. 2007 825-827*
- High-Temperature Stable HfLaON p-MOSFETs With High-Work-Function Ir₃Si Gate. *Wu, C. H.*, +, *EDL April 2007 292-294*
- Impact of High- k Gate Dielectrics on the Device and Circuit Performance of Nanoscale FinFETs. *Manoj, C. R.*, +, *EDL April 2007 295-297*
- Impact of Parameter Variations and Random Dopant Fluctuations on Short-Channel Fully Depleted SOI MOSFETs With Extremely Thin BOX. *Ohtou, T.*, +, *EDL Aug. 2007 740-742*
- Impacts of Dopant Segregation on the Performance and Interface-State Density of the MOSFET With FUSI NiSi Gate. *Liu, J.*, +, *EDL Jan. 2007 11-13*
- Impacts of Notched-Gate Structure on Contact Etch Stop Layer (CESL) Stressed 90-nm nMOSFET. *Lin, C.-T.*, +, *EDL May 2007 376-378*
- Improved Carrier Injection in Ultrathin-Body SOI Schottky-Barrier MOSFETs. *Zhang, M.*, +, *EDL March 2007 223-225*
- Improved Ge Surface Passivation With Ultrathin SiO_x Enabling High-Mobility Surface Channel pMOSFETs Featuring a HfSiO/WN Gate Stack. *Joshi, S.*, +, *EDL April 2007 308-311*
- Investigation and Localization of the SiGe Source/Drain (S/D) Strain-Induced Defects in PMOSFET With 45-nm CMOS Technology. *Cheng, C. Y.*, +, *EDL May 2007 408-411*
- Long Retention of Gain-Cell Dynamic Random Access Memory With Undoped Memory Node. *Nishiguchi, K.*, +, *EDL Jan. 2007 48-50*
- Low-Frequency Noise Assessment of Silicon Passivated Ge pMOSFETs With TiN/TaN/ HfO₂ Gate Stack. *Guo, W.*, +, *EDL April 2007 288-291*
- Low-Frequency Noise Characteristics in Strained-Si nMOSFETs. *Wang, Y. P.*, +, *EDL Jan. 2007 36-38*
- Measurement of Channel Stress Using Gate Direct Tunneling Current in Uniaxially Stressed nMOSFETs. *Hsieh, C.-Y.*, +, *EDL Sept. 2007 818-820*
- N-channel FinFETs With 25-nm Gate Length and Schottky-Barrier Source and Drain Featuring Ytterbium Silicide. *Lee, R. T. P.*, +, *EDL Feb. 2007 164-167*
- New Insights on "Capacitorless" Floating-Body DRAM Cells. *Fossum, J. G.*, +, *EDL June 2007 513-516*
- Nitrogen Incorporation in HfSiO(N)/TaN Gate Stacks: Impact on Performances and NBTI. *Aoulaiche, M.*, +, *EDL July 2007 613-615*
- Novel Approach to Reduce Source/Drain Series and Contact Resistance in High-Performance UTSOI CMOS Devices Using Selective Electrodeless CoWP or CoB Process. *Pan, J.*, +, *EDL Aug. 2007 691-693*
- Observation of Metal-Layer Stress on Si Nanowires in Gate-All-Around High- κ /Metal-Gate Device Structures. *Singh, N.*, +, *EDL July 2007 558-561*
- On the Control of Short-Channel Effect for MOSFETs With Reverse Halo Implantation. *Zhu, H.*, +, *EDL Feb. 2007 168-170*
- P-Channel Germanium FinFET Based on Rapid Melt Growth. *Feng, J.*, +, *EDL July 2007 637-639*
- PMOSFET Reliability Study for Direct Silicon Bond (DSB) Hybrid Orientation Technology (HOT). *Huang, Y.-T.*, +, *EDL Sept. 2007 815-817*
- Parasitic Bipolar Junction Transistors in a Floating-Gate MOSFET for Fluorescence Detection. *Shin, K.-S.*, +, *EDL July 2007 581-583*
- Piezoresistance Coefficients of (100) Silicon nMOSFETs Measured at Low and High (~ 1.5 GPa) Channel Stress. *Suthram, S.*, +, *EDL Jan. 2007 58-61*
- Pinch-Off Voltage-Adjustable High-Voltage Junction Field-Effect Transistor. *Liaw, C.-W.*, +, *EDL Aug. 2007 737-739*
- Role of Nitrogen Atoms in Reduction of Electron Charge Traps in Hf-Based High- κ Dielectrics. *Umezawa, N.*, +, *EDL May 2007 363-365*
- Selectively Doped High-Power AlGaIn/InGaIn/GaN MOS-DHFET. *Adivarahan, V.*, +, *EDL March 2007 192-194*
- Short-Channel Effects in Independent-Gate FinFETs. *Lu, Z.*, +, *EDL Feb. 2007 145-147*
- Strained-Si Channel Super-Self-Aligned Back-Gate/Double-Gate Planar Transistors. *Lin, H.*, +, *EDL June 2007 506-508*
- Stress Hybridization for Multigate Devices Fabricated on Supercritical Strained-SOI (SC-SSOI). *Collaert, N.*, +, *EDL July 2007 646-648*
- Substrate Bias Effect Linked to Parasitic Series Resistance in Multiple-Gate SOI MOSFETs. *Rudenko, T.*, +, *EDL Sept. 2007 834-836*
- Temperature-Oriented Experiment and Simulation as Corroborating Evidence of MOSFET Backscattering Theory. *Chen, M.-J.*, +, *EDL Feb. 2007 177-179*
- The Effects of the Injection-Channel Velocity on the Gate Leakage Current of Nanoscale MOSFETs. *Mao, L.*, *EDL Feb. 2007 161-163*
- The Investigation of Post-Annealing-Induced Defects Behavior on 90-nm In Halo nMOSFETs With Low-Frequency Noise and Charge-Pumping Measuring. *Lai, C.-M.*, +, *EDL Feb. 2007 142-144*
- Threshold Voltage Shift Due to Mechanical Stress-Enhanced Plasma Process-Induced Damage in 0.13- μ m pMOSFET. *Li, R.*, +, *EDL May 2007 360-362*
- Valence Band Offset Measurements on Thin Silicon-on-Insulator MOSFETs. *van der Steen, J.-L. P. J.*, +, *EDL Sept. 2007 821-824*
- Vertically Stacked SiGe Nanowire Array Channel CMOS Transistors. *Fang, W. W.*, +, *EDL March 2007 211-213*
- Yttrium- and Terbium-Based Interlayer on SiO₂ and HfO₂ Gate Dielectrics for Work Function Modulation of Nickel Fully Silicided Gate in nMOSFET. *Lim, A. E.-J.*, +, *EDL June 2007 482-485*

MOSFETs

- A New Degradation Mechanism in High-Voltage SiC Power MOSFETs. Agarwal, A., +, *EDL July 2007 587-589*
- Demonstration of Low V_t Ni-FUSI N-MOSFETs With SiON Dielectrics by Using a Dy₂O₃ Cap Layer. Yu, H. Y., +, *EDL Nov. 2007 957-959*
- Improved Electrical Characteristics of Ge-on-Si Field-Effect Transistors With ControlEDL Ge Epitaxial Layer Thickness on Si Substrates. Oh, J., +, *EDL Nov. 2007 1044-1046*
- Investigation of Carrier Transport in Germanium MOSFETs With WN/Al₂O₃/AlN Gate Stacks. Ritenour, A., +, *EDL Aug. 2007 746-749*
- Mobility Modeling and Its Extraction Technique for Manufacturing Strained-Si MOSFETs. Wang, J.-S., +, *EDL Nov. 2007 1040-1043*
- On the Enhanced Impact Ionization in Uniaxial Strained p-MOSFETs. Su, P., +, *EDL July 2007 649-651*
- On the Low-Frequency Noise of pMOSFETs With Embedded SiGe Source/Drain and Fully Silicided Metal Gate. Simoen, E., +, *EDL Nov. 2007 987-989*
- On the Origin of the Excess Low-Frequency Noise in Graded-Channel Silicon-on-Insulator nMOSFETs. Simoen, E., +, *EDL Oct. 2007 919-921*
- The Origin of Electron Mobility Enhancement in Strained MOSFETs. Hadjisavvas, G., +, *EDL Nov. 2007 1018-1020*

Magnetoresistance

- On the Apparent Mobility in Nanometric n-MOSFETs. Zilli, M., +, *EDL Nov. 2007 1036-1039*

Manufacturing

- Mobility Modeling and Its Extraction Technique for Manufacturing Strained-Si MOSFETs. Wang, J.-S., +, *EDL Nov. 2007 1040-1043*

Masks

- A Novel Low-Temperature Polysilicon Thin-Film Transistors With a Self-Aligned Gate and Raised Source/Drain Formed by the Damascene Process. Chang, K. M., +, *EDL Sept. 2007 806-808*

Materials

- Nonvolatile Multilevel Conductance and Memory Effect in Molecule-Based Devices. Guo, P., +, *EDL July 2007 572-574*
- A New Nonvolatile Bistable Polymer-Nanoparticle Memory Device. Lin, H.-T., +, *EDL Nov. 2007 951-953*
- Anomalous Cells With Low Reset Resistance in Phase-Change-Memory Arrays. Mantegazza, D., +, *EDL Oct. 2007 865-867*
- Enhanced Thermal Efficiency in Phase-Change Memory Cell by Double GST Thermally Confined Structure. Chao, D.-S., +, *EDL Oct. 2007 871-873*
- Solution-Processed n-Type Organic Field-Effect Transistors With High ON/OFF Current Ratios Based on Fullerene Derivatives. Tiwari, S. P., +, *EDL Oct. 2007 880-883*

Mathematical model

- Low-Temperature Transport Characteristics and Quantum-Confinement Effects in Gate-All-Around Si-Nanowire N-MOSFET. Rustagi, S. C., +, *EDL Oct. 2007 909-912*
- On the Apparent Mobility in Nanometric n-MOSFETs. Zilli, M., +, *EDL Nov. 2007 1036-1039*

Medical image processing

- On-Pixel Voltage-ControlEDL Oscillator in Amorphous-Silicon Technology for Digital Imaging Applications. Sanaie, G., +, *EDL Jan. 2007 33-35*

Memory architecture

- A High-Performance Body-Tied FinFET Bandgap Engineered SONOS (BE-SONOS) for NAND-Type Flash Memory. Hsu, T.-H., +, *EDL May 2007 443-445*
- Vertical Flash Memory Cell With Nanocrystal Floating Gate for Ultradense Integration and Good Retention. Sarkar, J., +, *EDL May 2007 449-451*

Memory management

- A New Nonvolatile Bistable Polymer-Nanoparticle Memory Device. Lin, H.-T., +, *EDL Nov. 2007 951-953*

Mercury compounds

- HgTe Nanocrystal-Based Thin-Film Transistors Fabricated on Glass Substrates. Kim, H., +, *EDL Jan. 2007 42-44*

Metal gates

- The Effect of an Yttrium Interlayer on a Ni Germanided Metal Gate Work-function in SiO₂/HfO₂. Yu, H. P., +, *EDL Dec. 2007 1098-1101*

Metal-semiconductor-metal structures

- AlGaIn Photodetectors Prepared on Si Substrates. Chiou, Y. Z., +, *EDL April 2007 264-266*

- Amorphous-SiCBN-Based Metal-Semiconductor-Metal Photodetector for High-Temperature Applications. Vijayakumar, A., +, *EDL Aug. 2007 713-715*

Metallisation

- Submicrometer Copper T-Gate AlGaIn/GaN HFETs: The Gate Metal Stack Effect. Sun, H. F., +, *EDL May 2007 350-353*

Metals

- Nonvolatile Multilevel Conductance and Memory Effect in Molecule-Based Devices. Guo, P., +, *EDL July 2007 572-574*
- Achieving Low- V_T Ni-FUSI CMOS by Ultra-Thin Dy₂O₃ Capping of Hafnium Silicate Dielectrics. Veloso, A., +, *EDL Nov. 2007 980-983*
- Demonstration of Metal-Gated Low V_t n-MOSFETs Using a Poly-Si/TaN/Dy₂O₃/SiON Gate Stack With a ScaEDL EOT Value. Yu, H. Y., +, *EDL July 2007 656-658*
- Design of On-Chip Transformer With Various Coil Widths to Achieve Minimal Metal Resistance. Hsu, H.-M., +, *EDL Nov. 2007 1029-1032*
- Effect of Substrate Parasitic Inductance on Silicon-Based Transmission Lines and On-Chip Inductors. Huang, F., +, *EDL Nov. 2007 1025-1028*
- NMOS Compatible Work Function of TaN Metal Gate With Erbium-Oxide-Doped Hafnium Oxide Gate Dielectric. Chen, J., +, *EDL Oct. 2007 862-864*
- Reduction of Threshold Voltage by Diffusion Control Technique in p-MISFETs Using Poly-Si/TiN/HfSiON Gate Stacks. Kawahara, T., +, *EDL Oct. 2007 868-870*
- The Leakage Current of the Schottky Contact on the Mesa Edge of AlGaIn/GaN Heterostructure. Xu, C., +, *EDL Nov. 2007 942-944*

Micromachining

- CMOS-Compatible Micromachined Toroid and Solenoid Inductors With High Q -Factors. Zine-El-Abidine, I., +, *EDL March 2007 226-228*

Microprocessor chips

- Electromigration Resistant Power Delivery Systems. Sekar, D. C., +, *EDL Aug. 2007 767-769*

Microstrip circuits

- A 0.2-W Heterostructure Barrier Varactor Frequency Tripler at 113 GHz. Vukusic, J., +, *EDL May 2007 340-342*

Microswitches

- Lifetime Extension of RF MEMS Direct Contact Switches in Hot Switching Operations by Ball Grid Array Dimple Design. Chow, L. L. W., +, *EDL June 2007 479-481*

Microwave devices

- RF-Enhanced Contacts to Wide-Bandgap Devices. Simin, G., +, *EDL Jan. 2007 2-4*

Microwave field effect transistors

- RF Power Measurements of InAlN/GaN Unstrained HEMTs on SiC Substrates at 10 GHz. Jessen, G. H., +, *EDL May 2007 354-356*

Microwave measurement

- RF Power Measurements of InAlN/GaN Unstrained HEMTs on SiC Substrates at 10 GHz. Jessen, G. H., +, *EDL May 2007 354-356*

Microwave switches

- Lifetime Extension of RF MEMS Direct Contact Switches in Hot Switching Operations by Ball Grid Array Dimple Design. Chow, L. L. W., +, *EDL June 2007 479-481*

Millimetre wave antenna arrays

- 100-GHz Quasi-Yagi Antenna in Silicon Technology. Sun, M., +, *EDL May 2007 455-457*

Millimetre wave detectors

- Temperature Dependence of High Frequency and Noise Performance of Sb-Heterostructure Millimeter-Wave Detectors. Su, N., +, *EDL May 2007 336-339*

Millimetre wave devices

- Lifetime Extension of RF MEMS Direct Contact Switches in Hot Switching Operations by Ball Grid Array Dimple Design. Chow, L. L. W., +, *EDL June 2007 479-481*

Millimetre wave field effect transistors

- Extraction of π -Type Substrate Resistance Based on Three-Port Measurement and the Model Verification up to 110 GHz. Kang, I. M., +, *EDL May 2007 425-427*

Millimetre wave filters

- Millimeter-Wave Bandpass Filters by Standard 0.18- μ m CMOS Technology. Sun, S., +, *EDL March 2007 220-222*

Mixers

- Improvement of the Conversion Performance of a Resonating Multimode Microelectromechanical Mixer-Filter Through Parametric Amplification. Koskenvuo, M., +, *EDL Nov. 2007 970-972*

Modulation

Improvement of the Conversion Performance of a Resonating Multimode Microelectromechanical Mixer-Filter Through Parametric Amplification. *Koskenvuori, M.*, +, *EDL Nov. 2007 970-972*

Modulators

Robust CoupEDL-Quantum-Well Structure for Use in Electrorefraction Modulators. *Ristic, S.*, +, *EDL Jan. 2007 30-32*

Molecular beam epitaxial growth

InGaAsSb/InP Double Heterojunction Bipolar Transistors Grown by Solid-Source Molecular Beam Epitaxy. *Chen, S.-H.*, +, *EDL Aug. 2007 679-681*

Monte Carlo methods

Temperature-Oriented Experiment and Simulation as Corroborating Evidence of MOSFET Backscattering Theory. *Chen, M.-J.*, +, *EDL Feb. 2007 177-179*

Hot-Phonon Effect on the Electrothermal Behavior of Submicrometer III-V HEMTs. *Sadi, T.*, +, *EDL Sept. 2007 787-789*

Injected Current and Quantum Transmission Coefficient in Low Schottky Barriers: WKB and Airy Approaches. *Rengel, R.*, +, *EDL Feb. 2007 171-173*

On the Apparent Mobility in Nanometric n-MOSFETs. *Zilli, M.*, +, *EDL Nov. 2007 1036-1039*

Predicting Thermal Neutron-Induced Soft Errors in Static Memories Using TCAD and Physics-Based Monte Carlo Simulation Tools. *Warren, K. M.*, +, *EDL Feb. 2007 180-182*

N**NAND circuits**

A High-Performance Body-Tied FinFET Bandgap Engineered SONOS (BE-SONOS) for NAND-Type Flash Memory. *Hsu, T.-H.*, +, *EDL May 2007 443-445*

Embedded TFT NAND-Type Nonvolatile Memory in Panel. *Chen, H.-T.*, +, *EDL June 2007 499-501*

The Effect of Trapped Charge Distributions on Data Retention Characteristics of NAND Flash Memory Cells. *Park, M.*, +, *EDL Aug. 2007 750-752*

Nanoelectronics

Temperature-Oriented Experiment and Simulation as Corroborating Evidence of MOSFET Backscattering Theory. *Chen, M.-J.*, +, *EDL Feb. 2007 177-179*

A 0.26- μm^2 U-Shaped Nitride-Based Programming Cell on Pure 90-nm CMOS Technology. *Lai, H.-C.*, +, *EDL Sept. 2007 837-839*

Conductance Modeling for Graphene Nanoribbon (GNR) Interconnects. *Naeemi, A.*, +, *EDL May 2007 428-431*

Electron Transport in Strained-Silicon Directly on Insulator Ultrathin-Body n-MOSFETs With Body Thickness Ranging From 2 to 25 nm. *Gomez, L.*, +, *EDL April 2007 285-287*

Enhanced Strain Effects in 25-nm Gate-Length Thin-Body nMOSFETs With Silicon-Carbon Source/Drain and Tensile-Stress Liner. *Ang, K.-W.*, +, *EDL April 2007 301-304*

Fermi-Level Pinning in Nanocrystal Memories. *Hou, T.-H.*, +, *EDL Feb. 2007 103-106*

Impact of High- k Gate Dielectrics on the Device and Circuit Performance of Nanoscale FinFETs. *Manoj, C. R.*, +, *EDL April 2007 295-297*

N-channel FinFETs With 25-nm Gate Length and Schottky-Barrier Source and Drain Featuring Ytterbium Silicide. *Lee, R. T. P.*, +, *EDL Feb. 2007 164-167*

The Effects of the Injection-Channel Velocity on the Gate Leakage Current of Nanoscale MOSFETs. *Mao, L.*, *EDL Feb. 2007 161-163*

Nanoparticles

Electrically Bistable Thin-Film Device Based on PVK and GNPs Polymer Material. *Song, Y.*, +, *EDL Feb. 2007 107-110*

A New Nonvolatile Bistable Polymer-Nanoparticle Memory Device. *Lin, H.-T.*, +, *EDL Nov. 2007 951-953*

Nanostructured materials

HgTe Nanocrystal-Based Thin-Film Transistors Fabricated on Glass Substrates. *Kim, H.*, +, *EDL Jan. 2007 42-44*

Fabrication of Ni Nanocrystal Flash Memories Using a Polymeric Self-Assembly Approach. *Shahrjerdi, D.*, +, *EDL Sept. 2007 793-796*

Fermi-Level Pinning in Nanocrystal Memories. *Hou, T.-H.*, +, *EDL Feb. 2007 103-106*

Giant Random Telegraph Signals in Nanoscale Floating-Gate Devices. *Fantini, P.*, +, *EDL Dec. 2007 1114-1116*

High- κ Al₂O₃-HfTiO Nanolaminates With Less Than 0.8-nm Equivalent Oxide Thickness. *Mikheleshvili, V.*, +, *EDL Jan. 2007 24-26*

Temperature-Dependent Characteristics of Cylindrical Gate-All-Around Twin Silicon Nanowire MOSFETs (TSNWFETs). *Cho, K. H.*, +, *EDL Dec. 2007 1129-1131*

The Preparation of Nanocrystalline Silicon by Plasma-Enhanced Hydrogenation for the Fabrication of Light-Emitting Diodes. *Jamei, M.*, +, *EDL March 2007 207-210*

Nanotechnology

Fabrication of Ni Nanocrystal Flash Memories Using a Polymeric Self-Assembly Approach. *Shahrjerdi, D.*, +, *EDL Sept. 2007 793-796*

Nanotube devices

An Efficient Macromodeling Approach for Simulating Carbon-Nanotube Field-Emission Triode Devices in Display Applications. *Guo, X.*, +, *EDL Aug. 2007 710-712*

Nanowires

Vertically Stacked SiGe Nanowire Array Channel CMOS Transistors. *Fang, W. W.*, +, *EDL March 2007 211-213*

A Novel Nanowire Channel Poly-Si TFT Functioning as Transistor and Non-volatile SONOS Memory. *Chen, S.-C.*, +, *EDL Sept. 2007 809-811*

Conductance Modeling for Graphene Nanoribbon (GNR) Interconnects. *Naeemi, A.*, +, *EDL May 2007 428-431*

High Transconductance MISFET With a Single InAs Nanowire Channel. *Do, Q.-T.*, +, *EDL Aug. 2007 682-684*

Observation of Metal-Layer Stress on Si Nanowires in Gate-All-Around High- κ /Metal-Gate Device Structures. *Singh, N.*, +, *EDL July 2007 558-561*

Neutron effects

Predicting Thermal Neutron-Induced Soft Errors in Static Memories Using TCAD and Physics-Based Monte Carlo Simulation Tools. *Warren, K. M.*, +, *EDL Feb. 2007 180-182*

Nickel

High-Temperature Leakage Improvement in Metal-Insulator-Metal Capacitors by Work-Function Tuning. *Chiang, K. C.*, +, *EDL March 2007 235-237*

Nickel alloys

Impacts of Dopant Segregation on the Performance and Interface-State Density of the MOSFET With FUSI NiSi Gate. *Liu, J.*, +, *EDL Jan. 2007 11-13*

Nickel compounds

A Novel Strain Method for Enhancement of 90-nm Node and Beyond FUSI-Gated CMOS Performance. *Lin, C.-T.*, +, *EDL Feb. 2007 111-113*

Electrical Properties of nMOSFETs Using the NiSi:Yb FUSI Electrode. *Yu, H. Y.*, +, *EDL Feb. 2007 154-156*

Improved Carrier Injection in Ultrathin-Body SOI Schottky-Barrier MOSFETs. *Zhang, M.*, +, *EDL March 2007 223-225*

Schottky-Barrier Height Tuning by Means of Ion Implantation Into Preformed Silicide Films Followed by Drive-In Anneal. *Zhang, Z.*, +, *EDL July 2007 565-568*

Sub-0.1-eV Effective Schottky-Barrier Height for NiSi on n-Type Si (100) Using Antimony Segregation. *Wong, H.-S.*, +, *EDL Aug. 2007 703-705*

Yttrium- and Terbium-Based Interlayer on SiO₂ and HfO₂ Gate Dielectrics for Work Function Modulation of Nickel Fully Silicided Gate in nMOSFET. *Lim, A. E.-J.*, +, *EDL June 2007 482-485*

Achieving Low- V_T Ni-FUSI CMOS by Ultra-Thin Dy₂O₃ Capping of Hafnium Silicate Dielectrics. *Veloso, A.*, +, *EDL Nov. 2007 980-983*

CMOS Dual-Work-Function Engineering by Using Implanted Ni-FUSI. *Lin, C.-T.*, +, *EDL Sept. 2007 831-833*

Characteristics of Ni/Gd FUSI for NMOS Gate Electrode Applications. *Lee, B.*, +, *EDL July 2007 555-557*

Demonstration of Low V_t Ni-FUSI N-MOSFETs With SiON Dielectrics by Using a Dy₂O₃ Cap Layer. *Yu, H. Y.*, +, *EDL Nov. 2007 957-959*

Fabrication of Ni Nanocrystal Flash Memories Using a Polymeric Self-Assembly Approach. *Shahrjerdi, D.*, +, *EDL Sept. 2007 793-796*

Improved Electrical Characteristics and Reliability of MILC Poly-Si TFTs Using Fluorine-Ion Implantation. *Chang, C.-P.*, +, *EDL Nov. 2007 990-992*

Improving the Electrical Properties of NILC Poly-Si Films Using a Gettering Substrate. *Hu, C.-M.*, +, *EDL Nov. 2007 1000-1003*

The Effect of an Yttrium Interlayer on a Ni Germanided Metal Gate Work-function in SiO₂/HfO₂. *Yu, H. P.*, +, *EDL Dec. 2007 1098-1101*

Use of a High-Work-Function Ni Electrode to Improve the Stress Reliability of Analog SrTiO₃ Metal-Insulator-Metal Capacitors. *Chiang, K. C.*, +, *EDL Aug. 2007 694-696*

Nitridation

Effective Work Function Engineering of Ta_xC_y Metal Gate on Hf-Based Dielectrics. *Yen, F. Y.*, +, *EDL March 2007 201-203*

Achieving Conduction Band-Edge Effective Work Functions by La_2O_3 Capping of Hafnium Silicates. *Ragnarsson, L.-A.*, +, *EDL June 2007 486-488*
 Ar Annealing for Suppression of Gate Oxide Thinning at Shallow Trench Isolation Edge. *Ohashi, T.*, +, *EDL July 2007 562-564*

Nitrogen Incorporation in $\text{HfSiO}(\text{N})/\text{TaN}$ Gate Stacks: Impact on Performances and NBTI. *Aoulaiche, M.*, +, *EDL July 2007 613-615*

Nitrogen

Nitrogen Incorporation in $\text{HfSiO}(\text{N})/\text{TaN}$ Gate Stacks: Impact on Performances and NBTI. *Aoulaiche, M.*, +, *EDL July 2007 613-615*

Ar Annealing for Suppression of Gate Oxide Thinning at Shallow Trench Isolation Edge. *Ohashi, T.*, +, *EDL July 2007 562-564*

Noise measurement

50-nm T-Gate $\text{InAlAs}/\text{InGaAs}$ Metamorphic HEMTs With Low Noise and High f_T Characteristics. *Lim, B. O.*, +, *EDL July 2007 546-548*

A Phase Change Memory Compact Model for Multilevel Applications. *Ventrice, D.*, +, *EDL Nov. 2007 973-975*

A Wide Dynamic-Range CMOS Image Sensor Using Self-Reset Technique. *Park, D.*, +, *EDL Oct. 2007 890-892*

Giant Random Telegraph Signals in Nanoscale Floating-Gate Devices. *Fantini, P.*, +, *EDL Dec. 2007 1114-1116*

On the Low-Frequency Noise of pMOSFETs With Embedded SiGe Source/Drain and Fully Silicided Metal Gate. *Simoen, E.*, +, *EDL Nov. 2007 987-989*

On the Origin of the Excess Low-Frequency Noise in Graded-Channel Silicon-on-Insulator nMOSFETs. *Simoen, E.*, +, *EDL Oct. 2007 919-921*

Nondestructive testing

Duration of the High Breakdown Voltage Phase in Deep Depletion SOI LDMOS. *Napoli, E.*, *EDL Aug. 2007 753-755*

Nonvolatile memory

Nonvolatile Multilevel Conductance and Memory Effect in Molecule-Based Devices. *Guo, P.*, +, *EDL July 2007 572-574*

A New Nonvolatile Bistable Polymer-Nanoparticle Memory Device. *Lin, H.-T.*, +, *EDL Nov. 2007 951-953*

A Novel Single Polysilicon EEPROM Cell With a Polyfinger Capacitor. *Na, K.-Y.*, +, *EDL Nov. 2007 1047-1049*

A Program-Erasable High- κ $\text{Hf}_{0.3}\text{N}_{0.2}\text{O}_{0.5}$ MIS Capacitor With Good Retention. *Yang, H. J.*, +, *EDL Oct. 2007 913-915*

Numerical models

On the Apparent Mobility in Nanometric n-MOSFETs. *Zilli, M.*, +, *EDL Nov. 2007 1036-1039*

O

OFETs

Solution-Processed n-Type Organic Field-Effect Transistors With High ON/OFF Current Ratios Based on Fullerene Derivatives. *Tiwari, S. P.*, +, *EDL Oct. 2007 880-883*

Ohmic contacts

RF-Enhanced Contacts to Wide-Bandgap Devices. *Simin, G.*, +, *EDL Jan. 2007 2-4*

SAW Filters Composed of Interdigital Schottky and Ohmic Contacts on $\text{AlGaIn}/\text{GaIn}$ Heterostructures. *Shigekawa, N.*, +, *EDL Feb. 2007 90-92*

Optical device fabrication

GaN-Based High- Q Vertical-Cavity Light-Emitting Diodes. *Lu, T.-C.*, +, *EDL Oct. 2007 884-886*

Optical microscopes

Direct Monitoring of RF Overstress in High-Power Transistors and Amplifiers. *Stoppel, A.*, +, *EDL May 2007 357-359*

Optical reflection

GaN-Based High- Q Vertical-Cavity Light-Emitting Diodes. *Lu, T.-C.*, +, *EDL Oct. 2007 884-886*

Optimization

Young's Modulus Measurements in Standard IC CMOS Processes Using MEMS Test Structures. *Marshall, J. C.*, +, *EDL Nov. 2007 960-963*

Organic compounds

Performance Improvement of Organic Thin-Film Transistors by Electrode/Pentacene Interface Treatment Using a Hydrogen Plasma. *Lee, J.-W.*, +, *EDL May 2007 379-382*

Fabrication of Ni Nanocrystal Flash Memories Using a Polymeric Self-Assembly Approach. *Shahrjerdi, D.*, +, *EDL Sept. 2007 793-796*

Organic light emitting diodes

A Novel LTPS-TFT Pixel Circuit Compensating for TFT Threshold-Voltage Shift and OEDL Degradation for AMOEDL. *Lin, C.-L.*, +, *EDL Feb. 2007 129-131*

A Simple and Effective Approach to Improve the Output Linearity of Switched-Current AMOEDL Pixel Circuitry. *Guo, X.*, +, *EDL Oct. 2007 887-889*

Organic semiconductors

Admittance Measurements on OFET Channel and Its Modeling With $R-C$ Network. *Jung, K.-D.*, +, *EDL March 2007 204-206*

Organic thin film transistors

Constant Bias Stress Effects on Threshold Voltage of Pentacene Thin-Film Transistors Employing Polyvinylphenol Gate Dielectric. *Kim, T. H.*, +, *EDL Oct. 2007 874-876*

Solution-Processed TIPS-Pentacene Organic Thin-Film-Transistor Circuits. *Park, S. K.*, +, *EDL Oct. 2007 877-879*

Oscillators

High-Temperature Operation of $\text{AlGaIn}/\text{GaIn}$ HEMTs Direct-Coupled FET Logic (DCFL) Integrated Circuits. *Cai, Y.*, +, *EDL May 2007 328-331*
 A Planar Gunn Diode Operating Above 100 GHz. *Khalid, A.*, +, *EDL Oct. 2007 849-851*

Improvement of the Conversion Performance of a Resonating Multimode Microelectromechanical Mixer-Filter Through Parametric Amplification. *Koskenvuori, M.*, +, *EDL Nov. 2007 970-972*

Solution-Processed TIPS-Pentacene Organic Thin-Film-Transistor Circuits. *Park, S. K.*, +, *EDL Oct. 2007 877-879*

Oxidation

Vertically Stacked SiGe Nanowire Array Channel CMOS Transistors. *Fang, W. W.*, +, *EDL March 2007 211-213*

1200-V $5.2\text{-m}\Omega \cdot \text{cm}^2$ 4H-SiC BJTs With a High Common-Emitter Current Gain. *Lee, H.-S.*, +, *EDL Nov. 2007 1007-1009*

Ar Annealing for Suppression of Gate Oxide Thinning at Shallow Trench Isolation Edge. *Ohashi, T.*, +, *EDL July 2007 562-564*

Low-Frequency Noise Assessment of Silicon Passivated Ge pMOSFETs With $\text{TiN}/\text{TaN}/\text{HfO}_2$ Gate Stack. *Guo, W.*, +, *EDL April 2007 288-291*

P

P-i-n photodiodes

High-Speed InGaP/GaAs p-i-n Photodiodes With Wide Spectral Range. *Wu, M.-C.*, +, *EDL Sept. 2007 797-799*

P-n junctions

Schottky-Barrier Height Lowering by an Increase of the Substrate Doping in PtSi Schottky Barrier Source/Drain FETs. *Lousberg, G. P.*, +, *EDL Feb. 2007 123-125*

A Quantum-Mechanical View on the Capacitance of a Silicon p-n Junction. *Hurkx, G. A. M.*, +, *EDL April 2007 312-314*

Effects of Oxide-Fixed Charge on the Breakdown Voltage of Superjunction Devices. *Balaji, S.*, +, *EDL March 2007 229-231*

Passivation

A High Schottky-Barrier of 1.1 eV Between Al and S-Passivated p-Type Si(100) Surface. *Song, G.*, +, *EDL Jan. 2007 71-73*

1200-V $5.2\text{-m}\Omega \cdot \text{cm}^2$ 4H-SiC BJTs With a High Common-Emitter Current Gain. *Lee, H.-S.*, +, *EDL Nov. 2007 1007-1009*

Effects of Sulfur Passivation on Germanium MOS Capacitors With HfON Gate Dielectric. *Xie, R.*, +, *EDL Nov. 2007 976-979*

Fluorine Passivation in Gate Stacks of Poly-Si/ TaN/HfO_2 (and $\text{HfSiON}/\text{HfO}_2$)/Si Through Gate Ion Implantation. *Zhang, M. H.*, +, *EDL March 2007 195-197*

Impact of Channel Dangling Bonds on Reliability Characteristics of Flash Memory on Poly-Si Thin Films. *Lin, Y.-H.*, +, *EDL April 2007 267-269*

Improved Ge Surface Passivation With Ultrathin SiO_x Enabling High-Mobility Surface Channel pMOSFETs Featuring a HfSiO/WN Gate Stack. *Joshi, S.*, +, *EDL April 2007 308-311*

Improving the Performance of SiGe Metal-Semiconductor-Metal Photodetectors by Using an Amorphous Silicon Passivation Layer. *Chen, Y. H.*, +, *EDL Dec. 2007 1111-1113*

Low-Frequency Noise Assessment of Silicon Passivated Ge pMOSFETs With $\text{TiN}/\text{TaN}/\text{HfO}_2$ Gate Stack. *Guo, W.*, +, *EDL April 2007 288-291*

Passivation Effects of Aluminum on Polycrystalline Silicon Thin-Film Transistor With Metal-Replaced Junctions. *Zhang, D.*, +, *EDL Feb. 2007 126-128*

Pentacene

Constant Bias Stress Effects on Threshold Voltage of Pentacene Thin-Film Transistors Employing Polyvinylphenol Gate Dielectric. *Kim, T. H.*, +, *EDL Oct. 2007 874-876*

Solution-Processed TIPS-Pentacene Organic Thin-Film-Transistor Circuits. *Park, S. K.*, +, *EDL Oct. 2007 877-879*

Percolation

Limits of Performance Gain of Aligned CNT Over Randomized Network: Theoretical Predictions and Experimental Validation. *Pimparkar, N.*, +, *EDL July 2007 593-595*

Performance evaluation

Strained n-Channel Transistors With Silicon Source and Drain Regions and Embedded Silicon/Germanium as Strain-Transfer Structure. *Ang, K.-W.*, +, *EDL July 2007 609-612*

High-Performance Self-Aligned Bottom-Gate Low-Temperature Poly-Silicon Thin-Film Transistors With Excimer Laser Crystallization. *Tsai, C.-C.*, +, *EDL July 2007 599-602*

High-Performance Short-Channel Double-Gate Low-Temperature Polysilicon Thin-Film Transistors Using Excimer Laser Crystallization. *Tsai, C.-C.*, +, *EDL Nov. 2007 1010-1013*

Improved Electrical Characteristics and Reliability of MILC Poly-Si TFTs Using Fluorine-Ion Implantation. *Chang, C.-P.*, +, *EDL Nov. 2007 990-992*

Investigation of Impact Ionization in InAs-Channel HEMT for High-Speed and Low-Power Applications. *Chang, C. Y.*, +, *EDL Oct. 2007 856-858*

Power Performance of AlGaIn/GaN HEMTs Grown on SiC by Ammonia-MBE at 4 and 10 GHz. *Poblenz, C.*, +, *EDL Nov. 2007 945-947*

Strained p-Channel FinFETs With Extended II-Shaped Silicon-Germanium Source and Drain Stressors. *Tan, K.-M.*, +, *EDL Oct. 2007 905-908*

Permittivity

High- κ Al₂O₃-HfTiO Nanolaminates With Less Than 0.8-nm Equivalent Oxide Thickness. *Mikheleshvili, V.*, +, *EDL Jan. 2007 24-26*

Impact of High- κ Gate Dielectrics on the Device and Circuit Performance of Nanoscale FinFETs. *Manoj, C. R.*, +, *EDL April 2007 295-297*

Thickness Scaling and Reliability Comparison for the Inter-Poly High- κ Dielectrics. *Chen, Y.-Y.*, +, *EDL Aug. 2007 700-702*

Phase change materials

Analysis of Temperature in Phase Change Memory Scaling. *Kim, S.*, +, *EDL Aug. 2007 697-699*

A New Nonvolatile Bistable Polymer-Nanoparticle Memory Device. *Lin, H.-T.*, +, *EDL Nov. 2007 951-953*

A Phase Change Memory Compact Model for Multilevel Applications. *Ventrice, D.*, +, *EDL Nov. 2007 973-975*

Anomalous Cells With Low Reset Resistance in Phase-Change-Memory Arrays. *Mantegazza, D.*, +, *EDL Oct. 2007 865-867*

Enhanced Thermal Efficiency in Phase-Change Memory Cell by Double GST Thermally Confined Structure. *Chao, D.-S.*, +, *EDL Oct. 2007 871-873*

Phase change memory

A Phase Change Memory Compact Model for Multilevel Applications. *Ventrice, D.*, +, *EDL Nov. 2007 973-975*

Phase transformations

A Novel Strain Method for Enhancement of 90-nm Node and Beyond FUSI-Gated CMOS Performance. *Lin, C.-T.*, +, *EDL Feb. 2007 111-113*

Phonons

Hot-Phonon Effect on the Electrothermal Behavior of Submicrometer III-V HEMTs. *Sadi, T.*, +, *EDL Sept. 2007 787-789*

Phosphorus

Schottky-Barrier Height Tuning by Means of Ion Implantation Into Preformed Silicide Films Followed by Drive-In Anneal. *Zhang, Z.*, +, *EDL July 2007 565-568*

Photodetectors

Three-Dimensional Photodetectors in 3-D Silicon-On-Insulator Technology. *Culurciello, E.*, +, *EDL Feb. 2007 117-119*

AlGaIn Photodetectors Prepared on Si Substrates. *Chiou, Y. Z.*, +, *EDL April 2007 264-266*

Amorphous-SiC_{BN}-Based Metal-Semiconductor-Metal Photodetector for High-Temperature Applications. *Vijayakumar, A.*, +, *EDL Aug. 2007 713-715*

High-Responsivity Photodetector in Standard SiGe BiCMOS Technology. *Lai, K.-S.*, +, *EDL Sept. 2007 800-802*

Impact of Local Strain From Selective Epitaxial Germanium With Thin Si/SiGe Buffer on High-Performance p-i-n Photodetectors With a Low Thermal Budget. *Loh, W. Y.*, +, *EDL Nov. 2007 984-986*

Improving the Performance of SiGe Metal-Semiconductor-Metal Photodetectors by Using an Amorphous Silicon Passivation Layer. *Chen, Y. H.*, +, *EDL Dec. 2007 1111-1113*

Parasitic Bipolar Junction Transistors in a Floating-Gate MOSFET for Fluorescence Detection. *Shin, K.-S.*, +, *EDL July 2007 581-583*

Photodiodes

Three-Dimensional Photodetectors in 3-D Silicon-On-Insulator Technology. *Culurciello, E.*, +, *EDL Feb. 2007 117-119*

Active Pixel Concept Combined With Organic Photodiode for Imaging Devices. *Tedde, S.*, +, *EDL Oct. 2007 893-895*

Application of Plasma-Doping (PLAD) Technique to Reduce Dark Current of CMOS Image Sensors. *Moon, C.-R.*, +, *EDL Feb. 2007 114-116*

Parasitic Bipolar Junction Transistors in a Floating-Gate MOSFET for Fluorescence Detection. *Shin, K.-S.*, +, *EDL July 2007 581-583*

Photoemission

Amorphous-SiC_{BN}-Based Metal-Semiconductor-Metal Photodetector for High-Temperature Applications. *Vijayakumar, A.*, +, *EDL Aug. 2007 713-715*

Photovoltaic cells

A Novel Silicon Photovoltaic Cell Using a Low-Temperature Quasi-Epitaxial Silicon Emitter. *Farrokh-Baroughi, M.*, +, *EDL July 2007 575-577*

Impact of Preferential P-Diffusion Along the Grain Boundaries on Fine-Grained Polysilicon Solar Cells. *Carnel, L.*, +, *EDL Oct. 2007 899-901*

Piezoresistance

Piezoresistance Coefficients of (100) Silicon nMOSFETs Measured at Low and High (~1.5 GPa) Channel Stress. *Suthram, S.*, +, *EDL Jan. 2007 58-61*

Mobility Modeling and Its Extraction Technique for Manufacturing Strained-Si MOSFETs. *Wang, J.-S.*, +, *EDL Nov. 2007 1040-1043*

Planarisation

1.3- μ m GaInAsN Vertical-Cavity Surface-Emitting Lasers by Oxide-Planarization and Surface-Relief Processes for Single-Mode Operation. *Lee, F.-M.*, +, *EDL Feb. 2007 120-122*

Plasma CVD

A Novel Silicon Photovoltaic Cell Using a Low-Temperature Quasi-Epitaxial Silicon Emitter. *Farrokh-Baroughi, M.*, +, *EDL July 2007 575-577*

Plasma CVD coatings

Stability of Amorphous-Silicon and Nanocrystalline Silicon Thin-Film Transistors Under DC and AC Stress. *Hatzopoulos, A. T.*, +, *EDL Sept. 2007 803-805*

Plasma applications

Application of Plasma-Doping (PLAD) Technique to Reduce Dark Current of CMOS Image Sensors. *Moon, C.-R.*, +, *EDL Feb. 2007 114-116*

Threshold Voltage Shift Due to Mechanical Stress-Enhanced Plasma Process-Induced Damage in 0.13- μ m pMOSFET. *Li, R.*, +, *EDL May 2007 360-362*

Plasma deposition

The Preparation of Nanocrystalline Silicon by Plasma-Enhanced Hydrogenation for the Fabrication of Light-Emitting Diodes. *Jamei, M.*, +, *EDL March 2007 207-210*

Plasma displays

A Novel Latch-Up Protection for Bulk-Silicon Scan Driver ICs of Shadow-Mask Plasma-Display Panel. *Sun, W.*, +, *EDL Dec. 2007 1135-1137*

Plasma materials processing

Nitrogen Incorporation in HfSiO(N)/TaN Gate Stacks: Impact on Performances and NBTI. *Aoulaiche, M.*, +, *EDL July 2007 613-615*

Impact of CF₄ Plasma Treatment on GaN. *Chu, R.*, +, *EDL Sept. 2007 781-783*

Plasma temperature

Effect of SiN_x Gate Dielectric Deposition Power and Temperature on a-Si:H TFT Stability. *Kattamis, A. Z.*, +, *EDL July 2007 606-608*

Low-Temperature Passivation of Amorphous-Silicon Thin-Film Transistors With Supercritical Fluids. *Tsai, C.-T.*, +, *EDL July 2007 584-586*

Plasmas

A Simple Spacer Technique to Fabricate Poly-Si TFTs With 50-nm Nanowire Channels. *Chang, C.-W.*, +, *EDL Nov. 2007 993-995*

Plastics

Amorphous-Silicon Thin-Film Transistors Fabricated at 300 °C on a Free-Standing Foil Substrate of Clear Plastic. *Cherenack, K. H.*, +, *EDL Nov. 2007 1004-1006*

Platinum

Effect of Top Electrode Material on Resistive Switching Properties of ZrO₂ Film Memory Devices. *Lin, C.-Y.*, +, *EDL May 2007 366-368*

Platinum alloys

Effect of Gate Sinking on the Device Performance of the InGaP/AlGaAs/InGaAs Enhancement-Mode PHEMT. *Chu, L. H., +, EDL Feb. 2007 82-85*

Platinum compounds

Schottky-Barrier Height Tuning by Means of Ion Implantation Into Preformed Silicide Films Followed by Drive-In Anneal. *Zhang, Z., +, EDL July 2007 565-568*

Poisson equation

A Quantum-Mechanical View on the Capacitance of a Silicon p-n Junction. *Hurkx, G. A. M., +, EDL April 2007 312-314*

Polymer blends

Fabrication of Ni Nanocrystal Flash Memories Using a Polymeric Self-Assembly Approach. *Shahrjerdi, D., +, EDL Sept. 2007 793-796*

Polymer films

A Novel Low-Temperature Polysilicon Thin-Film Transistors With a Self-Aligned Gate and Raised Source/Drain Formed by the Damascene Process. *Chang, K. M., +, EDL Sept. 2007 806-808*

Polymers

Electrically Bistable Thin-Film Device Based on PVK and GNPs Polymer Material. *Song, Y., +, EDL Feb. 2007 107-110*

A New Nonvolatile Bistable Polymer-Nanoparticle Memory Device. *Lin, H.-T., +, EDL Nov. 2007 951-953*

Porous materials

Fabrication of Ni Nanocrystal Flash Memories Using a Polymeric Self-Assembly Approach. *Shahrjerdi, D., +, EDL Sept. 2007 793-796*

Positive ions

Resistive Switching Mechanism in $Zn_xCd_{1-x}S$ Nonvolatile Memory Devices. *Wang, Z., +, EDL Jan. 2007 14-16*

Power HEMT

Power Stability of AlGaIn/GaN HFETs at 20 W/mm in the Pinched-Off Operation Mode. *Koudymov, A., +, EDL Jan. 2007 5-7*

ON-Resistance Modulation of High Voltage GAN HEMT on Sapphire Substrate Under High Applied Voltage. *Saito, W., +, EDL Aug. 2007 676-678*

Silicon Dioxide-Encapsulated High-Voltage AlGaIn/GaN HFETs for Power-Switching Applications. *Tipirneni, N., +, EDL Sept. 2007 784-786*

Power MOSFET

A Dynamical Power-Management Demonstration Using Four-Terminal Separated-Gate FinFETs. *Endo, K., +, EDL May 2007 452-454*

On-Resistance Degradations for Different Stress Conditions in High-Voltage pEDL MOS Transistor With Thick Gate Oxide. *Sun, W., +, EDL July 2007 631-633*

Power amplifiers

Direct Monitoring of RF Overstress in High-Power Transistors and Amplifiers. *Stopel, A., +, EDL May 2007 357-359*

Power bipolar transistors

High-Voltage Self-Aligned p-Channel DMOS-IGBTs in 4H-SiC. *Sui, Y., +, EDL Aug. 2007 728-730*

Power control

A Dynamical Power-Management Demonstration Using Four-Terminal Separated-Gate FinFETs. *Endo, K., +, EDL May 2007 452-454*

Power factor correction

Pinch-Off Voltage-Adjustable High-Voltage Junction Field-Effect Transistor. *Liaw, C.-W., +, EDL Aug. 2007 737-739*

Power field effect transistors

High-Voltage Self-Aligned p-Channel DMOS-IGBTs in 4H-SiC. *Sui, Y., +, EDL Aug. 2007 728-730*

Power integrated circuits

A 20-V CMOS-Based Monolithic Bidirectional Power Switch. *Fu, Y., +, EDL Feb. 2007 174-176*

1000-V $9.1\text{-m}\Omega \cdot \text{cm}^2$ Normally Off 4H-SiC Lateral RESURF JFET for Power Integrated Circuit Applications. *Zhang, Y., +, EDL May 2007 404-407*

Power measurement

RF Power Measurements of InAlN/GaN Unstrained HEMTs on SiC Substrates at 10 GHz. *Jessen, G. H., +, EDL May 2007 354-356*

Power semiconductor devices

A New Lateral-IGBT Structure With a Wider Safe Operating Area. *Bake-root, B., +, EDL May 2007 416-418*

Power semiconductor switches

A 20-V CMOS-Based Monolithic Bidirectional Power Switch. *Fu, Y., +, EDL Feb. 2007 174-176*

Duration of the High Breakdown Voltage Phase in Deep Depletion SOI LDMOS. *Napoli, E., EDL Aug. 2007 753-755*

High-Voltage Self-Aligned p-Channel DMOS-IGBTs in 4H-SiC. *Sui, Y., +, EDL Aug. 2007 728-730*

Silicon Dioxide-Encapsulated High-Voltage AlGaIn/GaN HFETs for Power-Switching Applications. *Tipirneni, N., +, EDL Sept. 2007 784-786*

Power supply circuits

Electromigration Resistant Power Delivery Systems. *Sekar, D. C., +, EDL Aug. 2007 767-769*

Power transistors

Direct Monitoring of RF Overstress in High-Power Transistors and Amplifiers. *Stopel, A., +, EDL May 2007 357-359*

Power transmission lines

Effect of Substrate Parasitic Inductance on Silicon-Based Transmission Lines and On-Chip Inductors. *Huang, F., +, EDL Nov. 2007 1025-1028*

Programmable logic devices

A $0.26\text{-}\mu\text{m}^2$ U-Shaped Nitride-Based Programming Cell on Pure 90-nm CMOS Technology. *Lai, H.-C., +, EDL Sept. 2007 837-839*

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Enhanced Thermal Efficiency in Phase-Change Memory Cell by Double GST Thermally Confined Structure. *Chao, D.-S., +, EDL Oct. 2007 871-873*

A Phase Change Memory Compact Model for Multilevel Applications. *Ventrice, D., +, EDL Nov. 2007 973-975*

Anomalous Cells With Low Reset Resistance in Phase-Change-Memory Arrays. *Mantegazza, D., +, EDL Oct. 2007 865-867*

Metal-Oxide-High- κ Dielectric-Oxide-Semiconductor (MOHOS) Capacitors and Field-Effect Transistors for Memory Applications. *Hsu, H., +, EDL Nov. 2007 964-966*

Q**Q-factor**

CMOS-Compatible Micromachined Toroid and Solenoid Inductors With High Q-Factors. *Zine-El-Abidine, I., +, EDL March 2007 226-228*

High-Q Integrated Inductor Using Post-CMOS Selectively Grown Porous Silicon (SGPS) Technique for RFIC Applications. *Li, C., +, EDL Aug. 2007 763-766*

Quantum Hall effect

A Quantum-Mechanical View on the Capacitance of a Silicon p-n Junction. *Hurkx, G. A. M., +, EDL April 2007 312-314*

Quantum cascade lasers

A Planar Gunn Diode Operating Above 100 GHz. *Khalid, A., +, EDL Oct. 2007 849-851*

Quantum well devices

1.3- μm GaInAsN Vertical-Cavity Surface-Emitting Lasers by Oxide-Planarized and Surface-Relief Processes for Single-Mode Operation. *Lee, F.-M., +, EDL Feb. 2007 120-122*

Flicker Noise and Its Degradation Characteristics Under Electrical Stress in MOSFETs With Thin Strained-Si/SiGe Dual-Quantum Well. *Jiang, Y., +, EDL July 2007 603-605*

Ultrahigh-Speed 0.5 V Supply Voltage $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ Quantum-Well Transistors on Silicon Substrate. *Datta, S., +, EDL Aug. 2007 685-687*

Quantum wells

Robust CoupEDL-Quantum-Well Structure for Use in Electrorefraction Modulators. *Ristic, S., +, EDL Jan. 2007 30-32*

R**Radiation hardening (electronics)**

Short-Channel Effects in Independent-Gate FinFETs. *Lu, Z., +, EDL Feb. 2007 145-147*

Radiofrequency integrated circuits

Bond Pad Design With Low Capacitance in CMOS Technology for RF Applications. *Hsiao, Y.-W., +, EDL Jan. 2007 68-70*

Ferrite-Integrated On-Chip Inductors for RF ICs. *Yang, C., +, EDL July 2007 652-655*

Raman spectroscopy

Time-Resolved Temperature Measurement of AlGaIn/GaN Electronic Devices Using Micro-Raman Spectroscopy. *Kuball, M., +, EDL Feb. 2007 86-89*

Random access memory

- A Program-Erasable High- κ $\text{Hf}_{0.3}\text{N}_{0.2}\text{O}_{0.5}$ MIS Capacitor With Good Retention. *Yang, H. J.*, +, *EDL Oct. 2007 913-915*
- n^+/p^+ Gate Bulk FinFETs With Locally Separated Channel Structure for Sub-50-nm DRAM Cell Transistors. *Jung, H.-A.-R.*, +, *EDL Dec. 2007 1126-1128*
- Good High-Temperature Stability of TiN/ Al_2O_3 /WN/TiN Capacitors. *Pan, T.-M.*, +, *EDL Nov. 2007 954-956*

Random-access storage

- Resistive Switching Mechanism in $\text{Zn}_x\text{Cd}_{1-x}\text{S}$ Nonvolatile Memory Devices. *Wang, Z.*, +, *EDL Jan. 2007 14-16*
- A Novel Dual-Polarity Nonvolatile Memory. *Lin, H.*, +, *EDL May 2007 412-415*
- A Novel Nanowire Channel Poly-Si TFT Functioning as Transistor and Nonvolatile SONOS Memory. *Chen, S.-C.*, +, *EDL Sept. 2007 809-811*
- Analysis of Temperature in Phase Change Memory Scaling. *Kim, S.*, +, *EDL Aug. 2007 697-699*
- Effect of Top Electrode Material on Resistive Switching Properties of ZrO_2 Film Memory Devices. *Lin, C.-Y.*, +, *EDL May 2007 366-368*
- Electrically Bistable Thin-Film Device Based on PVK and GNPs Polymer Material. *Song, Y.*, +, *EDL Feb. 2007 107-110*
- Experimental Study of Data Retention in Nitride Memories by Temperature and Field Acceleration. *Compagnoni, C. M.*, +, *EDL July 2007 628-630*
- Intrinsic Mismatch Between Floating-Gate Nonvolatile Memory Cell and Equivalent Transistor. *Duane, R.*, +, *EDL May 2007 440-442*
- New Operating Mode Based on Electron/Hole Profile Matching in Nitride-Based Nonvolatile Memories. *Furnemont, A.*, +, *EDL April 2007 276-278*
- Predicting Thermal Neutron-Induced Soft Errors in Static Memories Using TCAD and Physics-Based Monte Carlo Simulation Tools. *Warren, K. M.*, +, *EDL Feb. 2007 180-182*

Rapid thermal annealing

- Arsenic Junction Thermal Stability and High-Dose Boron-Pocket Activation During SPER in nMOS Transistors. *Severi, S.*, +, *EDL March 2007 198-200*
- A Program-Erasable High- κ $\text{Hf}_{0.3}\text{N}_{0.2}\text{O}_{0.5}$ MIS Capacitor With Good Retention. *Yang, H. J.*, +, *EDL Oct. 2007 913-915*
- High-Temperature Stable HfLaON p-MOSFETs With High-Work-Function Ir_3Si Gate. *Wu, C. H.*, +, *EDL April 2007 292-294*

Rapid thermal processing

- A Novel Strain Method for Enhancement of 90-nm Node and Beyond FUSI-Gated CMOS Performance. *Lin, C.-T.*, +, *EDL Feb. 2007 111-113*

Relaxation

- Comparison of On-The-Fly, DC I_d-V_g , and Single-Pulse Methods for Evaluating Threshold Voltage Instability in High- κ nMOSFETs. *Heh, D.*, +, *EDL March 2007 245-247*

Reliability

- Improved Reliability and ESD Characteristics of Flip-Chip GaN-Based EDLs With Internal Inverse-Parallel Protection Diodes. *Shei, S.-C.*, +, *EDL May 2007 346-349*
- Improved Electrical Characteristics and Reliability of MILC Poly-Si TFTs Using Fluorine-Ion Implantation. *Chang, C.-P.*, +, *EDL Nov. 2007 990-992*
- Lifetime Extension of RF MEMS Direct Contact Switches in Hot Switching Operations by Ball Grid Array Dimple Design. *Chow, L. L. W.*, +, *EDL June 2007 479-481*
- Thickness Scaling and Reliability Comparison for the Inter-Poly High- κ Dielectrics. *Chen, Y.-Y.*, +, *EDL Aug. 2007 700-702*
- Use of a High-Work-Function Ni Electrode to Improve the Stress Reliability of Analog SrTiO_3 Metal-Insulator-Metal Capacitors. *Chiang, K. C.*, +, *EDL Aug. 2007 694-696*

Resistance

- 35-nm Zigzag T-Gate $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ Metamorphic GaAs HEMTs With an Ultrahigh f_{max} of 520 GHz. *Lee, K.-S.*, +, *EDL Aug. 2007 672-675*
- A Phase Change Memory Compact Model for Multilevel Applications. *Ventrice, D.*, +, *EDL Nov. 2007 973-975*
- Anomalous Cells With Low Reset Resistance in Phase-Change-Memory Arrays. *Mantegazza, D.*, +, *EDL Oct. 2007 865-867*
- Current-Dependent Switching Characteristics of PI-Diphenyl Carbamyl Films. *Kim, M.*, +, *EDL Nov. 2007 967-969*
- Design of On-Chip Transformer With Various Coil Widths to Achieve Minimal Metal Resistance. *Hsu, H.-M.*, +, *EDL Nov. 2007 1029-1032*
- Enhanced Thermal Efficiency in Phase-Change Memory Cell by Double GST Thermally Confined Structure. *Chao, D.-S.*, +, *EDL Oct. 2007 871-873*

- Impact of Preferential P-Diffusion Along the Grain Boundaries on Fine-Grained Polysilicon Solar Cells. *Carnel, L.*, +, *EDL Oct. 2007 899-901*
- N-Channel (110)-Sidewall Strained FinFETs With Silicon-Carbon Source and Drain Stressors and Tensile Capping Layer. *Liow, T.-Y.*, +, *EDL Nov. 2007 1014-1017*
- Remarkable Reduction of On-Resistance by Ion Implantation in GaN/AlGaN/GaN HEMTs With Low Gate Leakage Current. *Nomoto, K.*, +, *EDL Nov. 2007 939-941*
- Submicrometer Inversion-Type Enhancement-Mode InGaAs MOSFET With Atomic-Layer-Deposited Al_2O_3 as Gate Dielectric. *Xuan, Y.*, +, *EDL Nov. 2007 935-938*

Resistors

- Effect of Load Distribution on the Voltage Drop and the Luminance Variation in an AC-PDP. *Kim, J.-S.*, +, *EDL Oct. 2007 896-898*

Resonant frequency

- Improvement of the Conversion Performance of a Resonating Multimode Microelectromechanical Mixer-Filter Through Parametric Amplification. *Koskenvuori, M.*, +, *EDL Nov. 2007 970-972*
- Young's Modulus Measurements in Standard IC CMOS Processes Using MEMS Test Structures. *Marshall, J. C.*, +, *EDL Nov. 2007 960-963*

Resonators

- Millimeter-Wave Bandpass Filters by Standard 0.18- μm CMOS Technology. *Sun, S.*, +, *EDL March 2007 220-222*

Ring oscillators

- Solution-Processed TIPS-Pentacene Organic Thin-Film-Transistor Circuits. *Park, S. K.*, +, *EDL Oct. 2007 877-879*

Robust control

- Robust CoupEDL-Quantum-Well Structure for Use in Electrorefraction Modulators. *Ristic, S.*, +, *EDL Jan. 2007 30-32*

S**S-parameters**

- Extraction of π -Type Substrate Resistance Based on Three-Port Measurement and the Model Verification up to 110 GHz. *Kang, I. M.*, +, *EDL May 2007 425-427*
- A New Method for Identification and Minimization of Distortion Sources in GaN HEMT Devices Based on Volterra Series Analysis. *Srinidhi, E. R.*, +, *EDL May 2007 343-345*
- Temperature Dependence of High Frequency and Noise Performance of Sb-Heterostructure Millimeter-Wave Detectors. *Su, N.*, +, *EDL May 2007 336-339*

SPICE

- An Efficient Macromodeling Approach for Simulating Carbon-Nanotube Field-Emission Triode Devices in Display Applications. *Guo, X.*, +, *EDL Aug. 2007 710-712*

Samarium compounds

- High-Performance Metal-Insulator-Metal Capacitors Using Amorphous $\text{BaSm}_2\text{Ti}_4\text{O}_{12}$ Thin Film. *Jeong, Y. H.*, +, *EDL Jan. 2007 17-20*

Sandwich structures

- Electrically Bistable Thin-Film Device Based on PVK and GNPs Polymer Material. *Song, Y.*, +, *EDL Feb. 2007 107-110*

Sapphire

- HgTe Nanocrystal-Based Thin-Film Transistors Fabricated on Glass Substrates. *Kim, H.*, +, *EDL Jan. 2007 42-44*
- High- κ Al_2O_3 -HfTiO Nanolaminates With Less Than 0.8-nm Equivalent Oxide Thickness. *Mikhelashvili, V.*, +, *EDL Jan. 2007 24-26*
- ON-Resistance Modulation of High Voltage GaN HEMT on Sapphire Substrate Under High Applied Voltage. *Saito, W.*, +, *EDL Aug. 2007 676-678*

Scanning electron microscopy

- The Preparation of Nanocrystalline Silicon by Plasma-Enhanced Hydrogenation for the Fabrication of Light-Emitting Diodes. *Jamei, M.*, +, *EDL March 2007 207-210*

Scattering

- Low-Temperature Transport Characteristics and Quantum-Confinement Effects in Gate-All-Around Si-Nanowire N-MOSFET. *Rustagi, S. C.*, +, *EDL Oct. 2007 909-912*
- Mobility Modeling and Its Extraction Technique for Manufacturing Strained-Si MOSFETs. *Wang, J.-S.*, +, *EDL Nov. 2007 1040-1043*
- The Origin of Electron Mobility Enhancement in Strained MOSFETs. *Hadjisavvas, G.*, +, *EDL Nov. 2007 1018-1020*

Schottky barriers

- A High Schottky-Barrier of 1.1 eV Between Al and S-Passivated p-Type Si(100) Surface. *Song, G.*, +, *EDL Jan. 2007 71-73*
- Effect of Gate Sinking on the Device Performance of the InGaP/AlGaAs/InGaAs Enhancement-Mode PHEMT. *Chu, L. H.*, +, *EDL Feb. 2007 82-85*
- Effective Schottky Barrier Height Reduction Using Sulfur or Selenium at the NiSi/n-Si (100) Interface for Low Resistance Contacts. *Wong, H.-S.*, +, *EDL Dec. 2007 1102-1104*
- Enhanced Gate Swing in InP HEMTs With High Threshold Voltage by Means of InAlAsSb Barrier. *Suemitsu, T.*, +, *EDL Aug. 2007 669-671*
- Improved Carrier Injection in Ultrathin-Body SOI Schottky-Barrier MOS-FETs. *Zhang, M.*, +, *EDL March 2007 223-225*
- Injected Current and Quantum Transmission Coefficient in Low Schottky Barriers: WKB and Airy Approaches. *Rengel, R.*, +, *EDL Feb. 2007 171-173*
- N-channel FinFETs With 25-nm Gate Length and Schottky-Barrier Source and Drain Featuring Ytterbium Silicide. *Lee, R. T. P.*, +, *EDL Feb. 2007 164-167*
- SAW Filters Composed of Interdigital Schottky and Ohmic Contacts on AlGaIn/GaN Heterostructures. *Shigekawa, N.*, +, *EDL Feb. 2007 90-92*
- Schottky-Barrier Height Lowering by an Increase of the Substrate Doping in PtSi Schottky Barrier Source/Drain FETs. *Lousberg, G. P.*, +, *EDL Feb. 2007 123-125*
- Sub-0.1-eV Effective Schottky-Barrier Height for NiSi on n-Type Si (100) Using Antimony Segregation. *Wong, H.-S.*, +, *EDL Aug. 2007 703-705*
- The Leakage Current of the Schottky Contact on the Mesa Edge of AlGaIn/GaN Heterostructure. *Xu, C.*, +, *EDL Nov. 2007 942-944*

Schottky diodes

- Injected Current and Quantum Transmission Coefficient in Low Schottky Barriers: WKB and Airy Approaches. *Rengel, R.*, +, *EDL Feb. 2007 171-173*
- A New Degradation Mechanism in High-Voltage SiC Power MOSFETs. *Agarwal, A.*, +, *EDL July 2007 587-589*
- Schottky-Barrier Height Tuning by Means of Ion Implantation Into Preformed Silicide Films Followed by Drive-In Anneal. *Zhang, Z.*, +, *EDL July 2007 565-568*
- Sub-0.1-eV Effective Schottky-Barrier Height for NiSi on n-Type Si (100) Using Antimony Segregation. *Wong, H.-S.*, +, *EDL Aug. 2007 703-705*

Schottky gate field effect transistors

- Schottky-Barrier Height Lowering by an Increase of the Substrate Doping in PtSi Schottky Barrier Source/Drain FETs. *Lousberg, G. P.*, +, *EDL Feb. 2007 123-125*
- Impact of CF₄ Plasma Treatment on GaN. *Chu, R.*, +, *EDL Sept. 2007 781-783*
- Schottky-Barrier Height Tuning by Means of Ion Implantation Into Preformed Silicide Films Followed by Drive-In Anneal. *Zhang, Z.*, +, *EDL July 2007 565-568*

Schrodinger equation

- Injected Current and Quantum Transmission Coefficient in Low Schottky Barriers: WKB and Airy Approaches. *Rengel, R.*, +, *EDL Feb. 2007 171-173*
- A Quantum-Mechanical View on the Capacitance of a Silicon p-n Junction. *Hurkx, G. A. M.*, +, *EDL April 2007 312-314*

Segregation

- Impacts of Dopant Segregation on the Performance and Interface-State Density of the MOSFET With FUSI NiSi Gate. *Liu, J.*, +, *EDL Jan. 2007 11-13*

Selenium

- Defect Passivation by Selenium-Ion Implantation for Poly-Si Thin Film Transistors. *Lai, J.*, +, *EDL Aug. 2007 725-727*
- Effective Schottky Barrier Height Reduction Using Sulfur or Selenium at the NiSi/n-Si (100) Interface for Low Resistance Contacts. *Wong, H.-S.*, +, *EDL Dec. 2007 1102-1104*

Self-assembly

- Fabrication of Ni Nanocrystal Flash Memories Using a Polymeric Self-Assembly Approach. *Shahrjerdi, D.*, +, *EDL Sept. 2007 793-796*

Semiconductor device breakdown

- Effects of Oxide-Fixed Charge on the Breakdown Voltage of Superjunction Devices. *Balaji, S.*, +, *EDL March 2007 229-231*
- Ar Annealing for Suppression of Gate Oxide Thinning at Shallow Trench Isolation Edge. *Ohashi, T.*, +, *EDL July 2007 562-564*
- Effective Work Function Engineering of Ta_xC_y Metal Gate on Hf-Based Dielectrics. *Yen, F. Y.*, +, *EDL March 2007 201-203*

Normally Off AlGaIn/GaN Low-Density Drain HEMT (LDD-HEMT) With Enhanced Breakdown Voltage and Reduced Current Collapse. *Song, D.*, +, *EDL March 2007 189-191*

On the Use of a SiGe Spike in the Emitter to Improve the f_T \times BV_{CEO} Product of High-Speed SiGe HBTs. *Choi, L. J.*, +, *EDL April 2007 270-272*

P-Channel Germanium FinFET Based on Rapid Melt Growth. *Feng, J.*, +, *EDL July 2007 637-639*

Silicon Dioxide-Encapsulated High-Voltage AlGaIn/GaN HFETs for Power-Switching Applications. *Tipirneni, N.*, +, *EDL Sept. 2007 784-786*

Semiconductor device manufacture

- Submicrometer Copper T-Gate AlGaIn/GaN HFETs: The Gate Metal Stack Effect. *Sun, H. F.*, +, *EDL May 2007 350-353*
- P-Channel Germanium FinFET Based on Rapid Melt Growth. *Feng, J.*, +, *EDL July 2007 637-639*

Semiconductor device measurement

- Three-Dimensional Photodetectors in 3-D Silicon-On-Insulator Technology. *Culurciello, E.*, +, *EDL Feb. 2007 117-119*
- Direct Measurement of Top and Sidewall Interface Trap Density in SOI FinFETs. *Kapila, G.*, +, *EDL March 2007 232-234*
- Submicrometer Inversion-Type Enhancement-Mode InGaAs MOSFET With Atomic-Layer-Deposited Al₂O₃ as Gate Dielectric. *Xuan, Y.*, +, *EDL Nov. 2007 935-938*
- Time-Resolved Temperature Measurement of AlGaIn/GaN Electronic Devices Using Micro-Raman Spectroscopy. *Kuball, M.*, +, *EDL Feb. 2007 86-89*
- Young's Modulus Measurements in Standard IC CMOS Processes Using MEMS Test Structures. *Marshall, J. C.*, +, *EDL Nov. 2007 960-963*

Semiconductor device metallisation

- Conductance Modeling for Graphene Nanoribbon (GNR) Interconnects. *Naeemi, A.*, +, *EDL May 2007 428-431*
- CMOS Dual-Work-Function Engineering by Using Implanted Ni-FUSI. *Lin, C.-T.*, +, *EDL Sept. 2007 831-833*

Semiconductor device models

- Temperature-Oriented Experiment and Simulation as Corroborating Evidence of MOSFET Backscattering Theory. *Chen, M.-J.*, +, *EDL Feb. 2007 177-179*
- A New Method for Identification and Minimization of Distortion Sources in GaN HEMT Devices Based on Volterra Series Analysis. *Srinidhi, E. R.*, +, *EDL May 2007 343-345*
- Admittance Measurements on OFET Channel and Its Modeling With R-C Network. *Jung, K.-D.*, +, *EDL March 2007 204-206*
- Compact Model of Current Collapse in Heterostructure Field-Effect Transistors. *Koudymov, A.*, +, *EDL May 2007 332-335*
- Conductance Modeling for Graphene Nanoribbon (GNR) Interconnects. *Naeemi, A.*, +, *EDL May 2007 428-431*
- Current-Voltage Characteristics of Long-Channel Nanobundle Thin-Film Transistors: A "Bottom-Up" Perspective. *Pimparkar, N.*, +, *EDL Feb. 2007 157-160*
- Extraction of π -Type Substrate Resistance Based on Three-Port Measurement and the Model Verification up to 110 GHz. *Kang, I. M.*, +, *EDL May 2007 425-427*
- Hot-Phonon Effect on the Electrothermal Behavior of Submicrometer III-V HEMTs. *Sadi, T.*, +, *EDL Sept. 2007 787-789*
- Injected Current and Quantum Transmission Coefficient in Low Schottky Barriers: WKB and Airy Approaches. *Rengel, R.*, +, *EDL Feb. 2007 171-173*
- On-Resistance Degradations for Different Stress Conditions in High-Voltage pEDLMOS Transistor With Thick Gate Oxide. *Sun, W.*, +, *EDL July 2007 631-633*
- The Effects of the Injection-Channel Velocity on the Gate Leakage Current of Nanoscale MOSFETs. *Mao, L.*, *EDL Feb. 2007 161-163*

Semiconductor device noise

- Low-Frequency Noise Characteristics in Strained-Si nMOSFETs. *Wang, Y. P.*, +, *EDL Jan. 2007 36-38*
- Flicker Noise and Its Degradation Characteristics Under Electrical Stress in MOSFETs With Thin Strained-Si/SiGe Dual-Quantum Well. *Jiang, Y.*, +, *EDL July 2007 603-605*
- Low-Frequency Noise Assessment of Silicon Passivated Ge pMOSFETs With TiN/TaN/HfO₂ Gate Stack. *Guo, W.*, +, *EDL April 2007 288-291*
- Numerical Simulation of Low-Frequency Noise in Polysilicon Thin-Film Transistors. *Pichon, L.*, +, *EDL Aug. 2007 716-718*

Semiconductor device reliability

- Improved Reliability by Reduction of Hot-Electron Damage in the Vertical Impact-Ionization MOSFET (I-MOS). *Abelein, U.*, +, *EDL Jan. 2007 65-67*

- A Reliability Model for Low-Temperature Polycrystalline Silicon Thin-Film Transistors. *Chen, C.-Y.*, +, *EDL May 2007 392-394*
- Ar Annealing for Suppression of Gate Oxide Thinning at Shallow Trench Isolation Edge. *Ohashi, T.*, +, *EDL July 2007 562-564*
- Effects of Measurement Temperature on NBTI. *Zhang, J. F.*, +, *EDL April 2007 298-300*
- Enhanced Hole Mobility and Reliability of Panel Epi-Like Silicon Transistors Using Backside Green Laser Activation. *Lin, Y.-T.*, +, *EDL Sept. 2007 790-792*
- Highly Reliable Multilevel and 2-bit/cell Operation of Wrapped Select Gate (WSG) SONOS Memory. *Wu, W.-C.*, +, *EDL March 2007 214-216*
- PMOSFET Reliability Study for Direct Silicon Bond (DSB) Hybrid Orientation Technology (HOT). *Huang, Y.-T.*, +, *EDL Sept. 2007 815-817*
- Semiconductor device testing**
- Impact of High- κ Offset Spacer in 65-nm Node SOI Devices. *Ma, M.-W.*, +, *EDL March 2007 238-241*
- Negligible Effect of Process-Induced Strain on Intrinsic NBTI Behavior. *Shickova, A.*, +, *EDL March 2007 242-244*
- Semiconductor devices**
- Carrier Transport Mechanism in a Nanoparticle-Incorporated Organic Bistable Memory Device. *Lin, H.-T.*, +, *EDL July 2007 569-571*
- Semiconductor diodes**
- Effects of Oxide-Fixed Charge on the Breakdown Voltage of Superjunction Devices. *Balaji, S.*, +, *EDL March 2007 229-231*
- A Planar Gunn Diode Operating Above 100 GHz. *Khalid, A.*, +, *EDL Oct. 2007 849-851*
- Semiconductor doping**
- Threshold Current for the Onset of Kirk Effect in Bipolar Transistors With a Fully Depleted Nonuniformly Doped Collector. *van der Toorn, R.*, *EDL Jan. 2007 54-57*
- Application of Plasma-Doping (PLAD) Technique to Reduce Dark Current of CMOS Image Sensors. *Moon, C.-R.*, +, *EDL Feb. 2007 114-116*
- Arsenic Junction Thermal Stability and High-Dose Boron-Pocket Activation During SPER in nMOS Transistors. *Severi, S.*, +, *EDL March 2007 198-200*
- CMOS Dual-Work-Function Engineering by Using Implanted Ni-FUSI. *Lin, C.-T.*, +, *EDL Sept. 2007 831-833*
- Schottky-Barrier Height Lowering by an Increase of the Substrate Doping in PtSi Schottky Barrier Source/Drain FETs. *Lousberg, G. P.*, +, *EDL Feb. 2007 123-125*
- Schottky-Barrier Height Tuning by Means of Ion Implantation Into Preformed Silicide Films Followed by Drive-In Anneal. *Zhang, Z.*, +, *EDL July 2007 565-568*
- Selectively Doped High-Power AlGaIn/GaN MOS-DHFET. *Adivarahan, V.*, +, *EDL March 2007 192-194*
- Semiconductor epitaxial layers**
- Arsenic Junction Thermal Stability and High-Dose Boron-Pocket Activation During SPER in nMOS Transistors. *Severi, S.*, +, *EDL March 2007 198-200*
- Semiconductor junctions**
- Passivation Effects of Aluminum on Polycrystalline Silicon Thin-Film Transistor With Metal-Replaced Junctions. *Zhang, D.*, +, *EDL Feb. 2007 126-128*
- Semiconductor materials**
- SiGe-Channel Confinement Effects for Short-Channel PFETs With Non-bandedge Gate Workfunctions. *Winstead, B.*, +, *EDL Aug. 2007 719-721*
- Semiconductor quantum dots**
- Transport Mechanism of SiGe Dot MOS Tunneling Diodes. *Kuo, P.-S.*, +, *EDL July 2007 596-598*
- Semiconductor quantum wells**
- Flicker Noise and Its Degradation Characteristics Under Electrical Stress in MOSFETs With Thin Strained-Si/SiGe Dual-Quantum Well. *Jiang, Y.*, +, *EDL July 2007 603-605*
- Ultrahigh-Speed 0.5 V Supply Voltage In_{0.7}Ga_{0.3}As Quantum-Well Transistors on Silicon Substrate. *Datta, S.*, +, *EDL Aug. 2007 685-687*
- Semiconductor quantum wires**
- Physical Modeling of Temperature Coefficient of Resistance for Single- and Multi-Wall Carbon Nanotube Interconnects. *Naemi, A.*, +, *EDL Feb. 2007 135-138*
- Semiconductor storage**
- Highly Reliable Multilevel and 2-bit/cell Operation of Wrapped Select Gate (WSG) SONOS Memory. *Wu, W.-C.*, +, *EDL March 2007 214-216*
- Carrier Transport Mechanism in a Nanoparticle-Incorporated Organic Bistable Memory Device. *Lin, H.-T.*, +, *EDL July 2007 569-571*
- Semiconductor technology**
- Effect of Gate Sinking on the Device Performance of the InGaP/AlGaAs/InGaAs Enhancement-Mode PHEMT. *Chu, L. H.*, +, *EDL Feb. 2007 82-85*
- Enhanced Strain Effects in 25-nm Gate-Length Thin-Body nMOSFETs With Silicon-Carbon Source/Drain and Tensile-Stress Liner. *Ang, K.-W.*, +, *EDL April 2007 301-304*
- Semiconductor thin films**
- Crystallization of Double-Layered Silicon Thin Films by Solid Green Laser Annealing for High-Performance Thin-Film Transistors. *Sugawara, Y.*, +, *EDL May 2007 395-397*
- A Novel Low-Temperature Polysilicon Thin-Film Transistors With a Self-Aligned Gate and Raised Source/Drain Formed by the Damascene Process. *Chang, K. M.*, +, *EDL Sept. 2007 806-808*
- Amorphous-SiC_{BN}-Based Metal-Semiconductor-Metal Photodetector for High-Temperature Applications. *Vijayakumar, A.*, +, *EDL Aug. 2007 713-715*
- Defect Passivation by Selenium-Ion Implantation for Poly-Si Thin Film Transistors. *Lai, J.*, +, *EDL Aug. 2007 725-727*
- Semiconductor-insulator-semiconductor devices**
- Profiling of Nitride-Trap-Energy Distribution in SONOS Flash Memory by Using a Variable-Amplitude Low-Frequency Charge-Pumping Technique. *Liao, Y.-Y.*, +, *EDL Sept. 2007 828-830*
- Sensors**
- Field-Controllable Flexible Strain Sensors Using Pentacene Semiconductors. *Ji, T.*, +, *EDL Dec. 2007 1105-1107*
- Series resistance**
- A Constant-Mobility Method to Enable MOSFET Series-Resistance Extraction. *Lin, D.-W.*, +, *EDL Dec. 2007 1132-1134*
- Signal to noise ratio**
- A Wide Dynamic-Range CMOS Image Sensor Using Self-Reset Technique. *Park, D.*, +, *EDL Oct. 2007 890-892*
- Silicon**
- Electrical Characterization of ZrO₂/Si Interface Properties in MOSFETs With ZrO₂ Gate Dielectrics. *Liu, C.-H.*, +, *EDL Jan. 2007 62-64*
- Silicon alloys**
- Impacts of Dopant Segregation on the Performance and Interface-State Density of the MOSFET With FUSI NiSi Gate. *Liu, J.*, +, *EDL Jan. 2007 11-13*
- Silicon carbide**
- A New Degradation Mechanism in High-Voltage SiC Power MOSFETs. *Agarwal, A.*, +, *EDL July 2007 587-589*
- 1200-V 5.2-m Ω · cm² 4H-SiC BJTs With a High Common-Emitter Current Gain. *Lee, H.-S.*, +, *EDL Nov. 2007 1007-1009*
- Comparison of GaN HEMTs on Diamond and SiC Substrates. *Felbinger, J. G.*, +, *EDL Nov. 2007 948-950*
- N-Channel (110)-Sidewall Strained FinFETs With Silicon-Carbon Source and Drain Stressors and Tensile Capping Layer. *Liow, T.-Y.*, +, *EDL Nov. 2007 1014-1017*
- Power Performance of AlGaIn/GaN HEMTs Grown on SiC by Ammonia-MBE at 4 and 10 GHz. *Poblenz, C.*, +, *EDL Nov. 2007 945-947*
- Silicon compounds**
- Effect of F₂ Postmetallization Annealing on the Electrical and Reliability Characteristics of HfSiO Gate Dielectric. *Chang, M.*, +, *EDL Jan. 2007 21-23*
- 1.3- μ m GaInAsN Vertical-Cavity Surface-Emitting Lasers by Oxide-Planarized and Surface-Relief Processes for Single-Mode Operation. *Lee, F.-M.*, +, *EDL Feb. 2007 120-122*
- 1000-V 9.1-m Ω · cm² Normally Off 4H-SiC Lateral RESURF JFET for Power Integrated Circuit Applications. *Zhang, Y.*, +, *EDL May 2007 404-407*
- A Novel Strain Method for Enhancement of 90-nm Node and Beyond FUSI-Gated CMOS Performance. *Lin, C.-T.*, +, *EDL Feb. 2007 111-113*
- Amorphous-SiC_{BN}-Based Metal-Semiconductor-Metal Photodetector for High-Temperature Applications. *Vijayakumar, A.*, +, *EDL Aug. 2007 713-715*
- Amorphous-Silicon Thin-Film Transistors Fabricated at 300 °C on a Free-Standing Foil Substrate of Clear Plastic. *Cherenack, K. H.*, +, *EDL Nov. 2007 1004-1006*
- Demonstration of Asymmetric Gate-Oxide Thickness Four-Terminal FinFETs Having Flexible Threshold Voltage and Good Subthreshold Slope. *Masahara, M.*, +, *EDL March 2007 217-219*
- Demonstration of Long-Pulse Power Amplification at 1 GHz Using 4H-SiC RF BJTs on a Conductive Substrate. *Zhao, F.*, +, *EDL May 2007 398-400*
- Effect of SiN_x Gate Dielectric Deposition Power and Temperature on a-Si:H TFT Stability. *Kattamis, A. Z.*, +, *EDL July 2007 606-608*

- Effective Work Function Engineering of Ta_xC_y Metal Gate on Hf-Based Dielectrics. *Yen, F. Y.*, +, *EDL March 2007 201-203*
- Electrical Properties of nMOSFETs Using the NiSi:Yb FUSI Electrode. *Yu, H. Y.*, +, *EDL Feb. 2007 154-156*
- Enhanced Strain Effects in 25-nm Gate-Length Thin-Body nMOSFETs With Silicon-Carbon Source/Drain and Tensile-Stress Liner. *Ang, K.-W.*, +, *EDL April 2007 301-304*
- Fluorine Passivation in Gate Stacks of Poly-Si/TaN/HfO₂ (and HfSiON/HfO₂)/Si Through Gate Ion Implantation. *Zhang, M. H.*, +, *EDL March 2007 195-197*
- High Mobility Strained Ge pMOSFETs With High- κ /Metal Gate. *Nicholas, G.*, +, *EDL Sept. 2007 825-827*
- High-Voltage Self-Aligned p-Channel DMOS-IGBTs in 4H-SiC. *Sui, Y.*, +, *EDL Aug. 2007 728-730*
- Highly Reliable Multilevel and 2-bit/cell Operation of Wrapped Select Gate (WSG) SONOS Memory. *Wu, W.-C.*, +, *EDL March 2007 214-216*
- Improved Ge Surface Passivation With Ultrathin SiO_x Enabling High-Mobility Surface Channel pMOSFETs Featuring a HfSiO/WN Gate Stack. *Joshi, S.*, +, *EDL April 2007 308-311*
- Improving the Performance of SiGe Metal-Semiconductor-Metal Photodetectors by Using an Amorphous Silicon Passivation Layer. *Chen, Y. H.*, +, *EDL Dec. 2007 1111-1113*
- Low-Frequency Noise Assessment of Silicon Passivated Ge pMOSFETs With TiN/TaN/HfO₂ Gate Stack. *Guo, W.*, +, *EDL April 2007 288-291*
- N-Channel (110)-Sidewall Strained FinFETs With Silicon-Carbon Source and Drain Stressors and Tensile Capping Layer. *Liow, T.-Y.*, +, *EDL Nov. 2007 1014-1017*
- N-channel FinFETs With 25-nm Gate Length and Schottky-Barrier Source and Drain Featuring Ytterbium Silicide. *Lee, R. T. P.*, +, *EDL Feb. 2007 164-167*
- Negligible Effect of Process-Induced Strain on Intrinsic NBTI Behavior. *Shickova, A.*, +, *EDL March 2007 242-244*
- RF Power Measurements of InAlN/GaN Unstrained HEMTs on SiC Substrates at 10 GHz. *Jessen, G. H.*, +, *EDL May 2007 354-356*
- Silicon Dioxide-Encapsulated High-Voltage AlGaN/GaN HFETs for Power-Switching Applications. *Tipirneni, N.*, +, *EDL Sept. 2007 784-786*
- Study of the Erase Mechanism of MANOS (Metal/Al₂O₃/SiN/SiO₂/Si) Device. *Lai, S.*, +, *EDL July 2007 643-645*
- The Application of an Ultrathin ALD HfSiON Cap Layer on SiON Dielectrics for Ni-FUSI CMOS Technology Targeting at Low-Power Applications. *Chang, S. Z.*, +, *EDL July 2007 634-636*
- Time-Resolved Temperature Measurement of AlGaN/GaN Electronic Devices Using Micro-Raman Spectroscopy. *Kuball, M.*, +, *EDL Feb. 2007 86-89*
- Yttrium- and Terbium-Based Interlayer on SiO₂ and HfO₂ Gate Dielectrics for Work Function Modulation of Nickel Fully Silicided Gate in nMOSFET. *Lim, A. E.-J.*, +, *EDL June 2007 482-485*
- Silicon germanium**
- Strained n-Channel Transistors With Silicon Source and Drain Regions and Embedded Silicon/Germanium as Strain-Transfer Structure. *Ang, K.-W.*, +, *EDL July 2007 609-612*
- Impact of Local Strain From Selective Epitaxial Germanium With Thin Si/SiGe Buffer on High-Performance p-i-n Photodetectors With a Low Thermal Budget. *Loh, W. Y.*, +, *EDL Nov. 2007 984-986*
- On the Low-Frequency Noise of pMOSFETs With Embedded SiGe Source/Drain and Fully Silicided Metal Gate. *Simoen, E.*, +, *EDL Nov. 2007 987-989*
- Strained p-Channel FinFETs With Extended II-Shaped Silicon-Germanium Source and Drain Stressors. *Tan, K.-M.*, +, *EDL Oct. 2007 905-908*
- Silicon on insulator technology**
- On the Origin of the Excess Low-Frequency Noise in Graded-Channel Silicon-on-Insulator nMOSFETs. *Simoen, E.*, +, *EDL Oct. 2007 919-921*
- Trigate FET Device Characteristics Improvement Using a Hydrogen Anneal Process With a Novel Hard Mask Approach. *Zaman, R. J.*, +, *EDL Oct. 2007 916-918*
- Silicon-on-insulator**
- Long Retention of Gain-Cell Dynamic Random Access Memory With Undoped Memory Node. *Nishiguchi, K.*, +, *EDL Jan. 2007 48-50*
- A Novel 700-V SOI LDMOS With Double-Sided Trench. *Luo, X.*, +, *EDL May 2007 422-424*
- A Novel Dual-Polarity Nonvolatile Memory. *Lin, H.*, +, *EDL May 2007 412-415*
- Direct Measurement of Top and Sidewall Interface Trap Density in SOI FinFETs. *Kapila, G.*, +, *EDL March 2007 232-234*
- Duration of the High Breakdown Voltage Phase in Deep Depletion SOI LDMOS. *Napoli, E.*, *EDL Aug. 2007 753-755*
- Electron Transport in Strained-Silicon Directly on Insulator Ultrathin-Body n-MOSFETs With Body Thickness Ranging From 2 to 25 nm. *Gomez, L.*, +, *EDL April 2007 285-287*
- Evaluation of RF Capacitance Extraction for Ultrathin Ultraleaky SOI MOS Devices. *Yu, C.*, +, *EDL Jan. 2007 45-47*
- Impact of High- κ Offset Spacer in 65-nm Node SOI Devices. *Ma, M.-W.*, +, *EDL March 2007 238-241*
- Impact of Parameter Variations and Random Dopant Fluctuations on Short-Channel Fully Depleted SOI MOSFETs With Extremely Thin BOX. *Ohtou, T.*, +, *EDL Aug. 2007 740-742*
- Improved Carrier Injection in Ultrathin-Body SOI Schottky-Barrier MOSFETs. *Zhang, M.*, +, *EDL March 2007 223-225*
- Low-Temperature Polymer-Based Three-Dimensional Silicon Integration. *Kim, S.*, +, *EDL Aug. 2007 706-709*
- New Insights on "Capacitorless" Floating-Body DRAM Cells. *Fossum, J. G.*, +, *EDL June 2007 513-516*
- Novel Approach to Reduce Source/Drain Series and Contact Resistance in High-Performance UT-SOI CMOS Devices Using Selective Electrodeless CoWP or CoB Process. *Pan, J.*, +, *EDL Aug. 2007 691-693*
- Observation of Threshold-Voltage Instability in Single-Crystal Silicon TFTs on Flexible Plastic Substrate. *Yuan, H.-C.*, +, *EDL July 2007 590-592*
- P-Channel Germanium FinFET Based on Rapid Melt Growth. *Feng, J.*, +, *EDL July 2007 637-639*
- Schottky-Barrier Height Lowering by an Increase of the Substrate Doping in PtSi Schottky Barrier Source/Drain FETs. *Lousberg, G. P.*, +, *EDL Feb. 2007 123-125*
- Stress Hybridization for Multigate Devices Fabricated on Supercritical Strained-SOI (SC-SSOI). *Collaert, N.*, +, *EDL July 2007 646-648*
- Strong Efficiency Improvement of SOI-EDLs Through Carrier Confinement. *Hoang, T.*, +, *EDL May 2007 383-385*
- Substrate Bias Effect Linked to Parasitic Series Resistance in Multiple-Gate SOI MOSFETs. *Rudenko, T.*, +, *EDL Sept. 2007 834-836*
- Symmetric Vertical Parallel Plate Capacitors for On-Chip RF Circuits in 65-nm SOI Technology. *Kim, D.*, +, *EDL July 2007 616-618*
- Three-Dimensional Photodetectors in 3-D Silicon-On-Insulator Technology. *Culurciello, E.*, +, *EDL Feb. 2007 117-119*
- Valence Band Offset Measurements on Thin Silicon-on-Insulator MOSFETs. *van der Steen, J.-L. P. J.*, +, *EDL Sept. 2007 821-824*
- 100-GHz Quasi-Yagi Antenna in Silicon Technology. *Sun, M.*, +, *EDL May 2007 455-457*
- A High Schottky-Barrier of 1.1 eV Between Al and S-Passivated p-Type Si(100) Surface. *Song, G.*, +, *EDL Jan. 2007 71-73*
- A Novel Approach in Separating the Roles of Electrons and Holes in Causing Degradation in Hf-Based MOSFET Devices by Using Stress-Anneal Technique. *Akbar, M. S.*, +, *EDL Feb. 2007 132-134*
- A Novel LTPS-TFT Pixel Circuit Compensating for TFT Threshold-Voltage Shift and OEDL Degradation for AMOEDL. *Lin, C.-L.*, +, *EDL Feb. 2007 129-131*
- A Novel Nanowire Channel Poly-Si TFT Functioning as Transistor and Non-volatile SONOS Memory. *Chen, S.-C.*, +, *EDL Sept. 2007 809-811*
- A Novel Silicon Photovoltaic Cell Using a Low-Temperature Quasi-Epitaxial Silicon Emitter. *Farrokh-Baroughi, M.*, +, *EDL July 2007 575-577*
- A Novel Single Polysilicon EEPROM Cell With a Polyfinger Capacitor. *Na, K.-Y.*, +, *EDL Nov. 2007 1047-1049*
- A Program-Erasable High- κ Hf_{0.3}N_{0.2}O_{0.5} MIS Capacitor With Good Retention. *Yang, H. J.*, +, *EDL Oct. 2007 913-915*
- A Quantum-Mechanical View on the Capacitance of a Silicon p-n Junction. *Hurkx, G. A. M.*, +, *EDL April 2007 312-314*
- A Reliability Model for Low-Temperature Polycrystalline Silicon Thin-Film Transistors. *Chen, C.-Y.*, +, *EDL May 2007 392-394*
- A Simple Spacer Technique to Fabricate Poly-Si TFTs With 50-nm Nanowire Channels. *Chang, C.-W.*, +, *EDL Nov. 2007 993-995*
- Achieving Low- V_T Ni-FUSI CMOS by Ultra-Thin Dy₂O₃ Capping of Hafnium Silicate Dielectrics. *Veloso, A.*, +, *EDL Nov. 2007 980-983*
- AlGaN Photodetectors Prepared on Si Substrates. *Chiou, Y. Z.*, +, *EDL April 2007 264-266*
- An Unassisted, Low Trigger-, and High Holding-Voltage SCR (uSCR) for On-Chip ESD-Protection Applications. *Lou, L.*, +, *EDL Dec. 2007 1120-1122*
- CMOS Inverter Based on Gate-All-Around Silicon-Nanowire MOSFETs Fabricated Using Top-Down Approach. *Rustagi, S. C.*, +, *EDL Nov. 2007 1021-1024*

- Crystallization of Double-Layered Silicon Thin Films by Solid Green Laser Annealing for High-Performance Thin-Film Transistors. *Sugawara, Y., +, EDL May 2007 395-397*
- Degradation of Laser-Crystallized Laterally Grown Poly-Si TFT under Dynamic Stress. *Liu, P.-T., +, EDL May 2007 401-403*
- Demonstration of Low V_i Ni-FUSI N-MOSFETs With SiON Dielectrics by Using a Dy₂O₃ Cap Layer. *Yu, H. Y., +, EDL Nov. 2007 957-959*
- Demonstration of Metal-Gated Low V_i n-MOSFETs Using a Poly-Si/TaN/Dy₂O₃/SiON Gate Stack With a ScaEDL EOT Value. *Yu, H. Y., +, EDL July 2007 656-658*
- Detection of Border Trap Density and Energy Distribution Along the Gate Dielectric Bulk of High- κ Gated MOS Devices. *Lu, C.-Y., +, EDL May 2007 432-435*
- Effect of Gate Dopant Diffusion on Leakage Current in n⁺ Poly-Si/HfO₂ and Examination of Leakage Paths by Conducting Atomic Force Microscopy. *Yu, X., +, EDL May 2007 373-375*
- Electrical Compensation of OEDL Luminance Degradation. *Chaji, G. R., +, EDL Dec. 2007 1108-1110*
- Gate Workfunction Engineering in Bulk FinFETs for Sub-50-nm DRAM Cell Transistors. *Park, K.-H., +, EDL Feb. 2007 148-150*
- High-Performance Polycrystalline-Silicon TFT by Heat-Retaining Enhanced Lateral Crystallization. *Liu, P.-T., +, EDL Aug. 2007 722-724*
- High-Performance Self-Aligned Bottom-Gate Low-Temperature Poly-Silicon Thin-Film Transistors With Excimer Laser Crystallization. *Tsai, C.-C., +, EDL July 2007 599-602*
- High-Performance Short-Channel Double-Gate Low-Temperature Polysilicon Thin-Film Transistors Using Excimer Laser Crystallization. *Tsai, C.-C., +, EDL Nov. 2007 1010-1013*
- High-Performance and Low-Temperature-Compatible p-Channel Polycrystalline-Silicon TFTs Using Hafnium-Silicate Gate Dielectric. *Yang, M.-J., +, EDL Oct. 2007 902-904*
- High-Quality Factor Electrolyte Insulator Silicon Capacitor for Wireless Chemical Sensing. *Garcia-Canton, J., +, EDL Jan. 2007 27-29*
- Hot-Carrier Effects in Strained n-Channel Transistor With Silicon-Carbon (Si_{1-y}C_y) Source/Drain Stressors and Its Orientation Dependence. *Ang, K.-W., +, EDL Nov. 2007 996-999*
- Impact of Local Strain From Selective Epitaxial Germanium With Thin Si/SiGe Buffer on High-Performance p-i-n Photodetectors With a Low Thermal Budget. *Loh, W. Y., +, EDL Nov. 2007 984-986*
- Impact of Preferential P-Diffusion Along the Grain Boundaries on Fine-Grained Polysilicon Solar Cells. *Carnel, L., +, EDL Oct. 2007 899-901*
- Improved Electrical Characteristics of Ge-on-Si Field-Effect Transistors With ControlEDL Ge Epitaxial Layer Thickness on Si Substrates. *Oh, J., +, EDL Nov. 2007 1044-1046*
- Improving the Electrical Properties of NILC Poly-Si Films Using a Gettering Substrate. *Hu, C.-M., +, EDL Nov. 2007 1000-1003*
- Investigation of Carrier Transport in Germanium MOSFETs With WN/Al₂O₃/AlN Gate Stacks. *Ritenour, A., +, EDL Aug. 2007 746-749*
- Low-Frequency Noise Assessment of Silicon Passivated Ge pMOSFETs With TiN/TaN/HfO₂ Gate Stack. *Guo, W., +, EDL April 2007 288-291*
- Low-Temperature Polymer-Based Three-Dimensional Silicon Integration. *Kim, S., +, EDL Aug. 2007 706-709*
- Metal-Oxide-High- κ Dielectric-Oxide-Semiconductor (MOHOS) Capacitors and Field-Effect Transistors for Memory Applications. *Hsu, H., +, EDL Nov. 2007 964-966*
- Millimeter-Wave Bandpass Filters by Standard 0.18- μ m CMOS Technology. *Sun, S., +, EDL March 2007 220-222*
- N-Channel (110)-Sidewall Strained FinFETs With Silicon-Carbon Source and Drain Stressors and Tensile Capping Layer. *Liow, T.-Y., +, EDL Nov. 2007 1014-1017*
- NMOS Compatible Work Function of TaN Metal Gate With Erbium-Oxide-Doped Hafnium Oxide Gate Dielectric. *Chen, J., +, EDL Oct. 2007 862-864*
- Negligible Effect of Process-Induced Strain on Intrinsic NBTI Behavior. *Shickova, A., +, EDL March 2007 242-244*
- Normally Off n-Channel GaN MOSFETs on Si Substrates Using an SAG Technique and Ion Implantation. *Kabayashi, H., +, EDL Dec. 2007 1077-1079*
- Numerical Simulation of Low-Frequency Noise in Polysilicon Thin-Film Transistors. *Pichon, L., +, EDL Aug. 2007 716-718*
- Observation of Metal-Layer Stress on Si Nanowires in Gate-All-Around High- κ /Metal-Gate Device Structures. *Singh, N., +, EDL July 2007 558-561*
- On the Enhanced Impact Ionization in Uniaxial Strained p-MOSFETs. *Su, P., +, EDL July 2007 649-651*
- On the Low-Frequency Noise of pMOSFETs With Embedded SiGe Source/Drain and Fully Silicided Metal Gate. *Simoen, E., +, EDL Nov. 2007 987-989*
- Passivation Effects of Aluminum on Polycrystalline Silicon Thin-Film Transistor With Metal-Replaced Junctions. *Zhang, D., +, EDL Feb. 2007 126-128*
- Piezoresistance Coefficients of (100) Silicon nMOSFETs Measured at Low and High (~1.5 GPa) Channel Stress. *Suthram, S., +, EDL Jan. 2007 58-61*
- Reduction of Threshold Voltage by Diffusion Control Technique in p-MISFETs Using Poly-Si/TiN/HfSiON Gate Stacks. *Kawahara, T., +, EDL Oct. 2007 868-870*
- Remarkable Reduction of On-Resistance by Ion Implantation in GaN/AlGaIn/GaN HEMTs With Low Gate Leakage Current. *Nomoto, K., +, EDL Nov. 2007 939-941*
- Schottky-Barrier Height Lowering by an Increase of the Substrate Doping in PtSi Schottky Barrier Source/Drain FETs. *Lousberg, G. P., +, EDL Feb. 2007 123-125*
- Stability of Amorphous-Silicon and Nanocrystalline Silicon Thin-Film Transistors Under DC and AC Stress. *Hatzopoulos, A. T., +, EDL Sept. 2007 803-805*
- Strained n-Channel Transistors With Silicon Source and Drain Regions and Embedded Silicon/Germanium as Strain-Transfer Structure. *Ang, K.-W., +, EDL July 2007 609-612*
- Strained p-Channel FinFETs With Extended II-Shaped Silicon-Germanium Source and Drain Stressors. *Tan, K.-M., +, EDL Oct. 2007 905-908*
- Strained-Si Channel Super-Self-Aligned Back-Gate/Double-Gate Planar Transistors. *Lin, H., +, EDL June 2007 506-508*
- Sub-0.1-eV Effective Schottky-Barrier Height for NiSi on n-Type Si (100) Using Antimony Segregation. *Wong, H.-S., +, EDL Aug. 2007 703-705*
- The Origin of Electron Mobility Enhancement in Strained MOSFETs. *Hadjisavvas, G., +, EDL Nov. 2007 1018-1020*
- The Preparation of Nanocrystalline Silicon by Plasma-Enhanced Hydrogenation for the Fabrication of Light-Emitting Diodes. *Jamei, M., +, EDL March 2007 207-210*
- Transport Mechanism of SiGe Dot MOS Tunneling Diodes. *Kuo, P.-S., +, EDL July 2007 596-598*
- Trigate FET Device Characteristics Improvement Using a Hydrogen Anneal Process With a Novel Hard Mask Approach. *Zaman, R. J., +, EDL Oct. 2007 916-918*
- Ultrahigh-Speed 0.5 V Supply Voltage In_{0.7}Ga_{0.3}As Quantum-Well Transistors on Silicon Substrate. *Data, S., +, EDL Aug. 2007 685-687*
- Vertically Stacked SiGe Nanowire Array Channel CMOS Transistors. *Fang, W. W., +, EDL March 2007 211-213*
- Sintering**
- HgTe Nanocrystal-Based Thin-Film Transistors Fabricated on Glass Substrates. *Kim, H., +, EDL Jan. 2007 42-44*
- Solar cells**
- A Novel Silicon Photovoltaic Cell Using a Low-Temperature Quasi-Epitaxial Silicon Emitter. *Farrokh-Baroughi, M., +, EDL July 2007 575-577*
- Solders**
- Electromigration Resistant Power Delivery Systems. *Sekar, D. C., +, EDL Aug. 2007 767-769*
- Solenoids**
- CMOS-Compatible Micromachined Toroid and Solenoid Inductors With High Q-Factors. *Zine-El-Abidine, I., +, EDL March 2007 226-228*
- Solid lasers**
- High-Performance Short-Channel Double-Gate Low-Temperature Polysilicon Thin-Film Transistors Using Excimer Laser Crystallization. *Tsai, C.-C., +, EDL Nov. 2007 1010-1013*
- Solid phase epitaxial growth**
- PMOSFET Reliability Study for Direct Silicon Bond (DSB) Hybrid Orientation Technology (HOT). *Huang, Y.-T., +, EDL Sept. 2007 815-817*
- Solids**
- On the Origin of the Excess Low-Frequency Noise in Graded-Channel Silicon-on-Insulator nMOSFETs. *Simoen, E., +, EDL Oct. 2007 919-921*
- Space-charge limited devices**
- Carrier Transport Mechanism in a Nanoparticle-Incorporated Organic Bistable Memory Device. *Lin, H.-T., +, EDL July 2007 569-571*
- Spin coating**
- HgTe Nanocrystal-Based Thin-Film Transistors Fabricated on Glass Substrates. *Kim, H., +, EDL Jan. 2007 42-44*
- Spontaneous emission**
- A New Degradation Mechanism in High-Voltage SiC Power MOSFETs. *Agarwal, A., +, EDL July 2007 587-589*

Springs

Improvement of the Conversion Performance of a Resonating Multimode Microelectromechanical Mixer-Filter Through Parametric Amplification. *Koskenvuori, M.*, +, *EDL Nov. 2007 970-972*

Sputter deposition

Room-Temperature Deposited Titanium Silicate Thin Films for MIM Capacitor Applications. *Brassard, D.*, +, *EDL April 2007 261-263*
An Improved Planar Triode With ZnO Nanopin Field Emitters. *Wei, L.*, +, *EDL Aug. 2007 688-690*

Sputter etching

Performance Improvement of Organic Thin-Film Transistors by Electrode/Pentacene Interface Treatment Using a Hydrogen Plasma. *Lee, J.-W.*, +, *EDL May 2007 379-382*

Sputtering

Fast Thin-Film Transistor Circuits Based on Amorphous Oxide Semiconductor. *Ofuji, M.*, +, *EDL April 2007 273-275*
Achieving Conduction Band-Edge Effective Work Functions by La₂O₃ Capping of Hafnium Silicates. *Ragnarsson, L.-A.*, +, *EDL June 2007 486-488*
Amorphous-SiC_N-Based Metal-Semiconductor-Metal Photodetector for High-Temperature Applications. *Vijayakumar, A.*, +, *EDL Aug. 2007 713-715*

Stability

Power Stability of AlGa_N/Ga_N HFETs at 20 W/mm in the Pinched-Off Operation Mode. *Koudymov, A.*, +, *EDL Jan. 2007 5-7*
Comparison of On-The-Fly, DC I_d - V_g , and Single-Pulse Methods for Evaluating Threshold Voltage Instability in High- κ nMOSFETs. *Heh, D.*, +, *EDL March 2007 245-247*
Negligible Effect of Process-Induced Strain on Intrinsic NBTI Behavior. *Shickova, A.*, +, *EDL March 2007 242-244*

Strain

Strained n-Channel Transistors With Silicon Source and Drain Regions and Embedded Silicon/Germanium as Strain-Transfer Structure. *Ang, K.-W.*, +, *EDL July 2007 609-612*
Hot-Carrier Effects in Strained n-Channel Transistor With Silicon-Carbon (Si_{1-y}C_y) Source/Drain Stressors and Its Orientation Dependence. *Ang, K.-W.*, +, *EDL Nov. 2007 996-999*
Impact of Local Strain From Selective Epitaxial Germanium With Thin Si/SiGe Buffer on High-Performance p-i-n Photodetectors With a Low Thermal Budget. *Loh, W. Y.*, +, *EDL Nov. 2007 984-986*
On the Enhanced Impact Ionization in Uniaxial Strained p-MOSFETs. *Su, P.*, +, *EDL July 2007 649-651*
On the Low-Frequency Noise of pMOSFETs With Embedded SiGe Source/Drain and Fully Silicided Metal Gate. *Simoen, E.*, +, *EDL Nov. 2007 987-989*
Strained p-Channel FinFETs With Extended II-Shaped Silicon-Germanium Source and Drain Stressors. *Tan, K.-M.*, +, *EDL Oct. 2007 905-908*
The Origin of Electron Mobility Enhancement in Strained MOSFETs. *Hadjisavvas, G.*, +, *EDL Nov. 2007 1018-1020*

Stress effects

A New Degradation Mechanism in High-Voltage SiC Power MOSFETs. *Agarwal, A.*, +, *EDL July 2007 587-589*
Stress Hybridization for Multigate Devices Fabricated on Supercritical Strained-SOI (SC-SSOI). *Collaert, N.*, +, *EDL July 2007 646-648*

Stress measurement

Measurement of Channel Stress Using Gate Direct Tunneling Current in Uniaxially Stressed nMOSFETs. *Hsieh, C.-Y.*, +, *EDL Sept. 2007 818-820*
Young's Modulus Measurements in Standard IC CMOS Processes Using MEMS Test Structures. *Marshall, J. C.*, +, *EDL Nov. 2007 960-963*
A Novel Single Polysilicon EEPROM Cell With a Polyfinger Capacitor. *Na, K.-Y.*, +, *EDL Nov. 2007 1047-1049*
Amorphous-Silicon Thin-Film Transistors Fabricated at 300 °C on a Free-Standing Foil Substrate of Clear Plastic. *Cherenack, K. H.*, +, *EDL Nov. 2007 1004-1006*
Constant Bias Stress Effects on Threshold Voltage of Pentacene Thin-Film Transistors Employing Polyvinylphenol Gate Dielectric. *Kim, T. H.*, +, *EDL Oct. 2007 874-876*
Effect of SiN_x Gate Dielectric Deposition Power and Temperature on a-Si:H TFT Stability. *Kattamis, A. Z.*, +, *EDL July 2007 606-608*
Hot-Carrier Effects in Strained n-Channel Transistor With Silicon-Carbon (Si_{1-y}C_y) Source/Drain Stressors and Its Orientation Dependence. *Ang, K.-W.*, +, *EDL Nov. 2007 996-999*
Improved Electrical Characteristics and Reliability of MILC Poly-Si TFTs Using Fluorine-Ion Implantation. *Chang, C.-P.*, +, *EDL Nov. 2007 990-992*

Mobility Modeling and Its Extraction Technique for Manufacturing Strained-Si MOSFETs. *Wang, J.-S.*, +, *EDL Nov. 2007 1040-1043*
N-Channel (110)-Sidewall Strained FinFETs With Silicon-Carbon Source and Drain Stressors and Tensile Capping Layer. *Liow, T.-Y.*, +, *EDL Nov. 2007 1014-1017*

Strained p-Channel FinFETs With Extended II-Shaped Silicon-Germanium Source and Drain Stressors. *Tan, K.-M.*, +, *EDL Oct. 2007 905-908*

Strontium compounds

High-Temperature Leakage Improvement in Metal-Insulator-Metal Capacitors by Work-Function Tuning. *Chiang, K. C.*, +, *EDL March 2007 235-237*
Use of a High-Work-Function Ni Electrode to Improve the Stress Reliability of Analog SrTiO₃ Metal-Insulator-Metal Capacitors. *Chiang, K. C.*, +, *EDL Aug. 2007 694-696*

Substrates

Low-Frequency Noise Assessment of Silicon Passivated Ge pMOSFETs With TiN/TaN/ HfO₂ Gate Stack. *Guo, W.*, +, *EDL April 2007 288-291*
Amorphous-Silicon Thin-Film Transistors Fabricated at 300 °C on a Free-Standing Foil Substrate of Clear Plastic. *Cherenack, K. H.*, +, *EDL Nov. 2007 1004-1006*
Body Thickness Dependence of Impact Ionization in a Multiple-Gate FinFET. *Han, J.-W.*, +, *EDL July 2007 625-627*
Comparison of GaN HEMTs on Diamond and SiC Substrates. *Felbinger, J. G.*, +, *EDL Nov. 2007 948-950*
Demonstration of Long-Pulse Power Amplification at 1 GHz Using 4H-SiC RF BJTs on a Conductive Substrate. *Zhao, F.*, +, *EDL May 2007 398-400*
Effect of Substrate Parasitic Inductance on Silicon-Based Transmission Lines and On-Chip Inductors. *Huang, F.*, +, *EDL Nov. 2007 1025-1028*
Effects of Sulfur Passivation on Germanium MOS Capacitors With HfON Gate Dielectric. *Xie, R.*, +, *EDL Nov. 2007 976-979*
Extraction of π -Type Substrate Resistance Based on Three-Port Measurement and the Model Verification up to 110 GHz. *Kang, I. M.*, +, *EDL May 2007 425-427*
Flexible Full-Color AMOEDL on Ultrathin Metal Foil. *Jeong, J. K.*, +, *EDL May 2007 389-391*
Impact of Parameter Variations and Random Dopant Fluctuations on Short-Channel Fully Depleted SOI MOSFETs With Extremely Thin BOX. *Ohtou, T.*, +, *EDL Aug. 2007 740-742*
Improved Electrical Characteristics of Ge-on-Si Field-Effect Transistors With Control EDL Ge Epitaxial Layer Thickness on Si Substrates. *Oh, J.*, +, *EDL Nov. 2007 1044-1046*
Improving the Electrical Properties of NILC Poly-Si Films Using a Gettering Substrate. *Hu, C.-M.*, +, *EDL Nov. 2007 1000-1003*
Normally Off n-Channel GaN MOSFETs on Si Substrates Using an SAG Technique and Ion Implantation. *Kambayashi, H.*, +, *EDL Dec. 2007 1077-1079*
Observation of Threshold-Voltage Instability in Single-Crystal Silicon TFTs on Flexible Plastic Substrate. *Yuan, H.-C.*, +, *EDL July 2007 590-592*
Power Performance of AlGa_N/Ga_N HEMTs Grown on SiC by Ammonia-MBE at 4 and 10 GHz. *Poblencz, C.*, +, *EDL Nov. 2007 945-947*
Reduction of Threshold Voltage by Diffusion Control Technique in p-MIS-FETs Using Poly-Si/TiN/HfSiON Gate Stacks. *Kawahara, T.*, +, *EDL Oct. 2007 868-870*
Solution-Processed TIPS-Pentacene Organic Thin-Film-Transistor Circuits. *Park, S. K.*, +, *EDL Oct. 2007 877-879*
Solution-Processed n-Type Organic Field-Effect Transistors With High ON/OFF Current Ratios Based on Fullerene Derivatives. *Tiwari, S. P.*, +, *EDL Oct. 2007 880-883*
Substrate Bias Effect Linked to Parasitic Series Resistance in Multiple-Gate SOI MOSFETs. *Rudenko, T.*, +, *EDL Sept. 2007 834-836*
Ultrahigh-Speed 0.5 V Supply Voltage In_{0.7}Ga_{0.3}As Quantum-Well Transistors on Silicon Substrate. *Datta, S.*, +, *EDL Aug. 2007 685-687*

Sulfur
Effective Schottky Barrier Height Reduction Using Sulfur or Selenium at the NiSi/n-Si (100) Interface for Low Resistance Contacts. *Wong, H.-S.*, +, *EDL Dec. 2007 1102-1104*

Superconductive tunnelling
Simulation of Graphene Nanoribbon Field-Effect Transistors. *Fiori, G.*, +, *EDL Aug. 2007 760-762*

Surface acoustic wave filters
SAW Filters Composed of Interdigital Schottky and Ohmic Contacts on AlGa_N/Ga_N Heterostructures. *Shigekawa, N.*, +, *EDL Feb. 2007 90-92*

Surface emitting lasers

1.3- μm GaInAsN Vertical-Cavity Surface-Emitting Lasers by Oxide-Planarized and Surface-Relief Processes for Single-Mode Operation. *Lee, F.-M.*, +, *EDL Feb. 2007 120-122*

Surface morphology

Metamorphic Heterostructure InP/GaAsSb/InP HBTs on GaAs Substrates by MOCVD. *Zhou, W.*, +, *EDL July 2007 539-542*

Surface states

Electrical Characterization of ZrO_2/Si Interface Properties in MOSFETs With ZrO_2 Gate Dielectrics. *Liu, C.-H.*, +, *EDL Jan. 2007 62-64*

Surface treatment

Effects of Sulfur Passivation on Germanium MOS Capacitors With HfON Gate Dielectric. *Xie, R.*, +, *EDL Nov. 2007 976-979*

Switches

Nonvolatile Multilevel Conductance and Memory Effect in Molecule-Based Devices. *Guo, P.*, +, *EDL July 2007 572-574*

OFF-State Avalanche-Breakdown-Induced ON-Resistance Degradation in Lateral DMOS Transistors. *Chen, J. F.*, +, *EDL Nov. 2007 1033-1035*

Active Pixel Concept Combined With Organic Photodiode for Imaging Devices. *Tedde, S.*, +, *EDL Oct. 2007 893-895*

Anomalous Cells With Low Reset Resistance in Phase-Change-Memory Arrays. *Mantegazza, D.*, +, *EDL Oct. 2007 865-867*

Current-Dependent Switching Characteristics of PI-Diphenyl Carbamyl Films. *Kim, M.*, +, *EDL Nov. 2007 967-969*

Switching

Effect of Top Electrode Material on Resistive Switching Properties of ZrO_2 Film Memory Devices. *Lin, C.-Y.*, +, *EDL May 2007 366-368*

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A Simple and Effective Approach to Improve the Output Linearity of Switched-Current AMOEDL Pixel Circuitry. *Guo, X.*, +, *EDL Oct. 2007 887-889*

System-on-chip

Ferrite-Integrated On-Chip Inductors for RF ICs. *Yang, C.*, +, *EDL July 2007 652-655*

Low-Temperature Polymer-Based Three-Dimensional Silicon Integration. *Kim, S.*, +, *EDL Aug. 2007 706-709*

T**Tantalum compounds**

High-Temperature Leakage Improvement in Metal-Insulator-Metal Capacitors by Work-Function Tuning. *Chiang, K. C.*, +, *EDL March 2007 235-237*

Achieving Conduction Band-Edge Effective Work Functions by La_2O_3 Capping of Hafnium Silicates. *Ragnarsson, L.-A.*, +, *EDL June 2007 486-488*

Border-Trap Characterization in High- κ Strained-Si MOSFETs. *Maji, D.*, +, *EDL Aug. 2007 731-733*

Effective Work Function Engineering of Ta_xC_y Metal Gate on Hf-Based Dielectrics. *Yen, F. Y.*, +, *EDL March 2007 201-203*

Fluorine Passivation in Gate Stacks of Poly-Si/TaN/HfO₂ (and HfSiON/HfO₂)/Si Through Gate Ion Implantation. *Zhang, M. H.*, +, *EDL March 2007 195-197*

Low-Frequency Noise Assessment of Silicon Passivated Ge pMOSFETs With TiN/TaN/HfO₂ Gate Stack. *Guo, W.*, +, *EDL April 2007 288-291*

Nitrogen Incorporation in HfSiO(N)/Ta_n Gate Stacks: Impact on Performances and NBTI. *Aoulaiche, M.*, +, *EDL July 2007 613-615*

Observation of Metal-Layer Stress on Si Nanowires in Gate-All-Around High- κ /Metal-Gate Device Structures. *Singh, N.*, +, *EDL July 2007 558-561*

Technology CAD (electronics)

Experimental and TCAD Investigation of the Two Components of the Impact Ionization MOSFET (IMOS) Switching. *Mayer, F.*, +, *EDL July 2007 619-621*

Telegraphy

Giant Random Telegraph Signals in Nanoscale Floating-Gate Devices. *Fantini, P.*, +, *EDL Dec. 2007 1114-1116*

Temperature

Effects of Measurement Temperature on NBTI. *Zhang, J. F.*, +, *EDL April 2007 298-300*

Temperature dependence

Solution-Processed n-Type Organic Field-Effect Transistors With High ON/OFF Current Ratios Based on Fullerene Derivatives. *Tiwari, S. P.*, +, *EDL Oct. 2007 880-883*

Temperature measurement

Time-Resolved Temperature Measurement of AlGaIn/GaN Electronic Devices Using Micro-Raman Spectroscopy. *Kuball, M.*, +, *EDL Feb. 2007 86-89*

Comparison of GaN HEMTs on Diamond and SiC Substrates. *Felbinger, J. G.*, +, *EDL Nov. 2007 948-950*

Effect of Load Distribution on the Voltage Drop and the Luminance Variation in an AC-PDP. *Kim, J.-S.*, +, *EDL Oct. 2007 896-898*

Impact of Preferential P-Diffusion Along the Grain Boundaries on Fine-Grained Polysilicon Solar Cells. *Carnel, L.*, +, *EDL Oct. 2007 899-901*

Low-Temperature Transport Characteristics and Quantum-Confinement Effects in Gate-All-Around Si-Nanowire N-MOSFET. *Rustagi, S. C.*, +, *EDL Oct. 2007 909-912*

Low-Temperature Passivation of Amorphous-Silicon Thin-Film Transistors With Supercritical Fluids. *Tsai, C.-T.*, +, *EDL July 2007 584-586*

Low-Temperature Transport Characteristics and Quantum-Confinement Effects in Gate-All-Around Si-Nanowire N-MOSFET. *Rustagi, S. C.*, +, *EDL Oct. 2007 909-912*

Temperature-Dependent Characteristics of Cylindrical Gate-All-Around Thin Silicon Nanowire MOSFETs (TSNWFETs). *Cho, K. H.*, +, *EDL Dec. 2007 1129-1131*

Tensile strain

The Origin of Electron Mobility Enhancement in Strained MOSFETs. *Hadjisavvas, G.*, +, *EDL Nov. 2007 1018-1020*

Impact of Local Strain From Selective Epitaxial Germanium With Thin Si/SiGe Buffer on High-Performance p-i-n Photodetectors With a Low Thermal Budget. *Loh, W. Y.*, +, *EDL Nov. 2007 984-986*

Tensile strength

Piezoresistance Coefficients of (100) Silicon nMOSFETs Measured at Low and High (~ 1.5 GPa) Channel Stress. *Suthram, S.*, +, *EDL Jan. 2007 58-61*

A Novel Strain Method for Enhancement of 90-nm Node and Beyond FUSI-Gated CMOS Performance. *Lin, C.-T.*, +, *EDL Feb. 2007 111-113*

Tensile-Strained Germanium CMOS Integration on Silicon. *Zang, H.*, +, *EDL Dec. 2007 1117-1119*

Terbium

Yttrium- and Terbium-Based Interlayer on SiO₂ and HfO₂ Gate Dielectrics for Work Function Modulation of Nickel Fully Silicided Gate in nMOSFET. *Lim, A. E.-J.*, +, *EDL June 2007 482-485*

Thermal conductivity

Enhanced Thermal Efficiency in Phase-Change Memory Cell by Double GST Thermally Confined Structure. *Chao, D.-S.*, +, *EDL Oct. 2007 871-873*

Thermal diffusion

Time-Resolved Temperature Measurement of AlGaIn/GaN Electronic Devices Using Micro-Raman Spectroscopy. *Kuball, M.*, +, *EDL Feb. 2007 86-89*

Thermal management (packaging)

Implementation of Side Effects in Thermal Characterization of RGB Full-Color EDLs. *Kim, L.*, +, *EDL July 2007 578-580*

Thermal resistance

Implementation of Side Effects in Thermal Characterization of RGB Full-Color EDLs. *Kim, L.*, +, *EDL July 2007 578-580*

Thermal stability

Arsenic Junction Thermal Stability and High-Dose Boron-Pocket Activation During SPER in nMOS Transistors. *Severi, S.*, +, *EDL March 2007 198-200*

A Reliability Model for Low-Temperature Polycrystalline Silicon Thin-Film Transistors. *Chen, C.-Y.*, +, *EDL May 2007 392-394*

Effect of SiN_x Gate Dielectric Deposition Power and Temperature on a-Si:H TFT Stability. *Kattamis, A. Z.*, +, *EDL July 2007 606-608*

Effects of Sulfur Passivation on Germanium MOS Capacitors With HfON Gate Dielectric. *Xie, R.*, +, *EDL Nov. 2007 976-979*

Nitrogen Incorporation in HfSiO(N)/Ta_n Gate Stacks: Impact on Performances and NBTI. *Aoulaiche, M.*, +, *EDL July 2007 613-615*

Thin film capacitors

High-Performance Metal-Insulator-Metal Capacitors Using Amorphous BaSm₂Ti₄O₁₂ Thin Film. *Jeong, Y. H.*, +, *EDL Jan. 2007 17-20*

Thin film circuits

A Novel LTPS-TFT Pixel Circuit Compensating for TFT Threshold-Voltage Shift and OEDL Degradation for AMOEDL. *Lin, C.-L.*, +, *EDL Feb. 2007 129-131*

Electrically Bistable Thin-Film Device Based on PVK and GNPs Polymer Material. *Song, Y.*, +, *EDL Feb. 2007 107-110*

Fast Thin-Film Transistor Circuits Based on Amorphous Oxide Semiconductor. *Ofuji, M.*, +, *EDL April 2007 273-275*

Thin film devices

Millimeter-Wave Bandpass Filters by Standard 0.18- μm CMOS Technology. *Sun, S.*, +, *EDL March 2007 220-222*

Room-Temperature Deposited Titanium Silicate Thin Films for MIM Capacitor Applications. *Brassard, D.*, +, *EDL April 2007 261-263*

Thin film inductors

Ferrite-Integrated On-Chip Inductors for RF ICs. *Yang, C.*, +, *EDL July 2007 652-655*

Thin film transistors

A Novel Four-Mask-Step Low-Temperature Polysilicon Thin-Film Transistor With Self-Aligned Raised Source/Drain (SARSD). *Chang, K. M.*, +, *EDL Jan. 2007 39-41*

A Novel LTPS-TFT Pixel Circuit Compensating for TFT Threshold-Voltage Shift and OEDL Degradation for AMOEDL. *Lin, C.-L.*, +, *EDL Feb. 2007 129-131*

A Novel Low-Temperature Polysilicon Thin-Film Transistors With a Self-Aligned Gate and Raised Source/Drain Formed by the Damascene Process. *Chang, K. M.*, +, *EDL Sept. 2007 806-808*

A Novel Nanowire Channel Poly-Si TFT Functioning as Transistor and Non-volatile SONOS Memory. *Chen, S.-C.*, +, *EDL Sept. 2007 809-811*

A Reliability Model for Low-Temperature Polycrystalline Silicon Thin-Film Transistors. *Chen, C.-Y.*, +, *EDL May 2007 392-394*

A Simple Spacer Technique to Fabricate Poly-Si TFTs With 50-nm Nanowire Channels. *Chang, C.-W.*, +, *EDL Nov. 2007 993-995*

A Simple and Effective Approach to Improve the Output Linearity of Switched-Current AMOEDL Pixel Circuitry. *Guo, X.*, +, *EDL Oct. 2007 887-889*

Active Pixel Concept Combined With Organic Photodiode for Imaging Devices. *Tedde, S.*, +, *EDL Oct. 2007 893-895*

Amorphous-Silicon Thin-Film Transistors Fabricated at 300 °C on a Free-Standing Foil Substrate of Clear Plastic. *Cherenack, K. H.*, +, *EDL Nov. 2007 1004-1006*

Constant Bias Stress Effects on Threshold Voltage of Pentacene Thin-Film Transistors Employing Polyvinylphenol Gate Dielectric. *Kim, T. H.*, +, *EDL Oct. 2007 874-876*

Crystallization of Double-Layered Silicon Thin Films by Solid Green Laser Annealing for High-Performance Thin-Film Transistors. *Sugawara, Y.*, +, *EDL May 2007 395-397*

Current-Voltage Characteristics of Long-Channel Nanobundle Thin-Film Transistors: A "Bottom-Up" Perspective. *Pimparkar, N.*, +, *EDL Feb. 2007 157-160*

Defect Passivation by Selenium-Ion Implantation for Poly-Si Thin Film Transistors. *Lai, J.*, +, *EDL Aug. 2007 725-727*

Degradation of Laser-Crystallized Laterally Grown Poly-Si TFT under Dynamic Stress. *Liu, P.-T.*, +, *EDL May 2007 401-403*

Effect of SiN_x Gate Dielectric Deposition Power and Temperature on a-Si:H TFT Stability. *Kattamis, A. Z.*, +, *EDL July 2007 606-608*

Embedded TFT NAND-Type Nonvolatile Memory in Panel. *Chen, H.-T.*, +, *EDL June 2007 499-501*

Fast Thin-Film Transistor Circuits Based on Amorphous Oxide Semiconductor. *Ofuji, M.*, +, *EDL April 2007 273-275*

Flexible Full-Color AMOEDL on Ultrathin Metal Foil. *Jeong, J. K.*, +, *EDL May 2007 389-391*

HgTe Nanocrystal-Based Thin-Film Transistors Fabricated on Glass Substrates. *Kim, H.*, +, *EDL Jan. 2007 42-44*

High-Performance Polycrystalline-Silicon TFT by Heat-Retaining Enhanced Lateral Crystallization. *Liu, P.-T.*, +, *EDL Aug. 2007 722-724*

High-Performance Self-Aligned Bottom-Gate Low-Temperature Poly-Silicon Thin-Film Transistors With Excimer Laser Crystallization. *Tsai, C.-C.*, +, *EDL July 2007 599-602*

High-Performance Short-Channel Double-Gate Low-Temperature Polysilicon Thin-Film Transistors Using Excimer Laser Crystallization. *Tsai, C.-C.*, +, *EDL Nov. 2007 1010-1013*

High-Performance and Low-Temperature-Compatible p-Channel Polycrystalline-Silicon TFTs Using Hafnium-Silicate Gate Dielectric. *Yang, M.-J.*, +, *EDL Oct. 2007 902-904*

Impact of Channel Dangling Bonds on Reliability Characteristics of Flash Memory on Poly-Si Thin Films. *Lin, Y.-H.*, +, *EDL April 2007 267-269*

Improved Electrical Characteristics and Reliability of MILC Poly-Si TFTs Using Fluorine-Ion Implantation. *Chang, C.-P.*, +, *EDL Nov. 2007 990-992*

Improved Stability of High-Performance ZnO/ZnMgO Hetero-MISFETs. *Sasa, S.*, +, *EDL July 2007 543-545*

Improving the Electrical Properties of NILC Poly-Si Films Using a Gettering Substrate. *Hu, C.-M.*, +, *EDL Nov. 2007 1000-1003*

Limits of Performance Gain of Aligned CNT Over Randomized Network: Theoretical Predictions and Experimental Validation. *Pimparkar, N.*, +, *EDL July 2007 593-595*

Low-Temperature Passivation of Amorphous-Silicon Thin-Film Transistors With Supercritical Fluids. *Tsai, C.-T.*, +, *EDL July 2007 584-586*

Numerical Simulation of Low-Frequency Noise in Polysilicon Thin-Film Transistors. *Pichon, L.*, +, *EDL Aug. 2007 716-718*

Observation of Threshold-Voltage Instability in Single-Crystal Silicon TFTs on Flexible Plastic Substrate. *Yuan, H.-C.*, +, *EDL July 2007 590-592*

On-Pixel Voltage-Control EDL Oscillator in Amorphous-Silicon Technology for Digital Imaging Applications. *Sanaie, G.*, +, *EDL Jan. 2007 33-35*

Passivation Effects of Aluminum on Polycrystalline Silicon Thin-Film Transistor With Metal-Replaced Junctions. *Zhang, D.*, +, *EDL Feb. 2007 126-128*

Performance Improvement of Organic Thin-Film Transistors by Electrode/Pentacene Interface Treatment Using a Hydrogen Plasma. *Lee, J.-W.*, +, *EDL May 2007 379-382*

Solution-Processed TIPS-Pentacene Organic Thin-Film-Transistor Circuits. *Park, S. K.*, +, *EDL Oct. 2007 877-879*

Stability of Amorphous-Silicon and Nanocrystalline Silicon Thin-Film Transistors Under DC and AC Stress. *Hatzopoulos, A. T.*, +, *EDL Sept. 2007 803-805*

Thin films

Electrical Compensation of OEDL Luminance Degradation. *Chaji, G. R.*, +, *EDL Dec. 2007 1108-1110*

Field-Controllable Flexible Strain Sensors Using Pentacene Semiconductors. *Ji, T.*, +, *EDL Dec. 2007 1105-1107*

Threshold voltage

Low-Temperature Passivation of Amorphous-Silicon Thin-Film Transistors With Supercritical Fluids. *Tsai, C.-T.*, +, *EDL July 2007 584-586*

Anomalous Cells With Low Reset Resistance in Phase-Change-Memory Arrays. *Mantegazza, D.*, +, *EDL Oct. 2007 865-867*

Constant Bias Stress Effects on Threshold Voltage of Pentacene Thin-Film Transistors Employing Polyvinylphenol Gate Dielectric. *Kim, T. H.*, +, *EDL Oct. 2007 874-876*

Experimental Evaluation of Effects of Channel Doping on Characteristics of FinFETs. *Endo, K.*, +, *EDL Dec. 2007 1123-1125*

Monolithically Integrated Logic NOR Gate Based on GaAs/AlGaAs Three-Terminal Junctions. *Muller, C. R.*, +, *EDL Oct. 2007 859-861*

Time-domain reflectometry

Time-Domain-Reflectometry for Capacitance-Voltage Measurement With Very High Leakage Current. *Wang, Y.*, +, *EDL Jan. 2007 51-53*

Accurate Series-Resistance Extraction From Capacitor Using Time Domain Reflectometry. *Wang, Y.*, +, *EDL April 2007 279-281*

Error and Correction in Capacitance-Voltage Measurement Due to the Presence of Source and Drain. *Wang, Y.*, +, *EDL July 2007 640-642*

Tin

Reduction of Threshold Voltage by Diffusion Control Technique in p-MIS-FETs Using Poly-Si/TiN/HfSiON Gate Stacks. *Kawahara, T.*, +, *EDL Oct. 2007 868-870*

Tin compounds

Observation of Threshold-Voltage Instability in Single-Crystal Silicon TFTs on Flexible Plastic Substrate. *Yuan, H.-C.*, +, *EDL July 2007 590-592*

Good High-Temperature Stability of TiN/Al₂O₃/WN/TiN Capacitors. *Pan, T.-M.*, +, *EDL Nov. 2007 954-956*

Titanium

Effect of Top Electrode Material on Resistive Switching Properties of ZrO₂ Film Memory Devices. *Lin, C.-Y.*, +, *EDL May 2007 366-368*

Titanium alloys

Effect of Gate Sinking on the Device Performance of the InGaP/AlGaAs/InGaAs Enhancement-Mode PHEMT. *Chu, L. H.*, +, *EDL Feb. 2007 82-85*

Titanium compounds

High- κ Al₂O₃-HfTiO Nanolaminates With Less Than 0.8-nm Equivalent Oxide Thickness. *Mikhelashvili, V.*, +, *EDL Jan. 2007 24-26*

Achieving Conduction Band-Edge Effective Work Functions by La₂O₃ Capping of Hafnium Silicates. *Ragnarsson, L.-A.*, +, *EDL June 2007 486-488*

Cointegration of High-Performance Tied-Gate Three-Terminal FinFETs and Variable Threshold-Voltage Independent-Gate Four-Terminal FinFETs With Asymmetric Gate-Oxide Thicknesses. *Liu, Y.*, +, *EDL June 2007 517-519*

High Mobility Strained Ge pMOSFETs With High- κ /Metal Gate. *Nicholas, G.*, +, *EDL Sept. 2007 825-827*

Low-Frequency Noise Assessment of Silicon Passivated Ge pMOSFETs With TiN/TaN/HfO₂ Gate Stack. *Guo, W.*, +, *EDL April 2007 288-291*
 Room-Temperature Deposited Titanium Silicate Thin Films for MIM Capacitor Applications. *Brassard, D.*, +, *EDL April 2007 261-263*
 The Preparation of Nanocrystalline Silicon by Plasma-Enhanced Hydrogenation for the Fabrication of Light-Emitting Diodes. *Jamei, M.*, +, *EDL March 2007 207-210*

Transconductance

Improved Stability of High-Performance ZnO/ZnMgO Hetero-MISFETs. *Sasa, S.*, +, *EDL July 2007 543-545*
 Submicrometer Inversion-Type Enhancement-Mode InGaAs MOSFET With Atomic-Layer-Deposited Al₂O₃ as Gate Dielectric. *Xuan, Y.*, +, *EDL Nov. 2007 935-938*

Transient analysis

Study of the Erase Mechanism of MANOS (Metal/Al₂O₃/SiN/SiO₂/Si) Device. *Lai, S.*, +, *EDL July 2007 643-645*

Transistors

Strained n-Channel Transistors With Silicon Source and Drain Regions and Embedded Silicon/Germanium as Strain-Transfer Structure. *Ang, K.-W.*, +, *EDL July 2007 609-612*
 OFF-State Avalanche-Breakdown-Induced ON-Resistance Degradation in Lateral DMOS Transistors. *Chen, J. F.*, +, *EDL Nov. 2007 1033-1035*
 n⁺/p⁺ Gate Bulk FinFETs With Locally Separated Channel Structure for Sub-50-nm DRAM Cell Transistors. *Jung, H.-A.-R.*, +, *EDL Dec. 2007 1126-1128*
 CMOS Inverter Based on Gate-All-Around Silicon-Nanowire MOSFETs Fabricated Using Top-Down Approach. *Rustagi, S. C.*, +, *EDL Nov. 2007 1021-1024*
 Electrical Compensation of OEDL Luminance Degradation. *Chaji, G. R.*, +, *EDL Dec. 2007 1108-1110*
 Enhanced Hole Mobility and Reliability of Panel Epi-Like Silicon Transistors Using Backside Green Laser Activation. *Lin, Y.-T.*, +, *EDL Sept. 2007 790-792*
 Field-Controllable Flexible Strain Sensors Using Pentacene Semiconductors. *Ji, T.*, +, *EDL Dec. 2007 1105-1107*
 High-Current-Gain InP/GaInP/GaAsSb/InP DHBTs With $f_T = 436$ GHz. *Liu, H. G.*, +, *EDL Oct. 2007 852-855*
 Hot-Carrier Effects in Strained n-Channel Transistor With Silicon-Carbon (Si_{1-y}C_y) Source/Drain Stressors and Its Orientation Dependence. *Ang, K.-W.*, +, *EDL Nov. 2007 996-999*
 Metal-Oxide-High- κ Dielectric-Oxide-Semiconductor (MOHOS) Capacitors and Field-Effect Transistors for Memory Applications. *Hsu, H.*, +, *EDL Nov. 2007 964-966*
 Monolithically Integrated Logic NOR Gate Based on GaAs/AlGaAs Three-Terminal Junctions. *Muller, C. R.*, +, *EDL Oct. 2007 859-861*
 On the Apparent Mobility in Nanometric n-MOSFETs. *Zilli, M.*, +, *EDL Nov. 2007 1036-1039*
 On the Origin of the Excess Low-Frequency Noise in Graded-Channel Silicon-on-Insulator nMOSFETs. *Simoen, E.*, +, *EDL Oct. 2007 919-921*
 Solution-Processed n-Type Organic Field-Effect Transistors With High ON/OFF Current Ratios Based on Fullerene Derivatives. *Tiwari, S. P.*, +, *EDL Oct. 2007 880-883*
 Trigate FET Device Characteristics Improvement Using a Hydrogen Anneal Process With a Novel Hard Mask Approach. *Zaman, R. J.*, +, *EDL Oct. 2007 916-918*

Transmission electron microscopy

A Novel Strain Method for Enhancement of 90-nm Node and Beyond FUSI-Gated CMOS Performance. *Lin, C.-T.*, +, *EDL Feb. 2007 111-113*
 Electron Transport in Strained-Silicon Directly on Insulator Ultrathin-Body n-MOSFETs With Body Thickness Ranging From 2 to 25 nm. *Gomez, L.*, +, *EDL April 2007 285-287*
 Metamorphic Heterostructure InP/GaAsSb/InP HBTs on GaAs Substrates by MOCVD. *Zhou, W.*, +, *EDL July 2007 539-542*
 The Preparation of Nanocrystalline Silicon by Plasma-Enhanced Hydrogenation for the Fabrication of Light-Emitting Diodes. *Jamei, M.*, +, *EDL March 2007 207-210*

Trigger circuits

An Unassisted, Low Trigger-, and High Holding-Voltage SCR (uSCR) for On-Chip ESD-Protection Applications. *Lou, L.*, +, *EDL Dec. 2007 1120-1122*

Triodes

Carbon Nanotube-Based Triode Field Emission Lamps Using Metal Meshes With Spacers. *Cho, W.-S.*, +, *EDL May 2007 386-388*

An Improved Planar Triode With ZnO Nanopin Field Emitters. *Wei, L.*, +, *EDL Aug. 2007 688-690*

Tungsten compounds

Improved Ge Surface Passivation With Ultrathin SiO_x Enabling High-Mobility Surface Channel pMOSFETs Featuring a HfSiO/WN Gate Stack. *Joshi, S.*, +, *EDL April 2007 308-311*

Tuning

Schottky-Barrier Height Tuning by Means of Ion Implantation Into Preformed Silicide Films Followed by Drive-In Anneal. *Zhang, Z.*, +, *EDL July 2007 565-568*

Tunnel diodes

Temperature Dependence of High Frequency and Noise Performance of Sb-Heterostructure Millimeter-Wave Detectors. *Su, N.*, +, *EDL May 2007 336-339*
 Transport Mechanism of SiGe Dot MOS Tunneling Diodes. *Kuo, P.-S.*, +, *EDL July 2007 596-598*

Tunnel transistors

Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec. *Choi, W. Y.*, +, *EDL Aug. 2007 743-745*

Tunnelling

The Effects of the Injection-Channel Velocity on the Gate Leakage Current of Nanoscale MOSFETs. *Mao, L.*, *EDL Feb. 2007 161-163*
 Correction to "Revision of Tunneling Field-Effect Transistor in Standard CMOS Technologies". *Nirschl, Th.*, +, *EDL April 2007 315-315*
 Detection of Border Trap Density and Energy Distribution Along the Gate Dielectric Bulk of High- κ Gated MOS Devices. *Lu, C.-Y.*, +, *EDL May 2007 432-435*
 Measurement of Channel Stress Using Gate Direct Tunneling Current in Uniaxially Stressed nMOSFETs. *Hsieh, C.-Y.*, +, *EDL Sept. 2007 818-820*
 Study of the Erase Mechanism of MANOS (Metal/Al₂O₃/SiN/SiO₂/Si) Device. *Lai, S.*, +, *EDL July 2007 643-645*
 The Effect of Trapped Charge Distributions on Data Retention Characteristics of NAND Flash Memory Cells. *Park, M.*, +, *EDL Aug. 2007 750-752*
 The Preparation of Nanocrystalline Silicon by Plasma-Enhanced Hydrogenation for the Fabrication of Light-Emitting Diodes. *Jamei, M.*, +, *EDL March 2007 207-210*

U

UHF bipolar transistors

Demonstration of Long-Pulse Power Amplification at 1 GHz Using 4H-SiC RF BJTs on a Conductive Substrate. *Zhao, F.*, +, *EDL May 2007 398-400*

UHF integrated circuits

Symmetric Vertical Parallel Plate Capacitors for On-Chip RF Circuits in 65-nm SOI Technology. *Kim, D.*, +, *EDL July 2007 616-618*
 High-Q Integrated Inductor Using Post-CMOS Selectively Grown Porous Silicon (SGPS) Technique for RFIC Applications. *Li, C.*, +, *EDL Aug. 2007 763-766*

Ultraviolet lithography

Fabrication of 0.15- μ m Γ -Shaped Gate In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As Metamorphic HEMTs Using DUV Lithography and Tilt Dry-Etching Technique. *Lien, Y.-C.*, +, *EDL Feb. 2007 93-95*

V

VLSI

On the Control of Short-Channel Effect for MOSFETs With Reverse Halo Implantation. *Zhu, H.*, +, *EDL Feb. 2007 168-170*

Valence bands

Valence Band Offset Measurements on Thin Silicon-on-Insulator MOSFETs. *van der Steen, J.-L. P. J.*, +, *EDL Sept. 2007 821-824*

Varactors

A 0.2-W Heterostructure Barrier Varactor Frequency Tripler at 113 GHz. *Vukusic, J.*, +, *EDL May 2007 340-342*

Vertical cavity surface emitting lasers

GaN-Based High-Q Vertical-Cavity Light-Emitting Diodes. *Lu, T.-C.*, +, *EDL Oct. 2007 884-886*

Voltage control

Demonstration of Asymmetric Gate-Oxide Thickness Four-Terminal FinFETs Having Flexible Threshold Voltage and Good Subthreshold Slope. *Masahara, M.*, +, *EDL March 2007 217-219*

An Unassisted, Low Trigger-, and High Holding-Voltage SCR (uSCR) for On-Chip ESD-Protection Applications. *Lou, L.*, +, *EDL Dec. 2007 1120-1122*

Experimental Evaluation of Effects of Channel Doping on Characteristics of FinFETs. *Endo, K.*, +, *EDL Dec. 2007 1123-1125*

High-Gain Low Turn-On Voltage AlGaAs/GaAsNSb/GaAs Heterojunction Bipolar Transistors Grown by Molecular Beam Epitaxy. *Lew, K. L.*, +, *EDL Dec. 2007 1083-1085*

Voltage measurement

A High Schottky-Barrier of 1.1 eV Between Al and S-Passivated p-Type Si(100) Surface. *Song, G.*, +, *EDL Jan. 2007 71-73*

Accurate Series-Resistance Extraction From Capacitor Using Time Domain Reflectometry. *Wang, Y.*, +, *EDL April 2007 279-281*

Effect of Load Distribution on the Voltage Drop and the Luminance Variation in an AC-PDP. *Kim, J.-S.*, +, *EDL Oct. 2007 896-898*

Extraction of the Threshold-Voltage Shift by the Single-Pulse Technique. *Heh, D.*, +, *EDL Aug. 2007 734-736*

Metal-Oxide-High- κ Dielectric-Oxide-Semiconductor (MOHOS) Capacitors and Field-Effect Transistors for Memory Applications. *Hsu, H.*, +, *EDL Nov. 2007 964-966*

On the Origin of the Excess Low-Frequency Noise in Graded-Channel Silicon-on-Insulator nMOSFETs. *Simoen, E.*, +, *EDL Oct. 2007 919-921*

Time-Domain-Reflectometry for Capacitance-Voltage Measurement With Very High Leakage Current. *Wang, Y.*, +, *EDL Jan. 2007 51-53*

Voltage-control EDL oscillators

On-Pixel Voltage-Control EDL Oscillator in Amorphous-Silicon Technology for Digital Imaging Applications. *Sanaie, G.*, +, *EDL Jan. 2007 33-35*

Volterra series

A New Method for Identification and Minimization of Distortion Sources in GaN HEMT Devices Based on Volterra Series Analysis. *Srinidhi, E. R.*, +, *EDL May 2007 343-345*

W

Wafer bonding

DC Characteristics of AlGaAs/GaAs/GaN HBTs Formed by Direct Wafer Fusion. *Lian, C.*, +, *EDL Jan. 2007 8-10*

Low-Temperature Polymer-Based Three-Dimensional Silicon Integration. *Kim, S.*, +, *EDL Aug. 2007 706-709*

Wide band gap semiconductors

Power Stability of AlGaIn/GaN HFETs at 20 W/mm in the Pinched-Off Operation Mode. *Koudymov, A.*, +, *EDL Jan. 2007 5-7*

1- μ m Enhancement Mode GaAs N-Channel MOSFETs With Transconductance Exceeding 250 mS/mm. *Rajagopalan, K.*, +, *EDL Feb. 2007 100-102*

1.3- μ m GaInAsN Vertical-Cavity Surface-Emitting Lasers by Oxide-Planarized and Surface-Relief Processes for Single-Mode Operation. *Lee, F.-M.*, +, *EDL Feb. 2007 120-122*

1000-V 9.1-m Ω · cm² Normally Off 4H-SiC Lateral RESURF JFET for Power Integrated Circuit Applications. *Zhang, Y.*, +, *EDL May 2007 404-407*

A New Method for Identification and Minimization of Distortion Sources in GaN HEMT Devices Based on Volterra Series Analysis. *Srinidhi, E. R.*, +, *EDL May 2007 343-345*

A Novel Dilute Antimony Channel In_{0.2}Ga_{0.8}AsSb/GaAs HEMT. *Su, K.-H.*, +, *EDL Feb. 2007 96-99*

AlGaN Photodetectors Prepared on Si Substrates. *Chiou, Y. Z.*, +, *EDL April 2007 264-266*

AlGaIn/GaN HEMTs With Thin InGaIn Cap Layer for Normally Off Operation. *Mizutani, T.*, +, *EDL July 2007 549-551*

Amorphous-SiC_{BN}-Based Metal-Semiconductor-Metal Photodetector for High-Temperature Applications. *Vijayakumar, A.*, +, *EDL Aug. 2007 713-715*

Compact Model of Current Collapse in Heterostructure Field-Effect Transistors. *Koudymov, A.*, +, *EDL May 2007 332-335*

DC Characteristics of AlGaAs/GaAs/GaN HBTs Formed by Direct Wafer Fusion. *Lian, C.*, +, *EDL Jan. 2007 8-10*

Demonstration of Long-Pulse Power Amplification at 1 GHz Using 4H-SiC RF BJTs on a Conductive Substrate. *Zhao, F.*, +, *EDL May 2007 398-400*

Enhanced Strain Effects in 25-nm Gate-Length Thin-Body nMOSFETs With Silicon-Carbon Source/Drain and Tensile-Stress Liner. *Ang, K.-W.*, +, *EDL April 2007 301-304*

Fabrication of 0.15- μ m Γ -Shaped Gate In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As Metamorphic HEMTs Using DUV Lithography and Tilt Dry-Etching Technique. *Lien, Y.-C.*, +, *EDL Feb. 2007 93-95*

High-Temperature Operation of AlGaIn/GaN HEMTs Direct-Coupled EDL FET Logic (DCFL) Integrated Circuits. *Cai, Y.*, +, *EDL May 2007 328-331*

High-Voltage Self-Aligned p-Channel DMOS-IGBTs in 4H-SiC. *Sui, Y.*, +, *EDL Aug. 2007 728-730*

Hot-Phonon Effect on the Electrothermal Behavior of Submicrometer III-V HEMTs. *Sadi, T.*, +, *EDL Sept. 2007 787-789*

Impact of CF₄ Plasma Treatment on GaN. *Chu, R.*, +, *EDL Sept. 2007 781-783*

Improved Reliability and ESD Characteristics of Flip-Chip GaN-Based EDLs With Internal Inverse-Parallel Protection Diodes. *Shei, S.-C.*, +, *EDL May 2007 346-349*

ON-Resistance Modulation of High Voltage GaN HEMT on Sapphire Substrate Under High Applied Voltage. *Saito, W.*, +, *EDL Aug. 2007 676-678*

RF Power Measurements of InAlN/GaN Unstrained HEMTs on SiC Substrates at 10 GHz. *Jessen, G. H.*, +, *EDL May 2007 354-356*

RF-Enhanced Contacts to Wide-Bandgap Devices. *Simin, G.*, +, *EDL Jan. 2007 2-4*

Silicon Dioxide-Encapsulated High-Voltage AlGaIn/GaN HFETs for Power-Switching Applications. *Tipirneni, N.*, +, *EDL Sept. 2007 784-786*

Submicrometer Copper T-Gate AlGaIn/GaN HFETs: The Gate Metal Stack Effect. *Sun, H. F.*, +, *EDL May 2007 350-353*

Time-Resolved Temperature Measurement of AlGaIn/GaN Electronic Devices Using Micro-Raman Spectroscopy. *Kuball, M.*, +, *EDL Feb. 2007 86-89*

Wireless sensor networks

High-Quality Factor Electrolyte Insulator Silicon Capacitor for Wireless Chemical Sensing. *Garcia-Canton, J.*, +, *EDL Jan. 2007 27-29*

Wires

CMOS Inverter Based on Gate-All-Around Silicon-Nanowire MOSFETs Fabricated Using Top-Down Approach. *Rustagi, S. C.*, +, *EDL Nov. 2007 1021-1024*

Work function

Fermi-Level Pinning in Nanocrystal Memories. *Hou, T.-H.*, +, *EDL Feb. 2007 103-106*

Achieving Conduction Band-Edge Effective Work Functions by La₂O₃ Capping of Hafnium Silicates. *Ragnarsson, L.-A.*, +, *EDL June 2007 486-488*

CMOS Dual-Work-Function Engineering by Using Implanted Ni-FUSI. *Lin, C.-T.*, +, *EDL Sept. 2007 831-833*

Characteristics of Ni/Gd FUSI for NMOS Gate Electrode Applications. *Lee, B.*, +, *EDL July 2007 555-557*

Gate Workfunction Engineering in Bulk FinFETs for Sub-50-nm DRAM Cell Transistors. *Park, K.-H.*, +, *EDL Feb. 2007 148-150*

High-Temperature Stable HfLaON p-MOSFETs With High-Work-Function Ir₃Si Gate. *Wu, C. H.*, +, *EDL April 2007 292-294*

Novel Single Polysilicon EEPROM Cell With Dual Work Function Floating Gate. *Na, K.-Y.*, +, *EDL Feb. 2007 151-153*

X

X-ray diffraction

A Novel Strain Method for Enhancement of 90-nm Node and Beyond FUSI-Gated CMOS Performance. *Lin, C.-T.*, +, *EDL Feb. 2007 111-113*

Metamorphic Heterostructure InP/GaAsSb/InP HBTs on GaAs Substrates by MOCVD. *Zhou, W.*, +, *EDL July 2007 539-542*

X-ray imaging

On-Pixel Voltage-Control EDL Oscillator in Amorphous-Silicon Technology for Digital Imaging Applications. *Sanaie, G.*, +, *EDL Jan. 2007 33-35*

X-ray photoelectron spectra

Effect of F₂ Postmetallization Annealing on the Electrical and Reliability Characteristics of HfSiO Gate Dielectric. *Chang, M.*, +, *EDL Jan. 2007 21-23*

Y

Yagi antenna arrays

100-GHz Quasi-Yagi Antenna in Silicon Technology. *Sun, M.*, +, *EDL May 2007 455-457*

Ytterbium

CMOS Dual-Work-Function Engineering by Using Implanted Ni-FUSI. *Lin, C.-T.*, +, *EDL Sept. 2007* 831-833

Ytterbium compounds

N-channel FinFETs With 25-nm Gate Length and Schottky-Barrier Source and Drain Featuring Ytterbium Silicide. *Lee, R. T. P.*, +, *EDL Feb. 2007* 164-167

Yttrium

Yttrium- and Terbium-Based Interlayer on SiO₂ and HfO₂ Gate Dielectrics for Work Function Modulation of Nickel Fully Silicided Gate in nMOSFET. *Lim, A. E.-J.*, +, *EDL June 2007* 482-485

Yttrium compounds

Ferrite-Integrated On-Chip Inductors for RF ICs. *Yang, C.*, +, *EDL July 2007* 652-655

Z**Zinc**

Improved Stability of High-Performance ZnO/ZnMgO Hetero-MISFETs. *Sasa, S.*, +, *EDL July 2007* 543-545

Zinc alloys

Resistive Switching Mechanism in Zn_xCd_{1-x}S Nonvolatile Memory Devices. *Wang, Z.*, +, *EDL Jan. 2007* 14-16

Zinc compounds

An Improved Planar Triode With ZnO Nanopin Field Emitters. *Wei, L.*, +, *EDL Aug. 2007* 688-690

Zirconium compounds

Electrical Characterization of ZrO₂/Si Interface Properties in MOSFETs With ZrO₂ Gate Dielectrics. *Liu, C.-H.*, +, *EDL Jan. 2007* 62-64

Effect of Top Electrode Material on Resistive Switching Properties of ZrO₂ Film Memory Devices. *Lin, C.-Y.*, +, *EDL May 2007* 366-368