Comments and Corrections

Correction to "Revision of Tunneling Field-Effect Transistor in Standard CMOS Technologies"

Th. Nirschl, M. Weis, M. Fulde, and D. Schmitt-Landsiedel

Previously published results [1]–[6] on the tunneling field-effect transistor (TFET) are revised in this correction. The devices that we had characterized as TFETs contain a conducting path in parallel to the intended tunneling junction. Therefore, the measured characteristics are similar to a MOSFET with a resistive source connection.

The cross section of the TFET (see Fig. 1) is similar to a gated pin diode (see, e.g., [7]). With a positive gate bias, the TFET is operated as an n-channel device. For strong inversion, a tunneling junction is formed between the n-channel and the p+ doped source. The width of the tunneling barrier is modulated by the gate bias.

In [1]–[6], we have published results of TFETs fabricated in industrial 130-, 90-, and 65-nm CMOS processes without modifications, where current values increased with each technology node. In this correction, we want to retract the faulty and misleading statements given in [1]–[6].

To produce a TFET, the source implant has to be reversed with respect to the corresponding MOSFET device. For this purpose, we used the design layer provided to define substrate/well contacts. It was drawn overlapping the source and part of the gate area. Unfortunately, we did not recognize that the used design layer affected only the highly doped drain (HDD) implant of the source/drain regions. The lightly doped drain (LDD) implant, however, was not reversed. By inspection of the actual masks used in our TFET test structures, we have made sure that this was the case for the 130-, 90-, and 65-nm test chips [1]–[6]. The cross section of the actually fabricated device is shown in Fig. 2. The LDD implant resulted in a shallow n-doped region in the upper part of the p-doped HDD implant region, constituting an electron-conducting path. Process simulation was performed using TSUPREM4 and proved that the n+ doping exceeds the p+ concentration near the surface, as shown in Fig. 3. Hence, the device shows the standard MOSFET behavior with an additional series resistance. The additional series resistance decreases for scaled technologies. The 130-nm device (schematic cross section, see Fig. 2) showed a rather low current of some microamperes per micrometer, comparable to the previously published TFET values, while the 65-nm device (schematic cross section, see Fig. 2) showed characteristics very similar to the corresponding MOSFET with currents above 100 $\mu\mathrm{A}/\mu\mathrm{m}$.

The authors involved in the erroneous publications (Nirschl and Schmitt-Landsiedel), also in the name of all coauthors of those publications, would like to express their sincere regrets for spreading the misleading information. They would like to thank M. Fulde and M. Weis for their valuable work in clarifying the true facts. All authors would like to thank P. Kuepper for the support by device simulation.

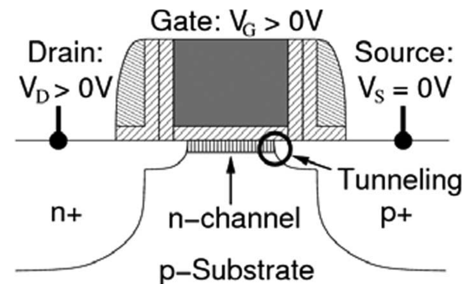

Fig. 1. Basic structure of TFET.

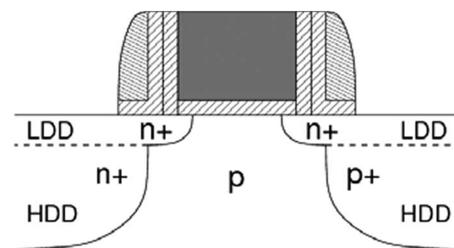

Fig. 2. Cross section of fabricated device.

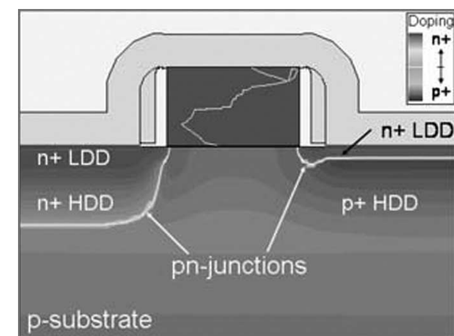

Fig. 3. Process simulation with TSUPREM4.

REFERENCES

[1] Th. Nirschl *et al.*, "The tunneling field effect transistor (TFET) as an add-on for ultra-low-voltage analog and digital processes," in *IEDM Tech. Dig.*, 2004, pp. 195–198.

[2] ——, "The tunneling field effect transistor (TFET) used in a single-event-upset (SEU) insensitive 6 transistor SRAM cell in ultra-low voltage applications," in *Proc. IEEE Conf. Nanotechnol.*, Munich, Germany, 2004, pp. 402–404.

[3] ——, "Impact of mask alignment on the tunneling field effect transistor (TFET)," in *Proc. ICMTS*, 2005, pp. 43–46.

[4] ——, "Scaling down the tunneling field effect transistor (TFET) from the 130 nm to the 65 nm CMOS process flow," in *Proc. Workshop ULIS*, 2005.

[5] ——, "The 65 nm tunneling field effect transistor (TFET) 0.68 $\mu\mathrm{m}^2$ 6T memory cell and multi-Vth device," in *Proc. 35th ESSDERC*, 2005, pp. 173–176.

[6] ——, "Scaling properties of the tunneling field effect transistor (TFET): Device and circuit," *Solid State Electron.*, vol. 50, no. 1, pp. 44–51, Jan. 2006.

[7] P.-F. Wang *et al.*, "Complementary tunneling transistor for low power application," *Solid State Electron.*, vol. 48, no. 12, pp. 2281–2286, Dec. 2004.

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