Multilevel Vertical-Channel SONOS Nonvolatile Memory on SOI

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***Abstract*—A first multilevel vertical-channel silicon-oxide-nitride-oxide-silicon (MLVC-SONOS) memory cell is proposed and fabricated using 0.12-μm silicon-on-insulator (SOI) standard logic process for Flash memory cell with ultrahigh density. If NAND array structure is used, the unit cell size of MLVC-SONOS is $4F^2$. Further reduction of cell size is possible by using the multilevel concept which is originated from the steady states by two carrier transports from both the substrate and the gate. The program threshold voltages and their windows are uniform and controllable depending on the negative gate bias conditions. In addition, we propose a new endurance measurement method for multilevels and report the retention characteristics for multilevel memory operation.**

***Index Terms*—Multilevel (ML), negative program, positive program, silicon-on-insulator (SOI), silicon-oxide-nitride-oxide-silicon (SONOS), steady state, vertical-channel (VC).**

I. Introduction

We are facing a barrier in the shrinkage of floating-gate-type Flash memories into the sub-0.1-μm regime because it is hard to reduce unit cell area, spacing between neighboring memory cells, overlap margins for active regions and floating polysilicon, contact hole size, and source line. Advanced NAND-type Flash memories were proposed [1], [2] to overcome some of the difficulties and novel NAND Flash memory structures such as S-SGT were also proposed [3]. In the other direction, an asymmetrically programmed 2-bit silicon-oxide-nitride-oxide-silicon (SONOS), namely, NROM, was evolved to increase memory density [4], [5].

In this letter, we introduce two novel concepts in multilevel vertical-channel silicon-oxide-nitride-oxide-silicon (MLVC-SONOS) for memory density increase. The first is reducing active pitch by using vertical silicon channel on silicon-on-insulator (SOI), so that unit cell size can be reduced to $4F^2$ ($2F \times 2F$ in a NAND array structure). The second is a multilevel operation originated from the steady states by two carrier transports from both the substrate and the gate.

In terms of reliability, endurance and retention of MLVC-SONOS for multilevel are measured. For reasonable endurance stress, combination theory is adopted in the selection of stress mode sequence and retention characteristics are measured before and after the endurance stress.

Manuscript received June 21, 2001; revised August 26, 2002. The review of this letter was arranged by Editor S. Kawamura.

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Digital Object Identifier 10.1109/LED.2002.805001

II. Fabrication of the Memory Cell

Fig. 1 illustrates the key process flow and TEM images on MLVC-SONOS. The starting material is p-type (100) SOI wafer. The SOI layer on top of 25-nm thick buried oxide layer (BOX) was thinned to the thickness of 57 nm. Then, 100-nm thick LPCVD oxide is deposited to suppress the top channel current to the level of less than 0.01% of the vertical-channel (VC) current at the bias of 12 V. This thickness is decided by device simulation (MEDICI). As shown in Fig. 1(a), the active region is patterned with the conventional lithography and one step etch for CVD oxide and the crystalline silicon (c-Si). Next, oxide-nitride-oxide (ONO) layers are formed with 15 Å thermal oxide, 50 Å LPCVD nitride, and 40 Å LPCVD oxide consecutively. After deposition, RTA was done for LPCVD dielectric densification at 1000 °C in N_2 ambient. On top of this stack, 2000 Å polysilicon is deposited and patterned with the conventional lithography in the step of Fig. 1(b). The memory's gate length is about 0.15 μm. In Fig. 1(c), the thick CVD oxide ($\sim$ 100 nm) over source/drain (S/D) region is etched by using the polysilicon as a mask. After the oxide is removed, S/D junctions can be formed by S/D implantation on top and vertical active region at the same time. Therefore, a stable S/D vertical junction and connection between W-Si contact and S/D vertical junction is made. In Fig. 1(d), lightly doped drain (LDD) implantation, spacer formation, S/D implantation, and back-end metal processes are done with a standard Si process.

Fig. 1(e) shows the cross-sectional TEM micrograph along the word-line direction [y-direction in Fig. 1(d)] on monitoring patterns. Lateral dimensions are different from the actual device sizes. Two vertical channels were formed on the c-Si side edges. Fig. 1(f) is a TEM image along bit-line direction [x-direction in Fig. 1(d)].

III. Results and Discussion

Fig. 2 shows the single-level characteristics. Program and erase are done by a Fowler–Nordheim (FN) tunneling method by stressing the on gate while all other nodes are grounded. The threshold voltage was decided by reading the gate voltage at the drain current of 1 nA at 0.5 V drain bias. The drain current is low because of the VC roughness and the high S/D resistance due to no-silicidation and c-Si thinning during oxide overetch. Threshold voltage shifts in program and erase are 1.4 V and $|1.6|$ V at $+8$ V$/-8$ V bias and 3 ms each. For the erase voltage

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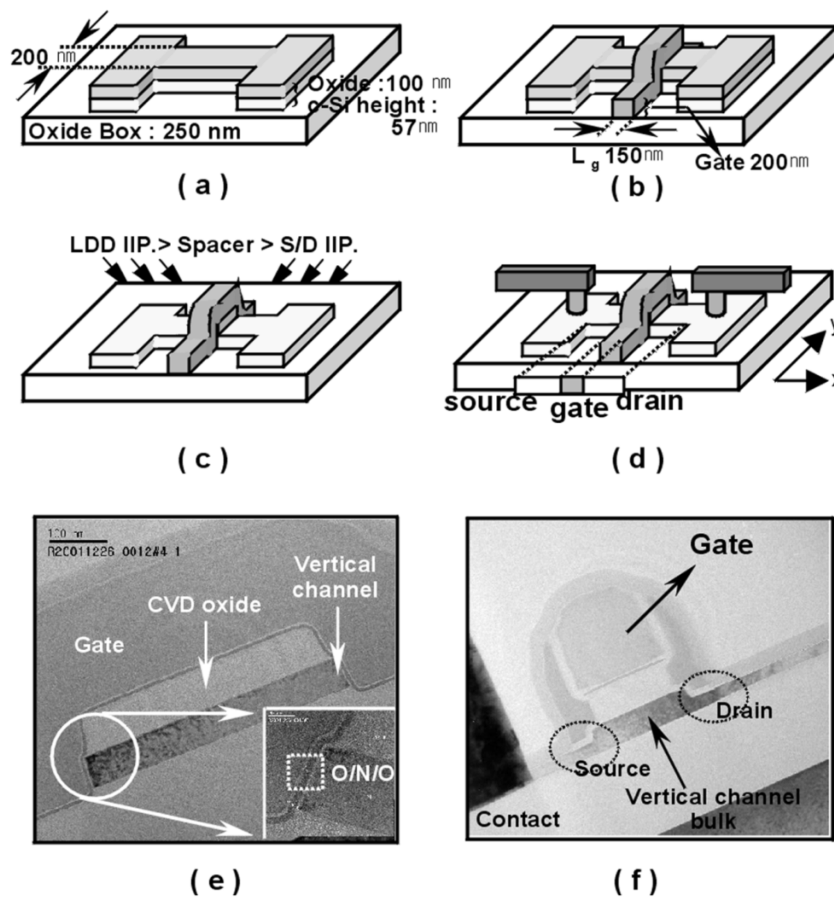

Fig. 1. (a)–(d) Key fabrication process flow of the MLVC-SONOS memory cell and (e) TEM images along the word-line direction. Two vertical channels are on both c-Si's edges and top-channel suppression CVD oxide and (f) image along the bit-line directions.

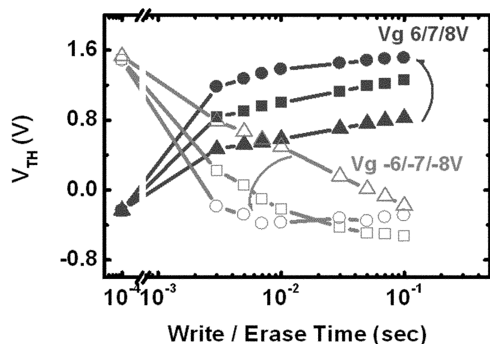

Fig. 2. Single-level operation characteristics with (a) positive bias program and (b) negative bias erase.

above $|-8|$ V, there is erase level saturation. This phenomenon is very useful in removing the over-erase problems in NOR-type Flash memory cells [6].

In the conventional SONOS memory, top oxide is considered only as a blocking oxide for carrier transport from the gate. However, in the range of highly scaled ONO thickness with the high field, we cannot exclude the carrier transport from the gate; and it used to be considered as a bad effect in erase mode. However, in terms of multilevel programming, this characteristic can be used to obtain stable multilevels.

Fig. 3(a) shows the comparison of the positive programming and negative programming. Negative programming maintains a steady state for a long time range. Generally speaking, there are always initial threshold voltage distributions and program speed distributions. If the same threshold voltage is maintained with time and the program time target is set in that range, the program speed distribution can be excluded and good program uniformity can be obtained. This characteristic is very useful for multilevel operation in high-density memories. Assuming that major carriers are the holes from the p-substrate and electrons from the n^+ gate, we have calculated FN tunneling current for electrons and direct tunneling current for holes. The electric field is calculated from electrical ONO thickness. Calculation results are summarized in Fig. 3(b) to explain the steady state and the threshold voltage increase as a function of the erase bias voltage above $|-8|$ V. Voltage difference between simulation and measured data comes from not considering the three-dimensional effect. In low-negative gate voltage, there is only hole current from the substrate. However, as the bias increases, electron current starts to flow from the gate and the slope is higher, so that a cross point appears. This balance generates a steady state. If the negative gate bias increases further, a new steady state can be generated by the threshold voltage increase ($A < B < C$), so that this change reduces the electric field for electrons from the gate and increases the electric field for holes from the substrate.

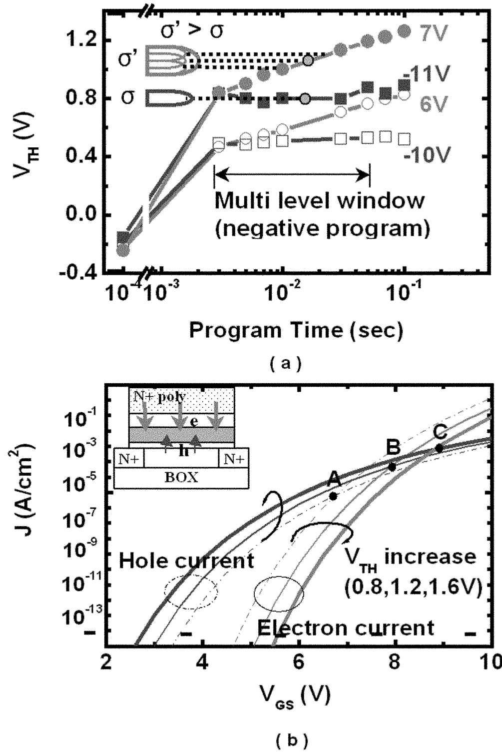

Fig. 3. Multilevel operation characteristics for MLVC-SONOS memory. (a) Comparison of the positive and negative programming. Negative programming has a long steady state. (b) Calculation summary for the explanation of the multilevel steady states and threshold voltage increase as negative gate bias increase.

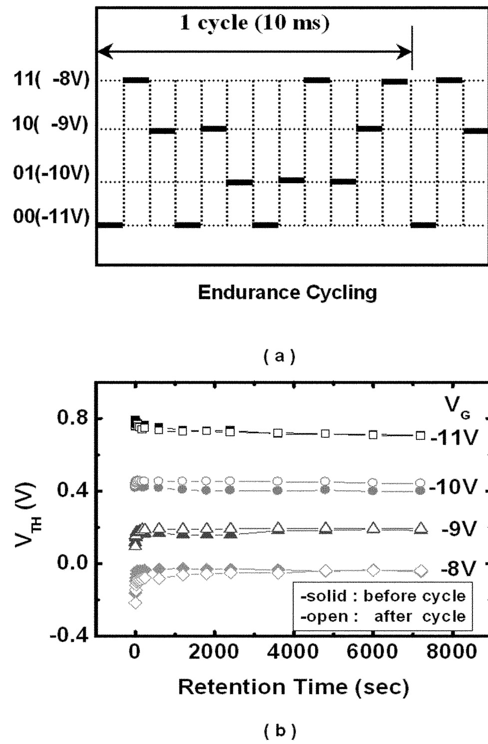

Fig. 4. Retention characteristics with multilevel states before and after endurance cycling. One endurance cycle is 10 ms and the total stress number is 100. For four levels, one endurance cycle is made up of 12 occasions, so that $(n+1)$th stress is different from the nth one and retention is measured until 7200 s.

Fig. 4 is the single cell's retention characteristics at room temperature for four levels before and after 100 endurance cycles. An endurance cycle is planned to make stress balancing among the four levels. Considering the fact that the conventional endurance cycle consists of one programming transition and one erasing transition, one complete endurance cycle shown in Fig. 4(b) is equivalent to six conventional cycles. From cycling fatigue and charge loss, the windows have narrowed from initial window from 0.3–0.4 V to 0.15–0.3 V after 7200 s. However, since the threshold voltages of steady state increase as negative program bias increases, their windows are changeable depending on the number of levels, we can tune the condition for stable multilevel operation. Programming disturbance is a concern in our structure, but we can minimize it by using a thicker SOI and programming voltage split between gate and S/D.

IV. Conclusions

We have fabricated 57-nm wide MLVC-SONOS memory cells with ONO 15/50/40 Å in physical thickness for the next-generation Flash memory. Active channels in MLVC-SONOS are on vertical c-Si, so that we can reduce the active pitch by the amount of lateral active width. In addition, the multilevel based on steady state with two carrier transports in negative programming reduces the unit cell size by one-half or one-third, and so on. By the combination occasioned endurance stress and retention test, the reliability of MLVC-SONOS has been shown.

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