The Unified UE Baseband Modem Hardware Platform Architecture for 3GPP Specifications

Hyunil Kwon, Kyungho Kim, and Chungyong Lee

Abstract: **This paper presents the unified user equipment (UE) baseband modulation and demodulation (modem) hardware platform architecture to support multiple radio access technologies. In particular, this platform selectively supports two systems; one is HEDGE system, which is the combination of third generation partnership project (3GPP) Release 7 high speed packet access evolution (HSPA+) and global system for mobile communication (GSM)/general packet radio service (GPRS)/enhanced data rates for GSM evolution (EDGE), while the other is LEDGE system, which is the combination of 3GPP Release 8 long term evolution (LTE) and GSM/GPRS/EDGE. This is done by applying the flexible pin multiplexing scheme to a hardwired pin mapping process. On the other hand, to provide stable connection, high portability, and high debugging ability, the stacking structure is employed. Here, a layered board architecture grouped by functional classifications is applied instead of the conventional one flatten board. Based on this proposed configuration, we provide a framework for the verification step in wireless cellular communications. Also, modem function/scenario test and inter-operability test with various base station equipments are verified by system requirements and scenarios.**

Index Terms: **Hardware platform, HEDGE, LEDGE, modem system on a chip (SoC), pin multiplexing, stacking structure.**

I. INTRODUCTION

Various mobile products satisfying requirements of higher throughput, reduced latency, and improved coverage are being actively commercialized. In this situation, the associated system on a chip (SoC) solutions complying with a variety of wireless communication standards have been a critical factor. On the other hand, to satisfy diversified and fast-changing system requirements, the flexible platform architecture has been investigated [1], [2]. Among these approaches, to emulate hardwired design characteristics as close as possible, field programmable gate array (FPGA)-based hardware platform has been mainly used, especially in wireless cellular applications [3], [4].

In the sense of dominant global market share of asynchronous communication systems, in this paper, we focus on the fully-fledged 3rd generation partnership project (3GPP) series radio access technologies and the corresponding modem SoC development. Specifically, to meet the backward compatibility with current mobile telephony services, such as wideband code division multiple access (WCDMA) and to provide seamless transition into the promising 3GPP Release 8 long term evolution (LTE) [5], we target for the combination of 3GPP Release 7 HSPA+ [6] and global system for mobile communication (GSM)/general packet radio service (GPRS)/enhanced data rates for GSM evolution (EDGE) [7], dubbed HEDGE system. Table 1 lists specifications for HEDGE system.

Additionally, to provide efficiency and reusability in hardware resources, this paper presents the flexible pin multiplexing scheme to comply with another combination of 3GPP LTE and GSM/GPRS/EDGE, called LEDGE system. However, this paper only conceptually describes the pin multiplexing method regarding LEDGE system. On the other hand, to provide a stable testbed for testing and debugging process, we adopt a stacking structure. It consists functionally of an micro control unit (MCU) board, a digital signal processor (DSP) board, a modem board, and a radio frequency (RF) board.

The main goal of this paper is to develop and implement a unified user equipment (UE) baseband modem hardware platform to support HEDGE and LEDGE system, selectively. Based on this platform configuration, a framework of verification and debugging process, which is suitable for wireless cellular communication applications, is also given. The rest of the paper is organized as follows. In Section II, the unified UE hardware platform architecture is discussed. Based on the proposed platform, Section III provides a verification framework for HEDGE functionalities. In Section IV, several experimental results are given. Finally, conclusions are drawn in Section V.

II. THE UNIFIED UE HARDWARE PLATFORM ARCHITECTURE

The overall block diagram of the proposed unified UE platform is depicted in Fig. 1. To provide early adaptation to the latest advanced microcontroller bus architecture (AMBA) and seamless software transition toward modem application specific integrated circuit (ASIC) SoC solutions, we target for AMBA advanced extensible interface (AXI) bus architecture. Moreover, stacking structure has been adopted to mitigate timing critical clock-jitter and support stable debugging testbed.

Accordingly, the proposed platform is functionally divided into

- a modem board for HSPA+ physical layer air-interface,
- an ARM1156 based MCU board on top of ARM emulation baseboard (EB),
- two XpertTeak-based DSP board,
- an RF board for commercial radio frequency integrated circuits (RFICs) and power management integrated circuits (PMICs).

For HSPA+ test, the complete platform configuration illustrated in Fig. 1 is used. For GSM/GPRS/EDGE test, the DSP

Manuscript received September 30, 2009; approved for publication by Gerhard P. Fettweis, Guest Editor, September 01, 2010.

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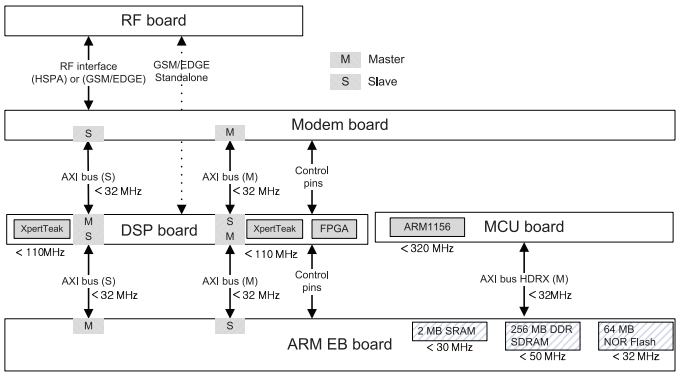

Fig. 1. The overall block diagram of the proposed platform.

Table 1. Specifications for HEDGE system.

GSM/GPRS/EDGE	
GSM features	FR/EFR/ARM/HR for voice codecs A5/1 and A5/3 for security Noise suppression, echo canceller
GPRS features	CS1/CS2/CS3/CS4 for coding schemes GEA1/GEA2 for encryption
EDGE features	236 kbps of multi-slot class 12 MCS 1-9 in downlink/uplink
HSPA+	
Specifications	WCDMA High speed downlink packet access (HSDPA) High spped uplink packet access (HSUPA)
Other features	Multiple input multiple output (MIMO) 64-QAM in downlink and 16-QAM in uplink Continuous packet connectivity (CPC)
Diversity	Space time transmit diversity Time-switched transmit diversity
Class capability	28.8 Mbps of Category 18 in downlink 11.5 Mbps of category 7 in uplink

board is connected directly to an RF board without a modem board, in which a FPGA on DSP board is used for hardware acceleration of GSM/GPRS/EDGE and RF control. While for LEDGE test, the downloading process of LTE dedicated FPGA image including the hardwired pin configuration of a modem board is only required in the complete board configuration given in Fig. 1.

A. An MCU Board

To control modem traffic and data flow in the form of the hardware-software development, ARM realview commercial EB board with core tile for ARM1156 is employed. Also, it is used for short software developing period and stable compatibility with latest ARM-series intellectual property (IP). Here, peripherals of the ARM EB, which is embedded on Virtex-II series FPGA, are partly modified to meet the AMBA 64bits AXI bus architecture. Throughout this paper, for convenience, an MCU board stands for the combination of the ARM EB and core tile for ARM1156. Meanwhile, this MCU board will be soon replaced by the latest ARM Core embedded HEDGE ASIC modem SoC to provide sufficient timing margin and the latest ARM related peripherals, such as peripheral component interconnect express (PCIe) and universal serial bus (USB).

B. A DSP Board

Recently, DSP solutions have been playing an important role in improving various wireless communication applications for

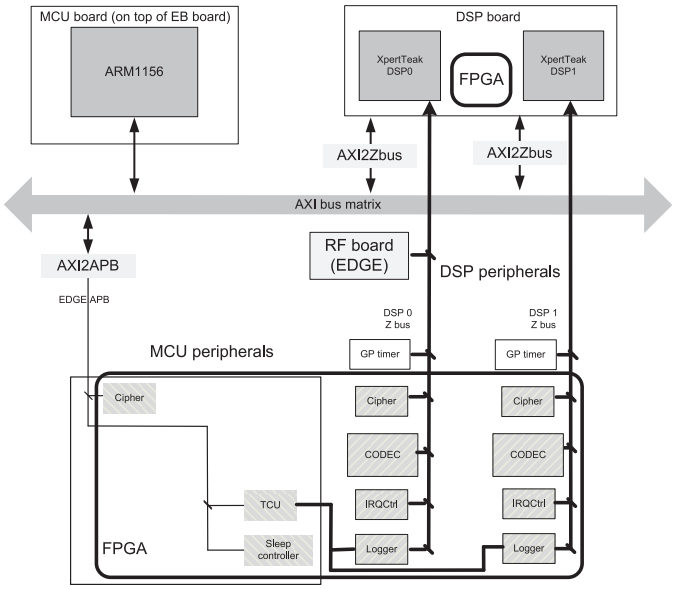

Fig. 2. The overall block diagram for GSM/GPRS/EDGE operating on a DSP board.

high-speed data transmission, in particular, the packet-based services [1], [2]. Furthermore, the advent of multi-core DSP guarantees enhanced performance in high-bandwidth wireless system as well as high computational applications, delivers a flexible platform for software development, and even reduces time-to-market delay for fast-changing mobile commercial products.

In this proposed platform, a DSP board with two XpertTeak DSPs and a Virtex-4 series FPGA have been used for GSM/GPRS/EDGE operation and HSPA+ dedicated computational or functional purpose.

Fig. 2 shows the overall block diagram for GSM/GPRS/EDGE operating on a DSP board. In what follows, a baseband coding and decoding (CODEC) hardware co-processor for a viterbi engine and a cipher engines in MCU/DSP side are implemented on a embedded FPGA. Here, viterbi co-processor engine helps equalization processing and convolutional channel decoding, which usually demands a large DSP million instructions per second (MIPS) resource. Cipher engine is used for cipher key generation and ciphering/deciphering of uplink and downlink data streams. Since these functions are implemented in the form of a hardware accelerator, higher security against unauthorized access is guaranteed. Among two DSPs, one DSP is mainly used for GSM/GPRS/EDGE function and the other DSP is used for additional MIPS processing and several HSPA+ dedicated functions listed in Table 2. On the other hand, for LTE test, a DSP board is directly applied without any change, where HSPA+ functions in the DSP board will be replaced into LTE dedicated functions.

As indicated in Fig. 2, the timing of hardware signals and software interrupts are controlled by timing and control unit (TCU). This unit interacts with sleep controller to enable low power operation and provides a logger for debugging. TCU operation is based on a multiple clock of 13 MHz. As other MCU peripherals, sleep controller is used for saving power during sleep and idle operation. Sleep controller forces main system oscillator

Table 2. HSPA+ dedicated functions supported by a DSP board.

HSPA+ dedicated DSP functions	
WCDMA	Fractional dedicated physical channel Paging indication channel detection
HSDPA	Chip equalizer processing MIMO processing
HSUPA	E-DCH HARQ acknowledgement E-DCH relative grant channel
CPC	Timing generation and parameter update
RF control	Transmit power calculation

consisting a 13 MHz voltage-controlled crystal oscillator to be shut down and allows an external low frequency oscillator for sleep operation to be calibrated with the main system oscillator. Among DSP peripherals, general purpose timer enables DSP to schedule special operations, such as frequency burst search process. Interrupt controller is used to control interrupt sources. Logger, which connects AMBA peripheral bus (APB) and Z-bus at once, provides APB debug framework and informs TCU event message and debugging information of DSP. The operation of DSP and TCU is logged into a file in sequence unit, and interactive operations between MCU and DSP board are finally verified. The RF solution for GSM/GPRS/EDGE is directly connected to Z-bus through analog-to-digital converter (ADC) and digital-to-analog converter (DAC).

C. A Modem Board

The overall block diagram for HSPA+ on a modem board is illustrated in Fig. 3. It consists of RF interface module, searcher module for system timing acquisition and synchronization, chip level processing (CLP) module, symbol level processing (SLP) module, uplink transmitter module, and lower medium access control (MAC) processing module.

RF interface module estimates input signal strength, adjusts automatic gain control (AGC) and automatic frequency control (AFC), and controls the gain of low noise amplifier and power amplifier. Various interfaces with commercial RF components, such as ADC, DAC, PMIC, and antenna diversity for multiple-input and multiple-output (MIMO) processing are supported.

Based on air-interface specifications, when the UE is powered on, searcher module initially performs slot synchronization, frame synchronization, scrambling code group search, and scrambling code search in a row. Moreover, re-acquisition for out of synchronization timing compensation when waking up from sleep mode, neighbor cell search for UE located in handover region, multi-path search for multi-path delay profile search, and offline search for power saving are supported.

Next, CLP module can be categorized into functions for WCDMA and HSDPA/HSUPA. CLP module for WCDMA receives an interpolated signal from RF interface module, then performs descrambling and de-spreading. And, it compensates the phase distortion and performs time and frequency tracking. Meanwhile, CLP module for HSDPA/HSUPA supports channel estimation for chip equalization, higher order modulation, MIMO processing, etc.

SLP module can be categorized into functions for WCDMA and HSDPA/HSUPA similar to CLP module. SLP module for

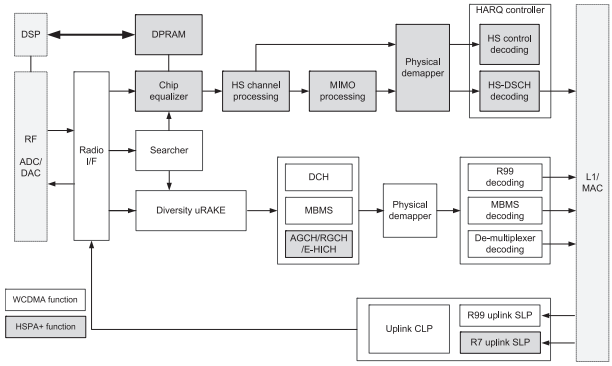

Fig. 3. The overall block diagram for HSPA+ system.

WCDMA consists of physical channel demapping, 2nd deinterleaver, 1st interleaver, rate matching, channel decoding with viterbi/turbo decoding, and cyclic redundancy check (CRC) check. While SLP module for HSDPA/HSUPA includes two functions; one is for demodulator of input buffering, demapper, deinterleaver, and 2nd rate dematcher, while the other is for decoding of 1st rate dematcher, turbo decoder controller, and output buffer controller.

Uplink transmitter module is in charge of the encoding chain for viterbi and turbo encoding, rate matching, and interleaving. Also, the modulator chain for spreading, symbol mapping/gain scaling, scrambling and code generator, timing generation for uplink channel transmission timing control, and discontinuous transmission scheme for power saving are supported.

Lower MAC (LMAC) module is defined as hardware accelerator to support fast data transfer for protocol stack layer 2, such as medium access control and radio link control. And, it is in charge of efficient bus and data path control through AXI bus to connect transmitter in uplink or channel decoder in downlink. To do this, LAMC module consists of encoder buffer for transmit path, decoder buffer for receive path, embedded direct memory access controller (eXDMAC) for AXI bus, and cipher function for security.

The implemented modem board for HSPA+ functionalities is composed of 7 Xilinx Virtex 5 series FPGA units shown in Fig. 7, in which each FPGAs has about 1200 I/O pins. Additionally, in the proposed platform configuration, in order to support LEDGE system, the flexible pin multiplexing described in Fig. 4 is applied. For easy identification, we omit a repetitive 1 pair of 2 FPGAs among 7 FPGAs. Specifically, for HSPA+ system, FPGA0 handles RF interface and search module, both FPGA1 and FPGA2 handle CLP module, FPGA3 handles SLP module, and FPGA4 deals with uplink transmitter module and LMAC module.

Based on the proposed platform, the pin mapping procedure is performed as follows. First, for inter-module connections of modem functions, the number of hardwired pin among each FPGAs is determined as the maximum dedicated pin connection value of specific HSPA+ and LTE module running on the same FPGA. For example, in case of HSPA+ system, the number of connections between FPGA2 for CLP module and FPGA3 for SLP module is 250 pins, while for LTE system, the number of connections between FPGA2 for frequency domain pro-

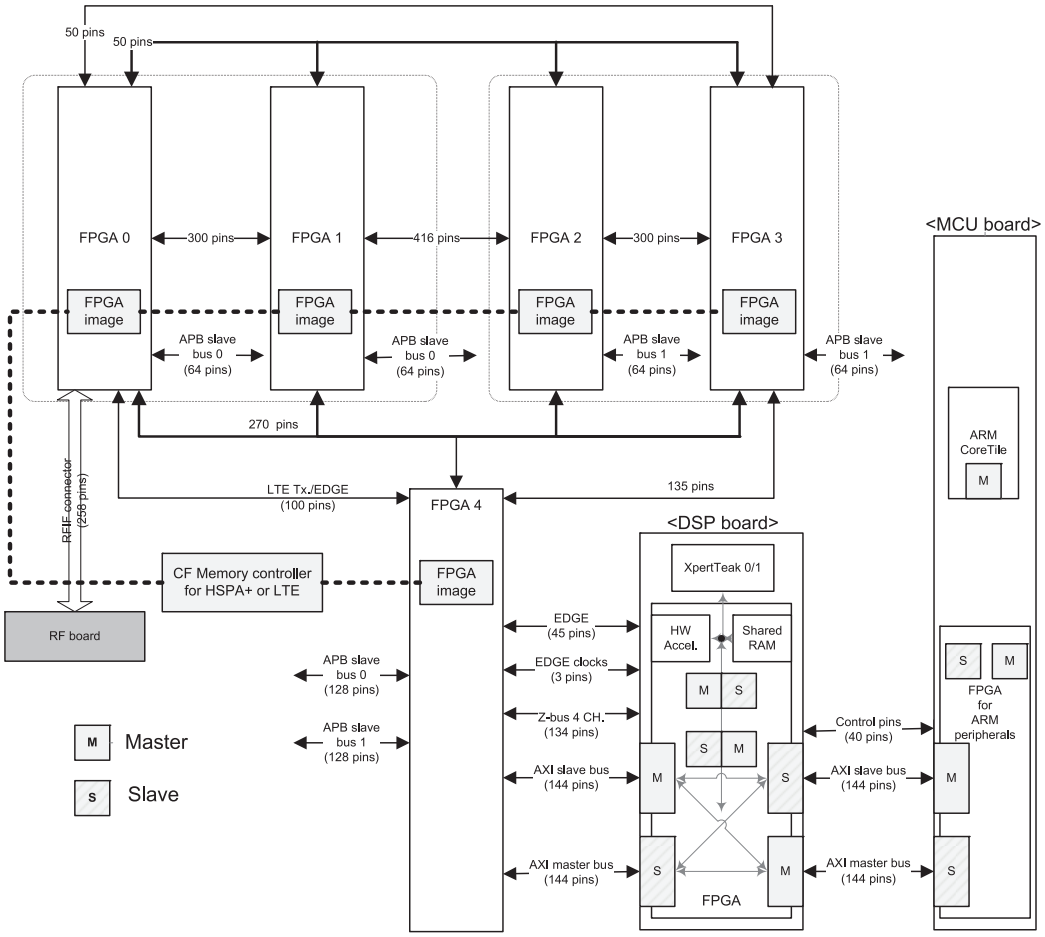

Fig. 4. The flexible pin multiplexing scheme for HEDGE and LEDGE system.

cessing module and FPGA3 for symbol level processing module is 300 pins. Eventually, physical pin connection is determined as 300 pins. Next, the connection for AMBA bus access, such as 144 pins for AXI bus and 64 pins for APB bus and 100 pins for common usage such as mictor connector, light emitting diode, DIP switch, and PROM interface are assigned on each FPGAs, individually. For example, in case of FPGA0 with an RF interface and search module in HSPA+ system, 258 pins for RF connector, 100 pins for FPGA4 connection, 300 pins for FPGA1 connection, 50 pins for FPGA3 connection, 270 pins for FPGA1/FPGA2/FPGA3/FPGA4 connection, 50 pins for FPGA1/FPGA2/FPGA3 connection, 64 pins for APB bus access, and 100 pins for common usage are physically assigned. On the other hand, HSPA+ or LTE dedicated FPGA image including modem functions and physical pin configuration is downloaded to each FPGAs through compact flash (CF) memory controller. To do this, HEDGE and LEDGE system can be selectively supported on this proposed platform.

D. An RF Board

To selectively support HSPA+ and GSM/GPRS/EDGE in HEDGE system, an RF board depicted in Fig. 5 supports both GSM/GPRS/EDGE RF solution and HSPA+ RF solution. HSPA+ clock signals from an RF board are supplied to a modem board to meet the minimal skew. On the other hand, the

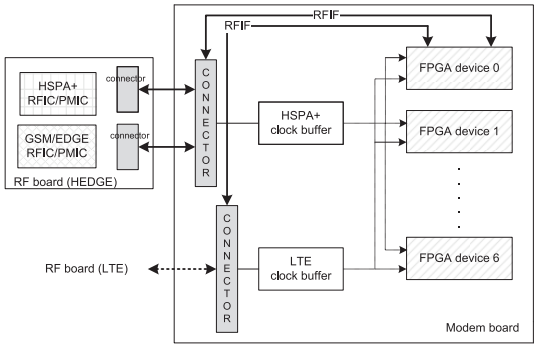

Fig. 5. The overall block diagram of an RF board.

additional connector and clock buffer for LTE system are also integrated on a modem board.

III. A VERIFICATION FRAMEWORK FOR HEDGE FUNCTIONALITIES

In this section, based on the proposed platform, a verification framework for HEDGE system is described according to regularized flow for wireless mobile SoC [8]. This framework consists of modem function and scenario test, inter-operation test with laboratory base station (BS) emulator or commercial

BS equipments, and physical chip emulation test for low power design.

A. Function and Scenario Test

Modem function test is performed using internal random access memory (RAM) containing known vectors and Agilent ESG vector signal generator (E4438C). First, to individually verify each HSPA+ internal modem module, known input vectors, which is previously stored in the internal RAM of an MCU board, are applied. The output dump files generated by modem baseband operation and the expected results generated from c-language link are compared in bit-by-bit fashion. Next, various signal vectors generated from E4438C are used to enhance the code coverage and validate the integrity of the designed modem functions. Here, diversified function test cases are employed in SystemVerilog verification process, which is a combination of hardware description language and hardware verification language based on extensions to verilog hardware description language. Since parameter update boundaries and timing related control sequential paths are critical points in hardware design, SystemVerilog verification process is intensively applied on these critical points.

Next, specification-defined scenario tests are performed to evaluate physical and higher layer inter-operation with a complicated combination of physical channels. For simplicity, several HSPA+ based scenario test items are listed as follows.

- Cell search and broadcasting channel decoding procedure: After receiving a downlink cell synchronization command from the higher layer, it finds BS having the biggest received signal strength indication (RSSI) value among candidate BSs, executes the 3-step synchronization procedure, and broadcast channel decoding procedure to find BS system frame number, and verifies CRC value.
- Random access channel (RACH) transmission procedure: After receiving an RACH start command from the higher layer, it transmits RACH preamble in uplink, receives acquisition indicator channel in downlink, transmits RACH message in uplink, demodulates message at BS, and verifies the CRC value in a row.
- Uplink/Downlink packet 384 kbps transmission procedure: After receiving a packet transmission command from the higher layer, it verifies each 384 kbps packet CRC value within UE and BS pair, and then reports estimated packet throughput into the higher layer.
- Power control procedure: After receiving a power up/down control command in closed loop fashion, it verifies increased or decreased power level through signal analyzer.

On the other hand, for mutual operation between different radio access technologies or frequencies, UE receives commands from radio access network and then measures qualities of the targeted cell. To do this measurement, radio access network verifies UE capability and instructs UE to enter compressed mode. In this scheme, the intersystem timing and the associated hardware operation are verified. For example, in handover region, when UE inside an HSPA+ serving cell is required to measure the neighboring GSM cell or vice versa, the intersystem timing unit aligns the operating frequency between two radio access technology systems and generates the associated control signals. Fig. 6 shows an example of the intersystem timing signal when UE inside a GSM serving cell is required to measure HSPA+ cell. Once GSM TCU operates, softer or frame interrupts and 3GMeasureStart signal are launched. And the operation transmission gap signals (T1–T9) for the associated HSPA+ operation are also generated along pre-defined interval x1–x6 shown Fig. 6. Using these generated signals, the measurement of HSPA+ cell is carried out and the associated results are informed to verify whether the operation is correct or not.

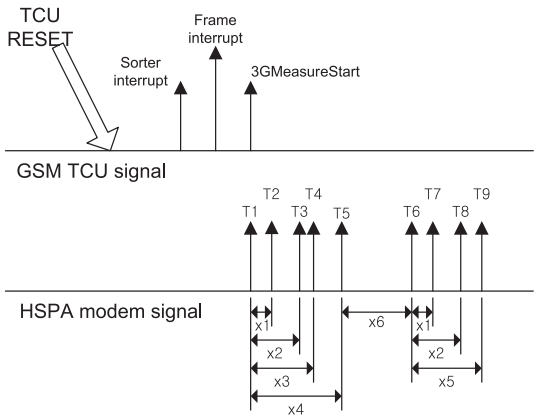

Fig. 6. An intersystem timing example for HSPA+ measurement in GSM serving cell.

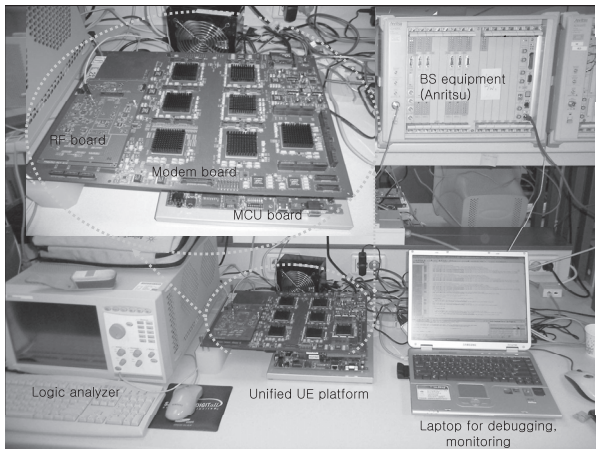

Fig. 7. The interoperability test environment for HSPA+ system.

B. Interoperability Test with BS Equipment/Emulator

For commercial wireless communication applications, FPGA based hardware platform is generally used as a mobile station. Also, it should be tested with laboratory BS emulator or commercial BS equipments according to each conforming testing specifications [9], [10]. To do this, modem full software including layer 1 and layer 2/3 protocol stack is ran together with interrupt priority and scheduling routine.

The overall test environment for HSPA+ hardware/software inter-operability and performance measurement is illustrated in Fig. 7. In what follows, personal computer, represented by laptop, is used for software downloading and monitoring, CF memory downloading, and board debugging. Signaling mes-

sage exchanges and data transfers between the unified UE platform and Anritsu BS equipment are carried out in this configuration. Meanwhile, when the laptop is used for compactflash downloading, the current call flow can be verified in real time basis. Also, with this complete test configuration, voice call test and file transfer test are performed. In a call test, mobile-oriented and mobile-terminated call set-up procedures are employed. For GSM/GPRS/EDGE call test, Racal-Dana series digital radio measurement set is used instead of Anritsu BS equipment for HSPA+. In a file transfer test, to measure the maximum throughput, the still image or music file is transferred in uplink or downlink and then data throughput is measured.

C. Physical Chip Emulation Test for Low Power Design

Wireless mobile applications have strict power requirements comparable to computer and embedded applications, while the clock speed and the integration density are lower than others. As a result, low power SoC design to minimize power dissipation is a critical factor towards a commercialization of wireless cellular products.

In ASIC SoC development, the dynamic power consumption by clock-switching is known to comprise nearly 30-50 percent of total chip power. To reduce this unnecessary clock switching, the clock gating is generally used in physical logic synthesis stage [11]. This solution is performed by electronic design automation (EDA) tools. However, there is a limitation in the fundamental low power SoC design.

In order to provide more aggressive power reduction, we employ two power control schemes. First, in the scenario based power domain classification, when the specific module is applied, the modules not correlated with this specific module operation are put into power-off domain. For example, in case of GSM/EDGE operation, HSPA+ modules are powered-off, except for the sleep and paging indication operation related modules. Second, in simple operating frequency based clock domain classification, all internal modules and IPs are categorized into diversified clock domains with respect to the operating frequencies, and the power is controlled by each clock domain. In Fig. 8, regarding the operation clock, overall blocks in HSPA+ uplink transmitter module are classified into four clock domain such as chipx1, chipx2, bus clock, and Z-bus clock. Accordingly, during WCDMA operation, chipx1 and bus clock domain blocks are in operation and other clock domain blocks are powered-off for power saving. While, for HSPA+ operation, chipx2, bus clock, and Z-bus clock domain blocks are in operation and chipx1 clock domain blocks are powered-off. On the other hand, those classification criterion should be carefully configured, because too fine clock domain classification is not easy to control.

Additionally, to functionally verify this power saving scheme on the proposed platform, we generate gated clock source complying with pre-defined clock domains or scenarios and execute the previous function/scenario test in subsection III-A, repetitively. Meanwhile, the real effect of this low power design will be physically measured on a test platform of released ASIC modem SoC sample and the associated mobile phone board.

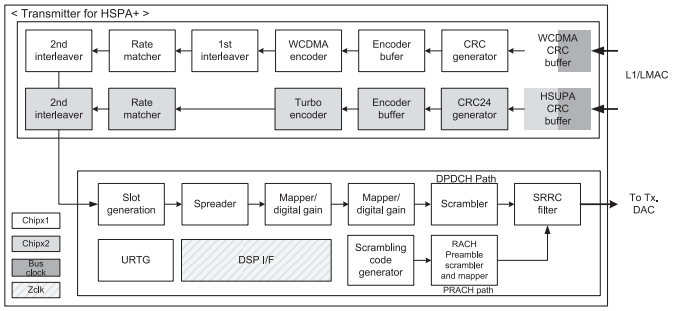

Fig. 8. Four clock domain classification for HSPA+ uplink transmitter.

Table 3. Data throughput in terms of wait cycle.

Wait cycle	Data throughput
0x0	52.2 Mbps
0x1	52 Mbps
0x2	51 Mbps
0xf	26 Mbps

IV. EXPERIMENTAL RESULTS

In this section, several performance results concerning the maximum operational clock speed and data throughput, which has been known as a main bottleneck in packet based services, are given. First, the maximum measured operation clocks are written by italic numerical values in Fig. 1. Here, the maximum clock frequency of 32 MHz between each boards is guaranteed on the proposed platform. This measured frequency is slightly higher than required 30 MHz clock of the conventional board. Also, the maximum operational frequency of XpertTeak DSP core of 110 MHz and the frequency of ARM1156 core of 320 MHz are measured om the proposed platform, respectively.

Meanwhile, in a commercialization of cellular applications, the combinations with regard to memory type and size are key features of design choices. Also, to support various high data-rate services, data throughput performance correlated with efficient memory access times is another. To comply with these requirements, we have carried out a simple data transfer test with internal and external memory. Here, the kind of internal memory is 64 bits data bus width at 30 MHz and that of external memory is 32 bits mobile double data rate (mDDR) synchronous dynamic random access memory (SDRAM) at the operating frequency of 50 MHz, individually.

First of all, since memory interface of a modem board is a bridge type of AMBA AXI bus, the wait cycle setting for efficient conversion on the bus should be optimized. To find the optimal wait cycle, we have tested data throughput in terms of different wait cycles, as shown in Table 3. As the wait cycle is smaller, the throughput performance improves while the timing margin is tighter. Eventually, we have found the optimal wait cycle of 0x1-0x2 with satisfying predefined timing margin requirements.

Next, data throughput test regarding internal and external memory has carried out. In internal memory based test, the conventional direct memory access (DMA) controller on an MCU board reads internal memory through a modem board's mem-

Table 4. Data throughput regarding internal and external memory.

	Data throughput
Internal memory based test	54.8 Mbps
External memory based test w/ LMAC	53.4 Mbps

Table 5. Processing time for data throughput in HSPA+ uplink.

	Processing time
Flatten structure	278.2 μs
Proposed platform	135.2 μs

ory interface, and then transfers the data into first-input first-output (FIFO). In external memory test, when the aforementioned LMAC module is employed, eXDMAC in LMAC module writes the data into external mDDR SDRAM using efficient data sequence control to eliminate redundant memory access, and similar procedure of internal memory test is applied. In Table 4, we show that internal memory based 54 Mbps throughput is nearly achieved by external memory test with efficient LMAC control, despite the performance degradation caused by external bus congestion. Thus, one of key features of beyond 3G standards, in other words, various multimedia services such as music and user-created contents (UCC), which requires huge external memory and efficient memory interface, can be sufficiently tested on our proposed platform.

Next, to compare processing time between our proposed platform and the conventional flatten board, we have investigated some of HSUPA specifications, which require 11.5 Mbps data rate in uplink and 640bits of protocol data unit (PDU) size. In the conventional flatten board, two kind functions of data transfer and cipher are separately implemented due to location or timing limitation between two functions embedded FPGA and external memory. In other words, this is mainly from long propagation delay of the flatten structure. As shown in Table 5, when it comes to one memory access time of roughly 71.5 μs, the existing board consumes processing time of 278.2 μs due to multiple number of memory access. However, in our proposed platform, due to stable stacking platform structure and LMAC control eliminating the redundant memory access time, we can approximately reduce processing time by half as 135.2 μs. On the other hand, the advent of the new MCU board including the latest ARM Core embedded HEDGE ASIC modem SoC, memory access time of 71.5 μs can be enhanced.

V. CONCLUSIONS

The unified UE baseband modem hardware platform to selectively support HEDGE and LEDGE system is presented. In order to do this, we propose a flexible pin multiplexing scheme in the hardwired pin mapping process. Moreover, the stacking structure is employed for stable testing and debugging process. Based on a framework for verification step, we evaluate HEDGE functionalities and some experimental results are given. Also, several investigations on low power design for wireless modem SoC development are described.

In addition to intangible contribution such as energy or cost efficiency by hardware resource reuse and developing/debugging time reduction, with given experimental results, our proposed platform can be highly helpful in developing wireless cellular communication applications.

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