From the EIC

Test compression saves bits, cycles, and money

As design sizes have grown larger and semiconductor manufacturing processes have scaled down to extremely small feature sizes, the number of test vectors needed to thoroughly test a chip has exploded. To alleviate this potentially road-blocking issue to further technology scaling, test data compression became an active research topic in the late 1990s, and has now become a standard offering within commercial DFT solutions. State-of-the-art compression schemes can achieve 10× to 100× reduction in both tester cycles and data volume. This might sound incredible, considering that Moore's law has been predicting only about 2× reduction every 12 to 18 months. However, many of the bits in test vectors are don't-care bits, and not every bit in the output responses needs to be observed in every test clock cycle. Test data volume is no longer a critical concern, thanks to the advances in test compression architectures, algorithms, and tools in the past decade.

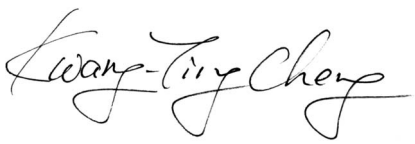
This issue of *IEEE Design & Test* features a special issue on the current state of test compression. Our guest editors, Scott Davidson and Nur Touba, have selected four articles, one of which provides a historical perspective on test compression for scan-based designs. The other three articles discuss architectures, methodologies, and algorithms for three different test compression technologies, two of which have been deployed in industry. I would like to take this opportunity to thank Scott and Nur for putting together this excellent issue.

This issue of *D&T* also concludes the theme of design and test of RFIC chips (featured in the Jan./Feb. 08 issue), with two additional articles. One of these introduces a low-cost, loopback DFT approach for single-VCO-based transceiver architectures. This DFT method overcomes the limitations of conventional loopback approaches for wafer probe testing. The other article demonstrates a wireless, embedded signal delivery system that can test multiple circuits simultaneously using a single RF test source.

Also included in this issue are two general-interest articles. One of these offers interesting insights about the tolerance to chip defects and errors at the application level. Observing that the presence of some defects or errors in a chip might not cause system malfunctions in specific applications, the authors attempt to define, characterize, and identify such defects with respect to the application context. The second article presents an approximate model for the drain-source current of a carbon nanotube FET in the ballistic regime. This model enables fast, accurate calculation of the drain-source current in a CNFET and thus can facilitate circuit-level simulation for designs based on these emerging devices.

Finally, this issue features an interview with Bob Dennard, the inventor of DRAM. Ken Wagner spoke to Dennard on his foundational work in DRAM as well as his views of CMOS process scaling.

I hope you enjoy this issue. If you have any feedback, please share it with us.



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