# Guest Editor's Introduction: Advances in Infrastructure IP

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**TODAY'S** SoCs need more than just the functional IP cores, such as processors and memories. They require embedding a special family of IP blocks, called infrastructure IP. These blocks don't add to the SoC's functionality, but rather support its manufacturability during product realization and support its operation in the field. For example, although every stage in the IC realization process affects yield, the semiconductor fabrication stage has the greatest impact because it is constantly evolving to implement advances in the fabrication process. For every new material or novel technique, a new generation of yield-limiting faults emerges. Furthermore, the increase in design complexity and the shrinking geometries in very deep-submicron technologies make devices more susceptible to systematic and random defects; debugging such designs is difficult.

## Infrastructure IP for ramp-up

Typically, yields are low for an IC's initial lots. Ramp-up, a critical period in the process, detects, analyzes, and corrects the yield problems of first silicon. Thus, the yield slowly ramps to a mature level, and then volume production begins. Shrinking the ramp-up period significantly impacts time to volume. Effective solutions that help yield learning, silicon characterization, and ease of test and debugging can be very valuable. The special issue in May-June 2002 *D&T* introduced such solutions, which used infrastructure IP to enhance the effectiveness of yield learning and shorten the time needed to reach volume production.

## Subsequent IC production stages

One year later, this special section addresses subsequent IC production stages—specifically, the volume production stage and field operation, where infrastructure IP plays a major role in improving production efficiency. Although the massive adoption of 90-nm technology could be somewhat delayed, causing an extension in the life cycle of 130-nm technology, the need for infrastructure IP that supports efficient manufacturability and field operation remains.

The articles in this special section expand our original coverage of basic infrastructure IP blocks for test and characterization. They introduce more advanced capabilities such as IP repair, protection, and configuration; they also expand our understanding of SoC-level challenges to those of manufacturing boards and systems. In the first article, Benso et al. discuss infrastructure IP for in-field, online self-repair. Next, Zorian and Shoukourian discuss field-level repair and power-up soft repair of embedded memories to achieve high manufacturing yield. Third, Quasem, Jiang, and Gupta present a SoC-specific test methodology that combines test application and DFT cost benefits with IP protection. Finally, Clark and Ricchetti discuss infrastructure IP for board- and system-level debugging and configuration.

**BOTH LAST YEAR'S SPECIAL ISSUE** and this year's special section on infrastructure IP constitute initial attempts to satisfy the growing need among design and test engineers to embed infrastructure IP in their designs. Future *IEEE Design & Test* issues, as well as the new Infrastructure IP Workshop (held in conjunction with the 2003 International Test Conference), will further address the variants of infrastructure IP and their value. ■

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