Test Challenges for 3D-SICs: All the Old, Most of the Recent, and Then Some New!

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Three-dimensional stacked integrated circuits (3D-SICs) are coming soon to a micro-electronics product near you! The test community needs to prepare itself to be able to test this new generation of 'super chips'.

Obviously, 3D-SICs require all the basic test technology with respect to test generation, design-for-test, wafer probe, handling, and test equipment. In addition, 3D-SICs require most of the recently-developed advanced test technology as well: (small) delay-faults, VLV tests, IEEE-1500, RPCT, TDC, BIST, KGD, adaptive test, diagnosis, PFA, yield learning... Test technology has advanced beyond simple stuck-at pattern generation, scan-only DfT, and the traditional test cell; it requires at least an annual trip to ITC for a DfT or test engineer to stay up-to-date with all the latest developments!

As if this is not enough to handle, 3D-SICs also provide some new, unique test challenges of their own.

- 3D-SICs have many more moments where it could make sense to perform Known-Good Die (KGD) and/or Known-Good Stack (KGS) tests: for an n-die stack, we have potentially $2n$ test moments. Optimizing the test flow for maximum effectiveness at lowest cost involves deciding which KGD/KGS tests to execute and what the exact content per test should be. This test flow optimization will work out differently for different products.
- Modular testing, originally developed for SoCs, is a very natural test approach for 3D-SICs. It enables per-die and per-module yield tracking, and supports the optimization of KGD/KGS test flows by giving the user the freedom to decide where in that flow a certain module is tested and/or re-tested.
  EDA vendors need to strengthen their support for the modular test approach. This includes automatic test wrapper and test access mechanism insertion, and automated test protocol expansion from the test module to the chip I/Os.
- Fault models and corresponding tests for new intra-die defects in the 3D context need to be developed. These new defects are for example due to wafer thinning (required to expose the Through-Silicon Vias (TSVs) at the back-side of the wafer), but also include malfunctioning ICs due to thermal and thermo-mechanical stress.
- The TSV-based interconnect is a new structure, unique to 3D-SICs. The defects in TSVs, before and after bonding, need to be studied, and classified into fault models, such that tests can be developed for them.
- KGD wafer probe solutions need to be developed that work with the small feature sizes, stringent probe damage requirements, and large numbers of TSV-based interconnects.
- KGS wafer probe solutions need to be developed that can handle stacks of thinned dies, and the non-flat profile of die stacks on wafers.
- DfT architectures need to be defined that take into account the unique requirements of 3D-SICs, such as the fact that the test source/sink might be different during KGD, KGS, and final tests. The DfT architecture should support modular testing, and leverage existing DfT standards as much as possible.
- Re-evaluation of the test resource partitioning: which resource is put by whom in which die?

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