FPGA CHALLENGES AND OPPORTUNITIES AT 40NM AND BEYOND

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ABSTRACT

FPGA companies are amongst the earliest adopters of next-generation process technology. This involves many challenges, including power management, device modeling, increasing I/O performance to match the computational capacity, and enabling very large designs to be completed quickly.

Process scaling increases FPGA capacity and allows new features, such as high-performance I/O protocols (e.g. PCI Express). Scaling favours FPGAs over competing technologies, as fewer and fewer ASICs have the volumes to justify the cost of a design in cutting-edge technology.

I will give an overview of the challenges in designing a cutting-edge FPGA, and describe the solutions Altera has adopted in its 40nm Stratix IV FPGAs. I/O bandwidth is crucial. While the density of FPGAs is increasing rapidly, the number of I/O pins is not -- we need to move more bits through the same number of pins. Another challenge is to model the timing, power and signal integrity of increasingly complex FPGAs in increasingly variable processes, while still keeping the tools easy to use. Managing power is a third challenge. Each process generation roughly doubles the number of transistors per die and tends to increase leakage power. The power budget per FPGA is roughly constant, so we need to innovate to control power.

Ever larger FPGAs also necessitate innovation to keep designers productive. We must both keep the compile time of traditional FPGA CAD tools reasonable, and develop new tools that allow designers to create and verify more complex systems in the same time.

BIOGRAPHY

Dr. Betz received his PhD in 1998 from the University of Toronto, his MS in 1993 from the University of Illinois at Urbana-Champaign, and his BSc in 1991 from the University of Manitoba, all in electrical engineering. For his doctoral dissertation he developed the VPR place and route and architecture exploration system for FPGAs. He co-founded Right Track CAD to commercialize VPR. Altera acquired Right Track in 2000, and developed the Stratix and Cyclone FPGA families with the acquired technology. The responsibilities of Dr. Betz's team include next-generation FPGA architecture development; floorplanning, placement and routing; synthesis optimization; and timing, power and signal integrity modeling.

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