Spin Electronics

Demonstration of Ultralow Bit Error Rates for Spin-Torque Magnetic Random-Access Memory With Perpendicular Magnetic Anisotropy

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Received 2 May 2011, accepted 5 May 2011, published 14 June 2011.

Abstract—Bit error rates below 10^{-11} are reported for a 4-kb magnetic random access memory chip, which utilizes spin transfer torque writing on magnetic tunnel junctions with perpendicular magnetic anisotropy. Tests were performed at wafer level, and error-free operation was achieved with 10 ns write pulses for all nondefective bits during a 66-h test. Yield in the 4-kb array was limited to 99% by the presence of defective cells. Test results for both a 4-kb array and individual devices are consistent and predict practically error-free operation at room temperature.

Index Terms—Spin electronics, spin-transfer torque, magnetic random-access memory (MRAM), magnetic switching.

I. INTRODUCTION

Spin-transfer torque [Slonczewski 1996] magnetic random-access memory (STT-MRAM) is a new, nonvolatile technology that is especially promising for mobile applications. It combines the features of high-speed operation, good scalability, and low power consumption [Lee 2011]. Until recently, the majority of STT-MRAM devices employed thin magnetic films with in-plane magnetization [Chung 2010, Oh 2010]. However, it is well known from both theory [Sun 2000] and experiment [Kishi, 2008, Worledge 2010] that STT-MRAM with perpendicular magnetic anisotropy (PMA) would offer significant benefit in terms of reduced switching currents and cell size. We previously presented data on individual devices [Worledge 2011] that use the recently discovered interfacial perpendicular anisotropy in thin CoFeB free layers sandwiched between a Ta seed layer and an MgO tunnel barrier [Ikeda 2010]. Here, we discuss the results of bit error rate (BER) tests performed at room temperature on a 4096-b (4-kb) array using this material. BER is defined as the number of errors measured divided by the number of repetitions of read/write operations. Details about the characterization of individual devices and materials used can be found in our recent article [Worledge 2011]. The particular chip reported, here, had an 8-Å-thick $Co_{60}Fe_{20}B_{20}$ free layer underneath an MgO tunnel barrier and a reference layer similar to that described previously [Worledge 2011]. Device yield for this array was limited to 99% by 45 defective cells, which we attribute to contamination during processing. All of the unaffected cells achieved very good functionality.

Reliability of these PMA MRAM devices was evaluated using a suite of tests specially written for STT-MRAM development. These tests give full electrical and magnetic characterization of individual memory cells and functional performance of the whole MRAM array. The 4-kb test array was powered and exercised by a Verigy 93K tester. The chip has separate write drivers for "zero" and "one" states and a sense amplifier circuit for read-out, which was operated with 50-mV bias across the tunnel junctions. Timing is controlled externally by the tester. All functional tests were performed with a supply voltage of $V_{dd} = 2.8$ V and a relaxed cycle time of 200 ns to ensure reliable reading. The write pulses had a 500-ps rise time, and adjustable amplitude and duration.

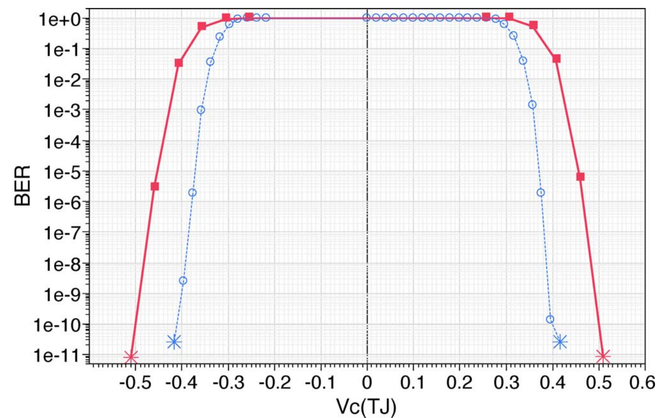

Fig. 1. BER dependence on write voltage amplitude V(TJ) for one MRAM cell. Negative and positive V(TJ) correspond to write "0" and "1," respectively. For both 10-ns (red, full squares) and 50-ns (blue, open circles) write pulses and both polarities, error-free operation was obtained at the upper end of the voltage sweep, after which the test was terminated. An upper bound on BER was calculated from the inverse of the number of writes, indicated by the stars at the ends of the curves.

II. MEASUREMENT OF BERs

Two BER tests were used to evaluate reliability of STT writing at low error levels: the individual BER test and the extinction BER test. The individual BER test consisted of a read/reset/read/write/read sequence, which was repeated on one junction as many times as was required to reach the requested error level. Both write and reset were done with the same amplitude and duration of voltage pulses. Three reads in this sequence allow identification of four possible error events, including write and reset errors, state reversions related with read disturbs, and bit retention errors. Fig. 1 shows the

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Digital Object Identifier: 10.1109/LMAG.2011.2155625

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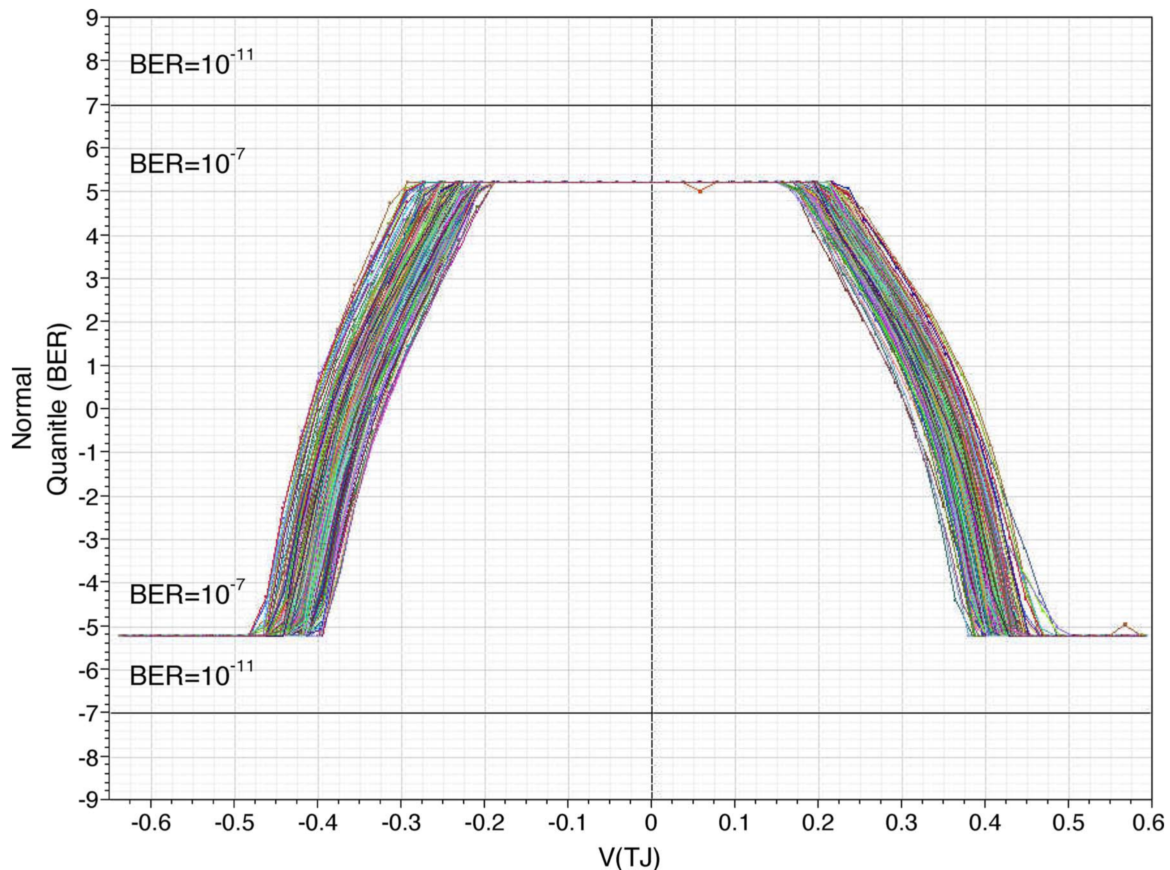

Fig. 2. NQ of BER for 256 randomly selected cells (each colored line represents one cell). Three cells (not shown) were defective. Each of the 253 electrically functioning cells reached the requested error floor of 10^{-7} and operated without errors at several higher voltages, as indicated by the flat parts of the lines. Two BER anomalies at around 60 mV and at 560 mV are external noise-related read errors.

dependence of individual BER on the write voltage across the tunnel junction V(TJ) for 10-ns- and 50-ns-wide write pulses and for writing both 0 and 1 for a randomly selected memory cell. This tunnel junction device was 140 nm in diameter and had resistance in the parallel state of 653 Ω and a magnetoresistance ratio MR of 43%. The corresponding resistance–area product was 10 $\Omega{\cdot}\mu$m^2. The device's coercivity, measured electrically with externally applied magnetic field and 20 μA bias current, was 480 Oe, and the loop offset was −72 Oe, with the antiparallel state preferred at zero external field. All BER tests were executed at 25 °C and zero external field. The most important result is that for both 10-ns and 50-ns write pulses, and for both bias polarities, we achieved error-free operation at the ends of every voltage sweep. At the end of every voltage sweep, the test was terminated due to limited test time (∼40 h) and the BER, indicated by stars in Fig. 1, was calculated from the inverse of the number of writes. Since at the highest values of V(TJ) not a single error was registered and the test was terminated due to limited tester time, the best BER estimated, here, is likely larger than the error rate the device would actually achieve for unlimited test time.

For both 50-ns and 10-ns write pulses, we achieved error-free operation at V(TJ) = 0.4 V and 0.5 V, respectively. These write voltages can be compared to tunnel junction breakdown characteristics. From breakdown statistics on the same type of devices, we know that for continue voltage stress V(TJ) = 0.5 V, mean lifetime is ten years [Robertazzi]. Hence, the breakdown-limited lifetime of this chip is likely longer than ten years for normal memory usage scenarios.

To examine device-to-device variations, the individual BER test was executed on 256 randomly selected cells. Fig. 2 shows the dependence of normal quantiles (NQ) of the BER on voltage amplitude for 253 functioning cells. Three cells were identified as defective in the first test cycle. The test was executed at 25 °C without external field and with 50-ns write pulses. All 253 functioning cells have similar shapes of NQ(V(TJ)), with all curves parallel to each other and bending toward lower V(TJ) at deeper BERs. Write voltages for individual cells in Fig. 2 were weakly correlated both with cell resistance and cell coercivity. Correlation coefficients were ∼0.43 and 0.31, respectively. The curvature separates two regions with different physical switching mechanisms: thermal activation over a voltage-dependent barrier at low V, and driven switching, gated by a thermal fluctuation in the initial condition and subsequently governed by conservation of angular momentum, at high V [Sun 2004, Bedau 2010]. After reaching the requested error floor of 10^{-7}, we continued writing at higher voltages to ensure error-free operation. Flat lines on both sides of the plot show that all 253

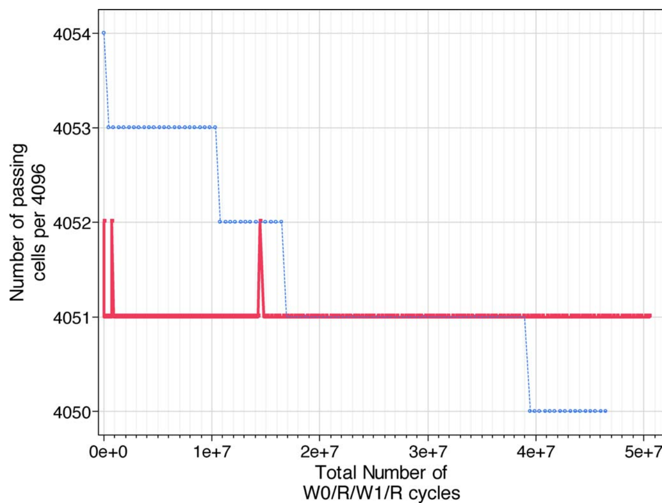

Fig. 3. Number of passing cells of a 4-kb test chip during a 66-h extinction BER test. For 50-ns write pulses (blue open circles), the write amplitude was 0.6 V and reading was not fully optimized. During a 62-h test, there were four errors. For 10-ns write pulses (red points), the write amplitudes were 0.6 V and 0.63 V for write "0" and "1," respectively. The 10-ns test was 66-h long and was divided into three parts, lasting 1 h, 19 h, and 46 h. At the beginning of each part, there was one error at the same address (red peaks). The remaining 4051 cells operated without a single error for more than 50 million cycles, which corresponds to a BER of 2.5×10^{-12}.

devices reached the test-time-limited error floor with each point on the flat parts of these lines corresponding to 10 million repetitions. This test was done with not fully optimized read conditions; two BER anomalies appear around 60 mV and at 560 mV in Fig. 2. Auxiliary diagnostics strongly indicate that these are noise-induced read errors. Time constraints prevented measurement of all 253 bits to BER $\approx 10^{-11}$, but by combining the data from Fig. 1 with these data, we can extrapolate V(TJ) to NQ $= 7$ (which corresponds to BER $\approx 10^{-11}$). This suggests that read disturb is well below 10^{-11} with 100-mV bias on the TJ, and that it is possible to achieve NQ $= -7$ (BER $\approx 10^{-11}$) at V(TJ) < 0.55 V. These results demonstrate that STT writing in these devices is very reproducible and suggest that error-free operation of STT-MRAM with PMA at room temperature may be possible.

Finally, we evaluated the whole 4-kb array by using the extinction BER test. The extinction BER test repeatedly executes a W0(4 kb) /R(4 kb)/W1(4 kb)/R(4 kb) sequence on the whole 4-kb array. Here, W0(4 kb) means write all 4 kb to the 0 state; R means read. For a particular cell, if both reads are as expected, the cell is flagged as passing. For every repetition, the program counts the number of passing cells and records the addresses of failing cells, which are then excluded in subsequent repetitions. Fig. 3 shows the number of passing cells as a function of test time for the whole 4-kb array for two write pulsewidths, 50 ns and 10 ns. At test initiation, there were 4054 passing cells for 50-ns pulses and 4052 passes for 10-ns pulses. By measuring device resistance and magnetoresistance for all cells, we found that there were 44 defective cells in this chip. The remaining 4052 good cells had MR $= 44.1 \pm 1.62\%$ and resistance in the parallel state Rp $= 659.4 \pm 29$ ohms. For the extinction BER test with 50-ns pulses, reading conditions were not fully optimized, and during a 62-h test there were four errors. These data illustrate how sensitive BER tests are to reading conditions on a wafer-level test, when the bits are digitally read by comparing to a reference voltage.

For the tests using 10-ns pulses, the read noise was reduced by replacing the probe card with one having better signal fidelity. As a result, we obtained error-free operation during a 66-h test. The test was divided into three parts, lasting 1 h, 19 h, and 46 h, and in all three tests the same address failed at the beginning of the test. If we consider that one cell as defective, we can estimate that the remaining 4051 cells were operating for 66 h without error, which corresponds to BER $= 2.5 \times 10^{-12}$ on these 4051 passing cells. This result is consistent with the individual BER tests.

III. CONCLUSION

Our demonstrated BERs are about four orders of magnitudes lower than those shown by Heindl *et al.* using STT-junctions with in-plane anisotropy [Heindl 2011]. This is in part due to a free layer in our junctions that is magnetically much thinner. Magnetically thinner free layers contain less total magnetic moment, which could be switched faster for a given amount of over-drive defined as V/V_{c0}, as dictated by angular momentum conservation [Sun 2000, Worledge 2011]. Furthermore, our BER decreases faster upon increasing write voltage than the macrospin model would predict, which is related to our junctions having lower energy barrier than the full volume macrospin value. A typical measured activation energy is of the order of 50 k_B T, roughly 4–6 times smaller than a simple macrospin volume estimate. The presence of such sub-volume thermal agitation is consistent with ultra-thin film thermodynamics including the thermal magnon degrees of freedom, and it alters the threshold position and distribution. This will be discussed in detail in a separate publication [Sun 2011].

We have demonstrated error-free operation of one randomly selected junction down to BERs of 10^{-11}. Furthermore, the BER dependence on voltage pulse amplitude measured on randomly selected 253 junctions does not show an anomalous switching (back-hopping) characteristic to junctions with in-plane anisotropy [Min 2010]. Finally, we have demonstrated that a 4-kb STT-MRAM with PMA can function with BER $<$ 10^{-11} at room temperature and 10-ns write pulses. Moreover, the achieved BER was limited by the experimentally accessible test time. This result suggests that STT-MRAM with PMA may work without error-correction codes.

ACKNOWLEDGMENT

The authors thank the staff of the Microelectronics Research Laboratory (MRL) at the IBM T. J. Watson Research Center for processing the MRAM wafers, and Eileen Galligan, Carol Jessen, and David Milletics for processing and measurements on unpatterned films.

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