Nanoelectronics Research for Beyond CMOS Information Processing

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I. INTRODUCTION

The field of nanoelectronics and, in particular, the vision of extending complementary metal–oxide–semiconductor (CMOS) and the possibility of discovering new, highly scalable, concepts for information processing and memory functions is becoming an exciting reality. Interdisciplinary research of nanoscale structures embodied in a myriad of new materials at the atomic-scale quantum domain promises the discovery of new paradigms for information processing. Specifically, research in nanoelectronics encompasses devices and technologies in which a critical dimension [e.g., channel length and/or thickness in a metal–oxide–semiconductor field-effect transistor (MOSFET)] is less than 100 nm and for which these nanoscale dimensions cause or amplify onset of new physical phenomena (e.g., quantization of channel charge in a MOSFET or the Coulomb blockade effect in a quantum dot). The invited papers in this special issue present a variety of nanostructures and related materials proposed to

This Special Issue presents a variety of invited papers covering nanostructures and related materials proposed to extend CMOS scaling to its ultimate limit and enable a variety of new logic and memory devices.

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extend CMOS scaling to its ultimate limit and enable a variety of new logic and memory devices. But first we digress to explore Moore's law scaling of silicon CMOS and memory technologies.

Silicon-based microelectronics will likely continue geometric and functional scaling for some time to come obtaining increased CMOS gate densities and enhanced circuit performance. This scaling will be achieved in many ways. Geometric scaling of the CMOS gate to smaller footprints, led by continuing improvements in lithography, will continue to drive this technology. However, geometric or Moore's law scaling eventually will encounter fundamental physical limitations. One such limit may be the extent to which electronic charge can continue to be used in its traditional role in digital electronics as the information processing "token." In this role, the presence of electronic charge on a MOSFET sufficient to realize a certain minimum voltage constitutes a logical "1" and the absence of this charge on the MOSFET constitutes a logical "0." Extreme scaling of CMOS will make it increasingly difficult to place and maintain electronic charge on this MOSFET, due to a variety of charge leakage mechanisms. In the domain of memory technologies, static random access memory (SRAM) and NAND Flash are also facing formidable challenges scaling to and beyond the 16-nm node. As an example, for SRAM, maintaining an acceptable noise margin as SRAM approaches the 16-nm node is an issue. For NAND Flash, scaling to the 16-nm technology generation may be limited by electrostatic coupling of adjacent cells and by other factors.

These eventualities place an exciting set of challenges before the nanoelectronics research community. The overriding opportunity is to develop a new concept and its enabling technology, capable of sustaining information processing (including memory) functional scaling beyond that attainable with ultimately scaled CMOS. This new concept could be based on use of a new "token" (e.g., electronic spin) to replace charge as the means to represent a bit of information.

Development of a new information processing technology is likely to be accomplished in two phases. The first phase would be its integration with CMOS to extend chip functionality beyond that possible with the "ultimately scaled" CMOS platform technology. The second phase would be further evolution to eventually realize a new, multifunctional, and scalable platform technology. For example, a spin-based magnetostatic RAM may first be integrated on a CMOS platform to replace the static RAM cache. In time, this could be followed by development of an all spin-based logic technology for performing processor logic and memory tasks.

A new concept for information processing must provide a means for representing and manipulating bits (or "tokens") as well as performing memory and interconnect functions using compatible technologies. Much of the current search, however, is focused on new devices to perform the information processing or the memory function. In both instances, research in nanoelectronics is playing a major role. As illustrated in this special issue, many new devices and technologies are proposed to perform either the processor function or the memory function, or in a couple of instances both functions in a universal device.

The invited papers included in these Proceedings of the IEEE are organized into five categories summarized below.

A. Nanoelectronics: International Collaboration and a Key Metric for "Beyond CMOS" Devices

The first category, consisting of the first two papers, overviews the research directions of major national and regional publicly funded nanoelectronics programs mapped onto eight research vectors. The second paper identifies reduced power dissipation as a key factor a new technology must offer as a replacement of CMOS. The second paper also evaluates and critiques the original five research vectors or directions proposed to guide research.

1) Many publicly funded nanoelectronics programs address the daunting challenges of extending Moore's law into the future. The first paper by Brillouët *et al.*, entitled "Regional, national, and international nanoelectronics research programs: Topical concentration and gaps," is an attempt to survey existing programs on emerging research devices and to find ways to support them through international collaborations. These results were obtained by an international working group [International Planning Working Group on Nanoelectronics (IPWGN)] founded in 2005 to provide information on European, Japanese, and United States nanoelectronics programs. The purpose of this project is to encourage international collaboration in the global search for a new information processing paradigm and technology. This group collected data from major publicly funded programs in Europe, Japan, and the United States on long-term nanoelectronics research. These programs and projects were mapped onto a set of research directions which are expected to drive nanoelectronics research for the long term. The objective was to identify those research topics attracting a lot of attention and those important topics that seem less attractive. This paper gives examples of inter-regional collaborative programs on nanoelectronics and identifies sources of funding specifically provided to support international collaborations.

2) The second paper, by Theis and Solomon entitled "In quest of the "next switch": Prospects for greatly reduced power dissipation in a successor to the silicon field-effect transistor," provides important insight to the search to replace the silicon MOSFET and CMOS gate as the unit logic device. They argue that of the several scaling parameters one can consider (e.g., constant voltage scaling of MOSFET dimensions, integration density, energy dissipation, etc.), reduced energy dissipation, limited by

economics, has become the most important. Three paths and several new device concepts are discussed to reduce energy dissipation. The three promising directions identified are energy filtering, internal voltage step-up, and internal transduction. The authors conclude that near- adiabatic switching does provide a theoretically possible path to low-energy operation but is unlikely to be implemented for a myriad of practical reasons. The paper concludes with a discussion critically reviewing the original five research vectors or directions guiding the U.S. Nanoelectronics Research Initiative.

B. Ultimately Scaled CMOS: Channel Replacement Materials

The second category, consisting of three papers, reviews use of carbon nanotubes, graphene, and III-V compound semiconductor nanowires as "channel replacement materials" to scale MOSFETs to their physical limit.

3) In the third paper entitled "Carbon nanotubes for VLSI: Interconnect and transistor applications," Awano *et al.* discuss application of carbon nanotubes (CNTs) to fabricate high-performance MOSFETs, interconnects, and vias. Because of the remarkable properties of CNTs, such as high-current density, ballistic transport, and ultrahigh thermal conductivity, they have potential for use as wiring materials and as alternate channel materials for extending CMOS performance in future very large scale integration (VLSI) technologies. The authors report the present status of CNT growth technologies and the applications for via interconnects and FETs. Growth of multiwalled CNTs at low temperatures with high density is reported and the authors have shown that a CNT via was able to sustain a current density as high as 5.0×10^6 A/cm^2 at 105 °C for 100 h without any deterioration in its properties. Last, a Si-process compatible technique is proposed to control carrier polarity of CNTFETs by utilizing fixed charges introduced by the gate oxide.

4) Since its discovery in 2004, no material has attracted more attention than graphene, which consists of a single or few layers of carbon atoms. The paper by Banerjee *et al.* entitled "Graphene for CMOS and beyond CMOS applications" summarizes several unique properties of graphene including very high mobility and linear band structure as well as challenges for digital logic applications. Furthermore, it is shown that such unique properties of graphene can lead to discovery and development of new "beyond CMOS" devices.

5) Semiconductor nanowires are considered as a promising alternative path to extend the Roadmap for scaled semiconductor devices. The improved electrostatic control in the cylindrical wrap-gate geometry and the possibility to utilize heterostructures in nanowire transistor design in both III-V and in group IV materials, are key advantages. The paper by Wernersson *et al.* entitled "III-V nanowires—Extending a narrowing road" presents an overview of the nanowire field with particular focus on the state- of-the-art for III-V nanowire devices implemented with a bottom-up approach. This approach appears to offer low contact resistance (in particular for InAs) and advantageous transport properties (high low-field mobility and saturated velocity, or rather high injection velocity in the ballistic limit). The III-V nanowire technology outlined in this paper may serve as a technology platform for low-power, high-speed applications, in the area of wireless technology and, at much longer term, provide a monolithic add-on of III-V optoelectronics to Si.

C. Extended CMOS: Hybrid Beyond CMOS Devices Co-Integrated on a CMOS Platform

The third category consists of one paper that discusses the co-integration of "beyond CMOS" devices onto a CMOS platform to extend the functionality of ultimately scaled CMOS.

6) The paper entitled "Enhancing CMOS using nanoelectronic devices: A perspective on hybrid integrated systems" asks the question: "In what ways might emerging research devices be integrated with CMOS technologies to yield systems with increased functionality?" The paper by Ricketts *et al.* provides a perspective on this question from the viewpoint of patterning technologies that enable direct writing on CMOS wafers. These technologies, e.g., tip-directed, field-emission-assisted nanomanufacturing (TFAN), enable the fabrication of nonvolatile, reconfigurable radio-frequency (RF) circuits, mechanical addressing of spin transfer torque magnetic tunnel junction (STT MTJ) memory devices, the integration of polymer nanowire sensors with CMOS, and perhaps ultimately, self-evolving systems using statistical learning.

D. Beyond CMOS Information Processing Devices: Noncharge-Based Devices

The fourth category has five papers addressing four new approaches to "beyond CMOS" information processing devices. Replacing electronic charge with a new information "token," these approaches propose as new tokens: electron spin (spin-up and spin-down), direction of a nanomagnetic vector, change in molecular configuration (change in molecular resistance) and charge-based molecular (change in molecular capacitance), and position of a micromechanical object. The fifth paper in this category proposes a new methodology, and reports preliminary results, for benchmarking and comparing the performance of several new information processing devices. This methodology involves evaluation of higher level logic functions implemented using each of the new devices.

7) Recent progress in microelectromechanical devices and related process technology has renewed the interest in mechanical computing for ultralow-power integrated circuit applications. In the paper "Mechanical computing redux: Relays for integrated circuit applications," Pott *et al.* overview the various types of micromechanical switches, with particular emphasis on electromechanical relays

as alternative devices for energy-efficient logic circuits. Their reliability and process integration challenges are discussed together with first demonstrations of low-power functional relay logic circuits. The authors suggest that submicron scaled relays can potentially provide $>10\times$ improvement in energy efficiency as compared with CMOS, for applications requiring performance up to around 100 MHz.

8) The paper by Seabaugh and Zhang "Low-voltage tunnel transistors for beyond CMOS logic" describes the use of interband tunneling to obtain steep subthreshold swing transistors at supply voltages less than a 0.5 V. After showing the potential of the tunnel field-effect transistors (TFETs) to compete with standard CMOS, the paper details the underlying theory of operation of the TFET. Finally, it addresses the key parameters and challenges for optimizing TFET performance.

9) The paper entitled "Molecular nanoelectronics" by Vuillaume discusses, perhaps, one of the more challenging if not speculative approaches to realizing a new paradigm for information processing. In addition to single molecules proposed as a three-terminal electronic logic switch, molecular electronics may provide means of assembling large numbers of molecules into nanoscaled objects to form new devices and circuit architectures. This paper confines its discussion to molecular nanoelectronics including fabrication and electrically contacting molecules (a very challenging task), and molecular electrical functionality based on use of a single molecule.

10) In this paper by Sugahara and Nitta entitled "Spin-transistor electronics: An overview and outlook," spin transistors are discussed as a new concept device that unites an ordinary transistor with useful functions of spin (magnetoresistive) devices. Spin transistors are expected to be a building block for novel integrated circuits employing spin degrees of freedom (i.e., spin-up and spin-down). Spin transistors could be used to realize nonvolatile information storage and reconfigurable output characteristics; features that are very useful and that offer suitable functionalities for new integrated circuit architectures that are inaccessible to ordinary transistor circuits. The authors review the current status and outlook of spin transistors from the viewpoint of integrated circuit applications. The fundamental and key phenomenological technologies for spin injection, transport, and manipulation in semiconductors, and the integrated circuit applications of nonvolatile logic and reconfigurable logic are described.

11) The paper entitled "The promise of nanomagnetics and spintronics for future logic and universal memory" by Wolf *et al.* provides an overview of basic principles associated with representing information in the form of magnetic polarization either as nanomagnetic domains of ferromagnetic materials or spin polarization of holes and electrons. Spin-based memory and logic devices are reviewed including magnetoresistive (MRAM) memories, spin transfer torque (STT-MRAM) memories, and magnetic quantum cellular automata (MQCA) logic structures. They introduce a new concept for assembling MQCA arrays called resistive arrays of magnetic automata (RAMA). The authors conclude that the inherent nonvolatility of magnetic materials at room temperature have obvious applications as memory devices and possible applications as nonvolatile logic structures. In addition, they offer potential energy savings relative to CMOS devices where the computational state must be constantly refreshed. Future engineering improvements in magnetic materials, structures, and circuits are likely to drive progress in this field.

12) The last paper in this section, by Bernstein *et al.* entitled "Device and architecture outlook for beyond CMOS switches," introduces the U.S. Nanoelectronics Research Initiative and catalogs many new device concepts that are being studied as an eventual replacement for CMOS. This paper then offers a quantitative methodology and some early results for benchmarking and comparing the performance of some of these new alternative logic devices used in a few common logic applications.

E. Nonvolatile Resistive Memory Devices Nanoscaled to the 8-nm Node

The fifth category consists of four papers addressing different approaches to resistive memory technologies. The first paper proposes a methodology for system-level analysis to examine the relationship of maximum performance of a memory element to its operative device physics. This method is demonstrated for DRAM and for a resistive RAM. The other three papers all review a different class of nanoscale resistive memories that offer potential replacement for NAND Flash and SRAM memory, which are facing very difficult scaling challenges at the 16-, 11-, and 8-nm nodes. Resistive RAM technologies discussed in this category are the phase change memory (PCM), the atomic switch, and the metal oxide memory.

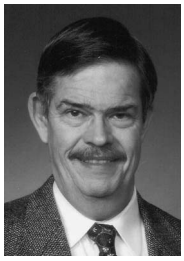
13) This paper, by Zhirnov *et al.* entitled "Memory devices: Energy–space–time tradeoffs," offers an interesting new principle or figure of merit for comparing different memory elements in terms of minimizing the product of their write/read time, write energy dissipation, and volumetric size. Using their new methodology, the authors find that for a DRAM, the optimum scaling is at $F \sim 40$–50 nm (F is the minimum half-pitch of memory cells), whereas for a generic resistive RAM, the figure of merit is a monotonically decreasing function of decreasing F and, therefore, does not predict an optimum value of F. The analytical framework seems to be a useful tool and can be applied to other devices. More refined analysis may be developed based on this framework and specific device characteristics.

14) A comprehensive and thorough review of PCM technologies, including discussion of material and device issues, is provided by Wong *et al.* in their paper titled "Phase change memory." The critical issues of PCM discussed in this paper begin with discussion of many approaches to substantially lower the write/erase or program current below 100 μA. Application of the PCM in a crossbar array will require a nonlinear select device for each memory element to ensure that only the chosen memory element is activated and not its neighboring elements. Currently, this select element must be a transistor in order to supply the large required program current. The footprint of this select transistor determines the density of the PCM array. The authors discuss the issues arising in their search for a much smaller diode select device and related issues (e.g., nearest neighbor thermal coupling) in scaling PCM below 10 nm.

15) One of the ultimate switches could be an atomic switch, where two terminals in a metal–oxide–metal (MOM) structure are connected or disconnected by a metal atomic bridge or wirelike filament. This paper, entitled "The atomic switch" by Aono and Hasegawa, describes the operation principles of the atomic switch and recent advancements in the research. They have demonstrated not only two-terminal but three-terminal atomic switches that can work as a nonvolatile transistor. Moreover, the integration of atomic switches with CMOS circuits has also been demonstrated.

16) The paper entitled "Resistive random access memory (ReRAM) based on metal oxides" by Akinaga and Shima reviews the class of MOM resistive memory structures, now called "Redox RAM," that depend on a chemical oxidation/reduction process to cause a relatively abrupt change in the resistance of the MOM structure upon application of a voltage pulse. This pulse must be of sufficient magnitude and duration to initiate a change in resistance states between the low resistance state (LRS) or set (program) state and a high resistance state (HRS) or reset (erase) state. The authors provide an overview of the technology, physical mechanisms governing the resistance switching processes, and the challenges of some of the better understood MOM structures. The paper also discusses the separate roles played by thermal mechanisms and electrochemical mechanisms in distinguishing between the unipolar and bipolar operations of these memory elements. ■

ABOUT THE GUEST EDITORS



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Dr. Hutchby chaired the IEEE Reynold B. Johnson Data Storage Device Technology Award Committee and the IEEE Electron Devices Society's Very Large Scale Integration (VLSI) Technology and Circuits Committee. He was General Chair of the IEEE International Electron Devices Meeting (IEDM), the IEEE Gallium Arsenide Integrated Circuit Symposium (now Compound Semiconductor Integrated Circuit Symposium), and the Workshop on Compound Semiconductor Materials and Devices. He also chaired the Duke University Electrical and Computer Engineering's Industry Advisory Panel. He is a recipient of the IEEE Third Millennium Medal.

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Dr. Hiramoto is a member of the Institute of Electronics, Information and Communication Engineers (IEICE) and Japan Society of Applied Physics. He was an Elected AdCom Member of the IEEE Electron Devices Society from 2001 to 2006. He served as the General Chair of Silicon Nanoelectronics Workshop in 2003 and the Program Chair in 1997, 1999, and 2001. He has served on Program Committee of Symposium on Very Large Scale Integration (VLSI) Technology since 2001. He also served on Program Subcommittee on CMOS Devices of the International Electron Devices Meeting (IEDM) in 2003 and 2004. He was the Subcommittee Chair of CMOS Devices in 2005, the Asian Arrangement Co-Chair in 2006 and 2007, the Publications Chair in 2008, and the Emerging Technologies Chair of IEDM in 2009.

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