A Future of Integrated Electronics: Moving Off the Roadmap

BY DANIEL J. RADACK, *Senior Member IEEE*
Guest Editor

JOHN C. ZOLPER, *Senior Member IEEE*
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Continuous advances in the miniaturization of electronics over the last 30 years have enabled the Information Age for 21st-century society. Throughout the last few decades, computers and other information and entertainment appliances have made tremendous gains in performance, productivity, and power efficiency based almost entirely on the scaling of field-effect transistors and their integration into ever more complex circuits. In 1965, Moore's law, or, more accurately, "Moore's projection," asserted that the number of transistors on an integrated circuit would double roughly every two years. This has resulted in an exponential increase in chip complexity and performance and has been the engine for innovation in integrated circuits. The seemingly endless ability to reduce the critical dimension of the transistor and thereby increase the performance and decrease the cost of a transistor has enabled new products and industries.

This issue presents topical papers discussing prospects for alternative strategies that will continue to deliver increased performance and functionality on a semiconductor-based integrated platform.

Today, however, the traditional approaches to transistor scaling and integration are slowing. The scaling reductions of the past appear to be facing fundamental limitations in the future due to electrostatics and parasitic phenomena. In addition, there are emerging issues with the increasing complexities of design and successful construction of circuits. While the issues are daunting, there are innovative efforts to overcome the barriers and maintain a path for improving future microelectronics generations that continue to deliver ever increasing performance and ever decreasing power dissipation while also reducing the cost per function. This special issue, entitled "A Future of Integrated Electronics: Moving Off the Roadmap," presents topical papers discussing prospects for alternative strategies that will continue to deliver increased performance—or, more generally, increased functionality—on a semiconductor-based integrated platform.

The scaling of the complementary metal–oxide–semiconductor (CMOS) field-effect transistor (FET) has been the key to innovation; however, conventional scaling faces severe challenges caused by practicalities of materials, processing, fundamental physics, and electromagnetics. Research efforts to find new scaling tactics are making progress for traditional applications and are also exploring new territories that are well off and outside the confines of traditional scaled CMOS.

The first group of papers discusses recent progress and directions in new device concepts, materials, fabrication processes, interconnects, and circuit architectures for moving beyond the extrapolation of conventional scaling. Prospects for replacing traditional semiconductors with other materials such as carbon nanotubes (CNTs) and spin-based logic devices are described.

The first paper, by J. Appenzeller (Purdue University, formerly IBM Research), provides an overview of the progress and outlook for exploiting

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carbon nanotubes as potential replacements for silicon field-effect transistors and other switching devices. Nanotubes have many attractive properties, including high mobility and highly confined channel conduction. However, they are encumbered with several critical challenges in placement and chirality control. Dr. Appenzeller describes the critical material and processing parameters necessary for implementing useful devices. This paper presents state-of-the-art results for a single wall carbon nanotube transistor and the first demonstration of CNT-based circuits. He also provides a discussion of the unique capabilities of the carbon nanotube for electronic applications with an overview of the remaining technical challenges.

The second paper in this section, by K. L. Wang *et al.* (University of California, Los Angeles), describes the efforts to exploit new functional materials, self-assembly fabrication processes, and nonconventional devices in new circuit architectures to either supplant or transcend the performance trajectory of CMOS scaling. This paper focuses on approaches that employ the heterogeneous integration of alternative materials with silicon to enable new switch functionality. The authors discuss work on the cointegration of III–V materials on silicon and progress in developing spin-based logic elements, and thereby exploiting a new domain of state variables. The status of these approaches, which are still in the early demonstration stage, is discussed, and future directions are outlined.

The third paper in this section, by R. G. Beausoleil *et al.* (Hewlett-Packard Laboratories), presents a discussion of the emerging on-chip communications bottleneck that is resulting in the intrinsic processing capability of complex, multicore microprocessors becoming unbalanced with the bisection communications bandwidth available from today's metal global interconnects. The imbalance is resulting in poor utilization of the processing cores. This paper presents an analysis of the role nanophotonics can play to enable power efficiency: on-chip optical interconnects that could restore the communications to processing balance and potentially give a four orders-of-magnitude increase in the bandwidth-to-power ratio over current projections for scaled metal interconnects. This paper reviews key challenges in developing such on-chip optical networks.

The final paper in this section is by R. F. Pease (Stanford University) and S. Y. Chou (Princeton University) and provides an overview of research and development in lithography and patterning for future nanoscale devices. Historically, lithography has been the key processing technology enabling continuous scaling. However, major challenges exist in pushing optical patterning to maintain scaling to 22 nm and below. This paper includes a new view of the limitations of beam-based methods as well as nano-imprint and similar methods of physical pattern transfer. The authors present current approaches and limitations and point to potential future solutions to patterning at the 22-nm technology node and below.

The next set of papers focuses on heterogeneous integration of materials and devices to form new circuit fabrics outside of the conventional digital domain. These alternative strategies bring additional functionality to the semiconductor platform that cannot be readily achieved with digital silicon CMOS technology.

The first paper in this area by M. J. Rodwell *et al.* presents progress in realizing ultra-high-performance transistors and circuits based on compound semiconductors, specifically InP heterojunction bipolar transistors (HBTs), that offer unique speed and power tradeoffs. An analysis is given of the scaling laws in InP HBTs that identify a path to a transistor with unity current gain (f_t) and the maximum frequency of operation (f_{max}) of 1 THz. Current results for f_t and f_{max} over 500 GHz are presented along with a discussion of the implementation of circuits such as simple static dividers operating at 150 GHz and direct digital synthesizers clocking at 30 GHz. These InP HBTs are particularly attractive for high bandwidth, high dynamic range mixed-signal circuits such as analog-to-digital converters and digital synthesizers.

The next paper in this section is by U. K. Mishra *et al.* and covers the materials, device, circuit technology, and status of wide-bandgap semiconductors, namely gallium nitride (GaN) and aluminum gallium nitride (AlGaN), for radio-frequency (RF) circuits. GaN-based RF circuits are emerging as the next technology for wireless cellular transmitters and for high-power military radars. These materials enable the realization of RF transistors to operate at ten times the voltage, for a given frequency, of conventional gallium arsenide (GaAs) technology, thereby enabling higher power, higher efficiency, and more compact RF components. Also discussed is the current status of technological development that is on the verge of achieving suitable reliability demonstrations to support system insertions.

The following paper is by G. K. Fedder *et al.* and covers the cofabrication of microelectromechanical devices with microelectronics devices to develop integrated microsystems for sensing, actuation, and signal processing. This paper reviews the strategies for cofabrication, with an emphasis on modular approaches that do not mix process sequences. The integrated processes are presented in the context of physical sensors, chemical and biological sensors, displays and optical switches, and nonvolatile memories.

The subsequent set of papers provide an overview of advanced research and activities to reshape design and circuit architectures. Design and architecture are major challenges in attempting to increase performance and functionality of integrated electronics, especially as they become more complex and move into nonclassical regimes of performance.

The first paper in this section by H. S. Lee and C. G. Sodini describes challenges in increasing the

performance of mixed-signal circuits, specifically analog-to-digital converters (ADCs), in the context of scaled CMOS technology. Mixed-signal circuits are critical in many applications, and there is interest in greater bandwidths, dynamic ranges, and lower power. An overview and in-depth technical discussion are given about the prospects for fabricating mixed-signal circuits in scaled CMOS technologies. Focusing on ADC circuits, Lee and Sodini describe the current state-of-the-art and limitations of ADCs from the technology perspective. They then discuss emerging techniques to enable mixed-signal circuits in deeply scaled technology generations with a particular emphasis on a new approach that replaces conventional op-amp based designs with a zero-crossing sensor referred to as a comparator-based switched-capacitor circuit. While this alternative approach is still being proven, it highlights several of the challenges facing mixed-signal circuit designers using scaled CMOS.

The next paper, by A. F. J. Levi, describes work to develop a design approach for implementation of new functions using quantum devices. He discusses a technique of solving an inverse problem to attain the desired function based on physics of atoms and collections of atoms, essentially a methodology for synthesis.

The final paper is by B. H. Calhoun *et al.* and provides an overview of the latest efforts to develop a new design methodology that overcomes some of the undesirable attributes of deeply scaled CMOS such as increase variability, leakage current, and reduced signal swing. New techniques are discussed for logic circuits, memory elements, and interconnects as well as clock and power distribution. ■

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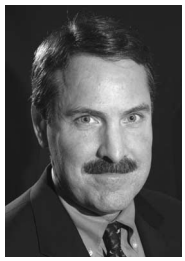
About the Guest Editors

Daniel J. Radack (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Maryland, College Park, in 1983, 1985, and 1989, respectively.

He is a Research Staff Member with the Institute for Defense Analyses, where he studies microelectronics and microsystems technologies. From 1997 to 2001, and again from 2002 to 2006, he was a Program Manager with the Microsystems Technology Office, Defense Advanced Research Projects Agency (DARPA). He managed a series of external research and development programs in high-performance semiconductor technologies. His work focused mainly on silicon-based semiconductors but spanned nearly all aspects from basic materials to design to integration and packaging. He was instrumental in the creation and funding of the Focus Center Research Program and also initiated a number of DARPA research programs that delivered advances in a number of technologies, including silicon-on-insulator, silicon-germanium, and RF CMOS. He also managed programs to advance silicon-carbide power electronics and heterogeneous integration technologies. From 1990 to 1996, he was with Science Applications International Corporation working on development of advanced microelectronic technologies for future defense applications. From 1983 to 1987, he was with the National Bureau of Standards (now the National Institute for Science and Technology) in the Semiconductor Electronics Division, where he developed dynamic test circuits and test structures for very large-scale integration processes.



John C. Zolper (Senior Member, IEEE) received the B.A. degree in physics from Gettysburg College, Gettysburg, PA, in 1982 and the Ph.D. degree in electrical engineering from the University of Delaware, Newark, in 1987.

He is currently the Vice President/Deputy of Corporate Research and Development at Raytheon Corporation where he is involved in strategic planning across a broad range of defense related technologies. Until December 2007, he was the Director of the Microsystems Technology Office (MTO), Defense Advanced Research Projects Agency (DARPA). He was responsible for the conceptual planning necessary to lead MTO into new program areas far in advance of the current state-of-the-art in the areas of electronics, photonics, microelectromechanical systems, component architectures, and algorithms. MTO supports research at the frontier of all of these areas. Previously, he was Deputy Office Director of MTO from September 2002. He joined MTO in October 2001 as a Program Manager. His program responsibilities included managing the Wide Bandgap Semiconductor Technology Initiative program thrust on High Power Electronics and the Technology for Frequency Agile Digitally Synthesized Transmitters (TFAST) program that has developed record-setting InP double heterojunction bipolar transistors and circuits. He is interested in a range of microsystems technologies, including novel semiconductor devices and circuits, ultra-high-speed analog devices, wide-bandgap electrical and photonic devices, high-power electronic components, and photovoltaics. Prior to joining DARPA, he was a Program Officer with the Electronics Division, Office of Naval Research (ONR), where he was responsible for managing ONR's basic and applied research programs in advanced electronics. His programs included several of the premier academic and industrial teams developing group III-nitride and SiC electronics. Prior to joining ONR in 1997, he was a Senior Member of Technical Staff with Sandia National Laboratories, Albuquerque, NM, from 1989 to 1997, where he developed advanced III–V semiconductor processes and devices, including the first GaN junction field-effect transistor. In 1988, he was a Postdoctoral Fellow with the University of New South Wales, Sydney, Australia, working on high-efficiency silicon solar cells. He is the author or coauthor of more than 150 journal and conference papers and seven book chapters, coeditor of one book, and has received five U.S. patents.