IEEE Trans. Circuits Syst., vol. CAS-25, pp. 196–200, Apr. 1978.
[3] C. Wei, "Design of sharp cut-off low-pass maximally flat RC-active filters by cascading third-order blocks," *IEEE Trans. Circuits Syst.*, vol. CAS-27, no. 5, May 1980.
[4] S. A. Boctor, "Design of a third-order single amplifier filter," *IEEE Trans. Circuits Syst.*, vol. CAS-22, pp. 329–334, Apr. 1975.
[5] L. P. Huelsman, "Equal-valued-capacitor active-RC-network realization of a 3rd-order lowpass Butterworth characteristic," *Electron. Lett.*, vol. 7, no. 10, pp. 271–272, May 1971.
[6] S. Tirtoprodjo, "Constraint removal for Huelsman's equal-valued capacitor active RC circuit," *Electron. Lett.*, vol. 7, no. 16, pp. 448–449, Aug. 1971.
[7] G. S. Moschytz, *Linear Integrated Networks Design*. New York: Van Nostrand-Reinhold, 1975, pp. 247–253.
[8] G. S. Beveridge and R. Schechter, *Optimization: Theory and Practice*. New York: McGraw-Hill, 1970, ch. VI, pp. 141–205.

Comment on "Voltage-Controlled Linear Resistor by Two MOS Transistors and its Application to Active *RC* Filter MOS Integration"

L. N. M. EDWARD

Published work (ca. 1984)[1] *claims a "novel" linear MOS resistor circuit comprising two MOS transistors in parallel, well suited to recent fabrication technology developments. This letter reports early work (ca. 1967) for the same circuit, and an alternative series circuit. Theoretical development is applied to an analog multiplier.*

I. Introduction

I refer to the letter by S. Han and Song B. Park.[1] I must inform the profession that the essential feature of their circuit, a "linear" resistor employing a parallel connection of two MOS transistors (MOST), was invented by me in late 1967 while I was employed by The Plessey Company Limited, at Roke Manor, Romsey, Hampshire, England. On January 16, 1968, a patent application was filed and British Patent No. 1251671 granted on January 17, 1969. The 1978 Patents Act (UK) provided for 20 year patent-life requiring annual renewal fees. Along with many other minor patents, Plessey decided not to maintain this one which is now in the public domain. The circuit idea presented by Han and Park is, therefore, unprotected and unpatentable.

Another recent independent discovery of this compensation method will be found in [1].

To complete the record I will now briefly outline some results from my 1967–1968 work.

II. Applications

The accompanying figures, 1–6, are reproduced from the patent. Figs. 1–3 are self-explanatory, being simply the normal, diode-connected, and parallel-compensated connections. In Fig. 3(a), R is just a resistance by which to convert the combined normal and diode currents to a voltage for observation on a CRO. Ideally, R is as near to zero as possible. An operational amplifier summing junction is ideal at low frequency.

The circuit of Fig. 4 illustrates one half of a balanced modulator, possibly realized in a simple integrated circuit. Thick film would be the appropriate technology. R_1 and R_2 form a voltage divider to reduce the signal coupled from drains to Q_2 gate; Q_2 having slightly greater beta so that by trimming R_1 the compensation can be optimized. Here, beta $= (e_{ox}uW)/(LT_{ox})$ where e_{ox} and T_{ox} are, respectively, the gate oxide permittivity and thickness, W and L the channel width and length, and u the mobility of carriers in the channel.

In Figs. 5 and 6, a series-compensation method of linearizing MOST low-level characteristics is not so successful as the parallel-compensation method, but it has the advantage that existing dual-gate MOSTs can be used.

These techniques are not limited to low frequencies associated with operational-amplifier circuits. My main objective was to find a way to realize high-frequency mixers exhibiting a wide dynamic range together with superior intermodulation performance. Fig. 8 shows the spectrum of a doubly balanced untuned mixer employing two parallel-compensated MOST resistors (four MOSTs). Two 50-mV rms local-oscillator antiphase sinusoids drive the gates of the normal MOSTs at 117 MHz, while two antiphase 33-MHz sinusoids

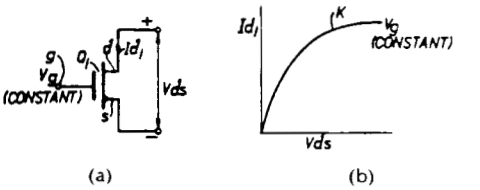


Fig. 1. Normally connected MOST.

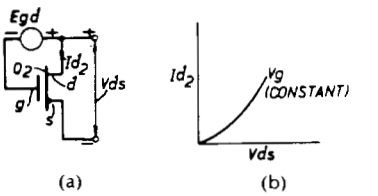


Fig. 2. Diode connected MOST.

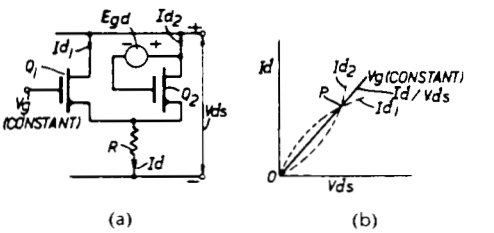


Fig. 3. Parallel compensation connection.

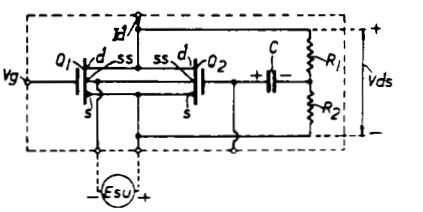


Fig. 4. Half of balanced modulator: practical circuit.

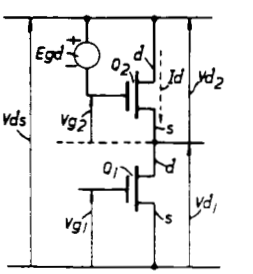


Fig. 5. Series compensation: principle.

Manuscript received January 29, 1985; revised October 22, 1985.
The author is with the University of Canterbury, Christchurch 1, New Zealand.
[1] S. Han and S. B. Park, *Proc. IEEE* (Lett.), vol. 72, no. 11, pp. 1655–1657, Nov. 1984.

0018-9219/86/0500-0753$01.00 ©1986 IEEE

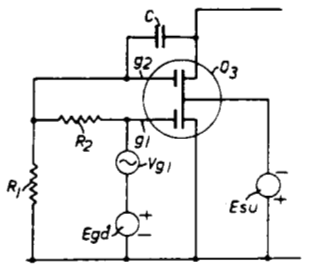


Fig. 6. Series compensation: dual-gate MOST.

are applied to the common drains. Currents are summed in the emitter of a common-base amplifier driving a 50-Ω coaxial line to the spectrum analyzer. After 18 years I cannot recall the precise circuit detail and my data come from material that was prepared for in-house presentations and minor symposia.

Other work investigated the balanced modulators as broad-band frequency doublers, and triode MOSTs as square-law frequency doublers. Cascaded and untuned, square-law doublers gave useful multiplication of up to 8 times for output frequencies up to 30 MHz. At that time, no doubler tests were performed at higher frequencies because of time and equipment limitations.

III. Simple Theory

In 1967, MOSTs were just becoming commercially available and reliable enough to use in analog circuits. The work involving dual-gate MOSTs used RCA type TA7010 while that on parallel compensation used TRW type PT201, RCA TA2840 (3N128), or n-channel enhancement type 2N4038.

All theoretical work was based on the gradual-channel model, SAH (1964) [2], which, for the large geometries then in use, adequately predicted the test results, and encouraged its use in design.

My analysis of the series-compensated (or dual-gate) MOST is too complicated to present here, but the parallel-compensation theory is quite straightforward.

Consider Fig. 3(a). The gradual-channel approximation is well known, so for negligibly small R

$$I_{d1} = B_1\left[\left(V_{g1} - V_{t1}\right)V_{ds} - \frac{V_{ds}^2}{2}\right] \tag{1}$$

$$I_{d2} = B_2\left[\left(V_{ds} - E_{gd} - V_{t2}\right)V_{ds} - \frac{V_{ds}^2}{2}\right] \tag{2}$$

where

B_1 Q_1 beta
B_2 Q_2 beta
V_{g1} Q_1 gate-to-source voltage
V_{t1} Q_1 strong-inversion threshold voltage
V_{t2} Q_2 strong-inversion threshold voltage
E_{gd} Q_2 drain–gate bias voltage
V_{ds} total drain–source voltage.

Simplifying (2) gives

$$I_{d2} = B_2\left[\left(-E_{gd} - V_{t2}\right)V_{ds} + \frac{V_{ds}^2}{2}\right]. \tag{3}$$

Now, if the normal and diode-connected MOSTs are placed in parallel so that their drain (or source) currents add, then

$$I_d = I_{d1} + I_{d2}$$

$$= \left[B_1\left(V_{g1} - V_{t1}\right) + B_2\left(-E_{gd} - V_{t2}\right)\right]V_{ds} + \frac{V_{ds}^2}{2}\left(B_2 - B_1\right). \tag{4}$$

Thus by making $B_2 = B_1$ we may eliminate the second-order dependence of I_d on V_{ds} independently of E_{gd} provided both Q_1 and Q_2 remain conducting and $V_{ds} < (V_{g1} - V_{t1})$ under peaks of the signals on gates and drains.

Let $V_{g1} = f_1\{t\}$ and $V_{ds} = f_2\{t\}$ then, since V_{t1} and V_{t2} are constants (for constant substrate bias) the output, for these input signals, is given by

$$I_d\{t\} = k_1 f_1\{t\} f_2\{t\} + k_2 f_2\{t\}. \tag{5}$$

If a balanced arrangement is used, as shown in Fig. 7, then $V'_{g1} = -f_1\{t\}$ and $V'_{ds} = -f_2\{t\}$ so that

$$I'_d\{t\} = K_1[-f_1\{t\}][-f_2\{t\}] - K_2 f_2\{t\}. \tag{6}$$

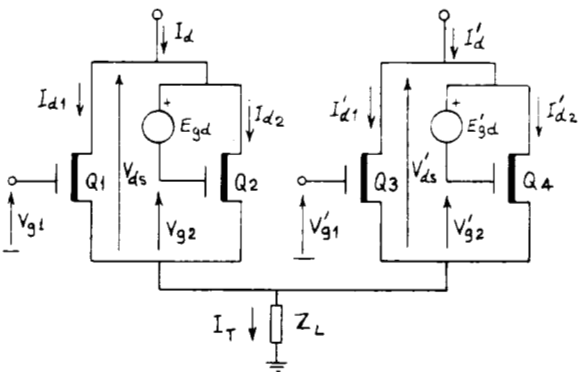


Fig. 7. Balanced multiplier.

Now, summing the total current $I_T = I_d + I'_d$ by connecting the sources to a low-impedance load Z_L we obtain

$$I_T\{t\} = (K_1 + k_1) f_1\{t\} f_2\{t\} + (k_2 - K_2) f_2\{t\} \tag{7}$$

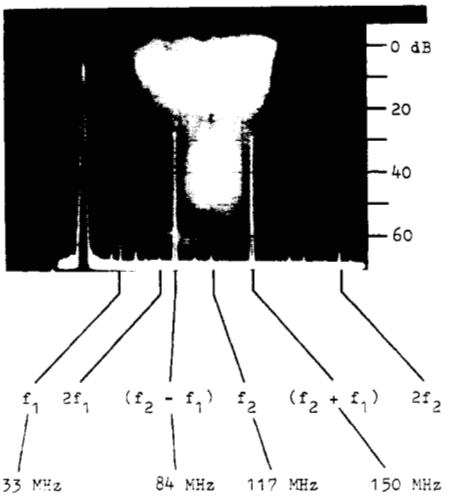
where the subscripts refer to $Q_{1,2,3,4}$ while the $k_{1,2}$ and $K_{1,2}$ are functions of $Q_{1,2,3,4}$ and their biasing.

Thus by appropriate choice of the bias conditions, we may balance the multiplier to the signal $f_2\{t\}$ by making $k_2 = K_2$ and so reduce the term $(k_2 - K_2)f_2\{t\}$ to zero without affecting the second-order cancellation conditions of (4), to yield, because of the symmetry between Q_1 and Q_2 (and Q_3 and Q_4), a bipolar multiplier which in practice is nearly linear.

In principle, a triode MOST is symmetrical because the source and drain are interchangeable, except for many discrete packaged MOSTs which have the source internally connected to the substrate and, being of annular geometry with the drain innermost to minimize parasitic drain currents, must be approached with caution if employed in these linearized modes. But no such restriction exists for the custom circuit designer to whom these comments are mainly directed. When V_{ds} is made negative, circuit operation is unchanged except that the roles of Q_1 and Q_2 are exchanged such that Q_1 now has feedback from "drain" to gate while Q_2 is in common-"source" configuration. The inference here is that the MOST gates and drains are driven by low-impedance generators, and the drain currents are summed in a low-impedance load. Failure in this respect will degrade multiplier linearity, even though the MOST resistors themselves may be perfectly linear.

Because the substrate exerts a gating action (as in a junction FET) via the channel–substrate depletion region, the substrate should be reverse-biased with respect to the channel so as to reduce the nonlinearity which will result from consequential variation of the strong-inversion thresholds V_{t1} and V_{t2} as the mean channel potential varies with $f_1\{t\}$ and $f_2\{t\}$. Another reason for this bias is to increase the permissible drain voltage swing before the source- or drain-substrate diodes become forward-biased with consequent catastrophic effects on the MOST resistor or multiplier linearity.

The operation of MOSTs is based upon surface inversion layers, and the effect of depletion charge cannot really be neglected as it has been in the gradual-channel approximation [3]. The effect, in an n-channel MOST, of increasing the substrate doping is to shift the strong-inversion threshold in a positive direction and to reduce the drain pinchoff voltage. Clearly, a lowered pinchoff voltage is an advantage when the MOST is used as an amplifier in the saturation region but undesirable for a voltage-controlled linear resistor because the drain voltage range over which compensation is possible is progressively reduced as the substrate doping increases. Thus for a given peak signal at the drains, residual nonlinearity may be expected to increase with the doping level. Typical NMOS processes



DRAIN SIGNALS: each 50 mV rms to earth.
V_{ds} = 0 Volts dc.
GATE SIGNALS: each 50 mV rms to earth

SPECTRUM:

	0 Hz	
	external interference	
(1)	f_1	33 MHz
(3)	f_2-2f_1	51 MHz
	external interference	
(2)	$2f_1$	66 MHz
(2)	f_2-f_1	84 MHz
	external interference	
(1)	f_2	117 MHz
(2)	f_2+f_1	150 MHz
(3)	f_2+2f_1	183 MHz
(3)	$2f_2-f_1$	201 MHz
(2)	$2f_2$	234 MHz

Fig. 8. Output spectrum of doubly balanced untuned mixer.

use starting material doped at about 10^{15} to 10^{16} cm^{-3}, leaving limited scope for linearity improvement with typical enhancement MOSTs. A second implant, almost compensating the substrate doping, may in future be possible for just these MOSTs, if the additional mask cost can be justified. Meanwhile, standard depletion devices must serve. CMOS processes, which have lower gate-threshold voltages and are much more suitable for analog (linear) circuits than are NMOS, may be more promising in this respect and should be fully investigated. Silicon-on-insulator MOSTs, exhibiting no body effect, may show much improved linearity. The recently announced MOSFET structure [4], which has polysilicon gates above and below a thin (200-nm) recrystalized silicon channel region, should also exhibit no body effect and may be the most promising yet. One of the gates could connect to the drain to form the compensating MOST while the other gate is used to control the MOST resistor.

References

[1] J. N. Babanezhad and G. C. Temes, "A linear NMOS depletion resistor and its application in an integrated amplifier," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 932–938, Dec. 1984.

[2] C. T. Sah, "Characteristics of the metal-oxide-semiconductor transistors," *IEEE Trans. Electron Devices*, vol. ED-11, pp. 324–345, July 1964.

[3] J. A. Van Nielen and O. W. Memelink, "The influence of the substrate upon the dc characteristics of silicon MOS transistors," *Phillips Res. Rep.*, vol. 22, pp. 55–71, 1967.

[4] C. L. Cohen, "New FET design could speed the arrival of 3-D circuits," *Electronics*, vol. 58, no. 36, p. 14, Sept. 9, 1985.

Vector-Radix Algorithm for a 2-D Discrete Hartley Transform

R. KUMARESAN AND P. K. GUPTA

A new multidimensional Hartley transform is defined and a vector-radix algorithm for fast computation of the transform is developed. The algorithm is shown to be faster (in terms of multiplication and addition count) compared to other related algorithms.

Manuscript received August 15, 1985. This research was supported by ONR under Contract N00014-84-K-0094.

The authors are with the Department of Electrical Engineering, University of Rhode Island, Kingston, RI 02881, USA.

I. Introduction

The two-dimensional (2-D) discrete Fourier transform (DFT) is an important tool in digital signal processing. It is defined as

$$y(k_1,k_2)=\sum_{n_1=0}^{N-1}\sum_{n_2=0}^{N-1}y(n_1,n_2)W_N^{n_1k_1}W_N^{n_2k_2},$$

$$k_1,k_2=0,1,\cdots,N-1. \quad (1)$$

A standard method for computing the transform is via the row–column decomposition [1], which takes advantage of the separability of (1). That is, the 2-D transform is broken up into two 1-D transforms, computed in a row–column or column–row wise format. If the fast Fourier transform (FFT) is used to evaluate the 1-D DFT, then the number of complex multiplications required is $N^2 \log_2 N$. In addition it needs a matrix transposition algorithm. Further, savings in the number of multiplications is achieved by using the vector-radix method due to Rivard [2], [3]. In this method, a 2-D DFT is broken down into successively smaller 2-D DFTs until, ultimately, only trivial 2-D DFTs need to be evaluated. The number of complex multiplications now is $3/4\ N^2 \log_2 N$ [2], [3], which is 25 percent lower than row–column decomposition. In many important applications the input data are real-valued. In such cases, a disadvantage of the above algorithms is the need for complex-arithmetic and storage of complex values.

Bracewell [4], [5] recently proposed a real 1-D transform called the discrete Hartley transform (DHART) which is defined below. (The abbreviation DHT is used for Hilbert transform)

$$y_H(k)=\sum_{n=0}^{N-1}y(n)\left(\cos\frac{2\pi nk}{N}+\sin\frac{2\pi nk}{N}\right),$$

$$k=0,1,2\cdots,N-1. \quad (2)$$

This transform is related to the DFT, but with two important differences [4]. Since it is a real transform it uses only real arithmetic. Secondly, the inverse DHART is identical to the DHART, but for a scale factor. That is

$$y(n)=N^{-1}\sum_{k=0}^{N-1}Y_H(k)\left(\cos\frac{2\pi nk}{N}+\sin\frac{2\pi nk}{N}\right),$$

$$n=0,1,2\cdots,N-1. \quad (3)$$

If DFT needs to be calculated, it can be obtained from the DHART by using the formulas [4], [5]; $\mathrm{Re}(Y(k))=1/2(Y_H(k)+Y_H(N-k))$ and $\mathrm{Im}(Y(k))=-1/2(Y_H(k)-Y_H(N-k))$, where $Y(k)$ is the DFT of $y(n)$. Bracewell [5] also proposed a radix-2 Cooley–Tukey type fast transform for calculating the DHART. In [6], a prime-factor algorithm for calculating (2) is given. A related prime-factor decomposition using real arithmetic is due to Parsons [7].

An extension of the 1-D DHART to 2-D is as follows (the m-D

0018-9219/86/0500-0755$01.00 ©1986 IEEE