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Scanning the Issue

THE SPECIAL ISSUE ON VLSI DESIGN: PROBLEMS AND TOOLS

"THE DEVELOPMENT of semiconductor devices has depended upon a synergism with computers. This is particularly true for integrated circuits, whose development was motivated by the computer applications. With each advance in components, the computers resulting from their use reached a wider market, motivating further advances in the semiconductor technology" [1]. The synergism stressed in the above quotation goes even further; the development of components depends on the extensive use of computers. In turn, more powerful computers can be built, which are required for the development of next-generation components, and so on. This is particularly true for the development of of very-large-scale integrated circuits (VLSI). The complexity of such parts can be handled only with ever improved and extended computer-aided design (CAD).

While CAD is an explosively growing area in many engineering disciplines, VLSI-CAD is certainly the most widely used and best developed CAD branch [2]. New CAD tools are continually developed in order to cope with the ever increasing problems of VLSI complexity. Since this development is in full swing now, the interested reader may appreciate this Special Issue of the PROCEEDINGS OF THE IEEE on "VLSI Design: Problems and Tools."

The bristling richness of this rapidly emerging field unfolds in this issue with 14 authoritative papers covering practically every significant aspect. In the opening paper, M. Feuer sets the scene with a historical sketch, a comprehensive description of the state of the art, and an outline of key current problems.

The second paper by W. L. Engl, H. K. Dirks, and B. Meinerzhagen is on device modeling. As the complexity of the technology grew, optimization of devices through "trial and error" became more and more inefficient. Gradually, this crude method was replaced and complemented by device modeling in order to predict the properties of the devices in advance of the production of expensive hardware. This paper deals in detail with the various aspects of device modeling and its significance for the device designer and the circuit engineer, stressing especially the importance of numerical approaches.

With the next two papers the issue proceeds to larger units, namely circuits and logic networks. The paper by A. E. Ruehli and G. S. Ditlow is a review of circuit analysis, logic simulation, and design verification, including time analysis. J. P. Avenier, on the other hand, concentrates more on layout technologies, including digitizing and rule checking. The most frequently used methods are described, compared, and rated.

The interconnection of components in VLSI chips is becoming an increasingly complex problem. In their paper, S. J. Hong and R. Nair discuss several approaches to solving this problem with emphasis on special wire routing machines. With such machines the wire routing time can be reduced significantly; their use in the design of future VLSI chips may become mandatory. Whether there should be many machines, each of which specializes in some aspect of VLSI physical design automation, or a "consensus" machine that can be used for most of the critical computational needs, is an emerging question. Hierarchical design methods—as compared to automated design approaches—offer an alternative means of managing the VLSI-design problem. In his paper, C. Niessen discusses in detail the methodology of hierarchical design approaches, including their advantages and disadvantages.

The use of computers to design newer computer systems automatically has been a dream of computer system designers since the early days of digital computers. In his paper, S. G. Shiva surveys several automatic synthesis systems which could be considered steps toward this goal. None of the systems proposed and developed so far is completely automatic. Human interaction of varying degree is needed to guide the synthesis process. One significant conclusion the author draws is that it may not be practical (and even not desirable) to make the synthesis completely automatic. Some methodical aspects of logic synthesis are discussed in H. M. Lipp's paper. The author especially compares top-down with bottom-up optimization Lipp predicts that in the VLSI era the bottom-up optimization approach will lose influence in favor of new top-down design tools for logic synthesis.

With the emerging VLSI technology, it has become apparent that considerable care will have to be taken in the design stage in order to ensure testability. In the paper by T. W. Williams and K. P. Parker, the various concepts to serve this purpose are

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described and compared. Their advantages and disadvantages are discussed.

Contrary to most of the papers listed so far—which cover fairly broad topics—the following paper by D. I. Moldovan concentrates on the rather specialized subject of mapping cyclic loop algorithms into special-purpose VLSI arrays. Such arrays can be used to construct systems with a high level of parallelism. The potential and the problems of this approach are discussed in detail. The concept is not restricted to VLSI systems; it can also be used for mapping algorithms into other fixed parallel computer architectures.

CAD tools for IC processing are being used as aids in developing new technologies. A. R. Neureuther's paper gives an overview of such tools, particularly for topography effects in lithography, etching, and deposition. Such tools are helpful, especially for complex tradeoffs between conflicting physical mechanisms in multistep processing sequences.

The next paper reviews the historical aspect of the CAD systems developed for IC design and manufacture in Japan. It describes the current status of VLSI-CAD systems and technologies, from device to system levels. It comprises the description and evaluation of most of the respective CAD tools used in Japan and discusses the standardization issue, which has become indispensable for the efficient usage of the various CAD resources. It is followed by the paper of A. B. Bhattacharrya, dealing with VLSI problems in the developing countries and their various options of VLSI-technology acquisition. While the author chooses to illustrate those topics with India as an example, most of his findings relate in similar manner to other developing countries. The discussion reveals that the realities of the developing nations are heavily weighted against a rapid adoption of microelectronics technology. But a gradually increasing awareness of the downstream application of VLSI chips in basic tools will soon evolve in these countries.

The issue closes with a review by C. H. Sequin with the future-oriented title: "Managing VLSI Complexity." The positive aspects of VLSI complexity as a way to increase performance and reduce chip size are presented. The changing role of the designer is discussed in view of the increasing use of automatic and semiautomatic tools. Recommendations are made for the education of next-generation designers with skills to enable them to cope with the increasing VLSI complexity.

This Special Issue will serve its purpose if the reader deepens his understanding of the problems associated with VLSI design and if he receives some insights into the various tools (available and emerging) developed for the future evolution of VLSI.

Finally, the reader interested in continuing coverage of this subject should note that the IEEE Circuits and Systems Society publishes the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS. The first issue of this quarterly journal appeared in January 1982.

REFERENCES

[1] R. N. Noyce, *Computer*, p. 26, Dec. 1976.
[2] *Proc. IEEE* (Special Issue on Computer-Aided Design), vol. 69, pp. 1187–1376, Oct. 1981.

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Guest Editor

Otto G. Folberth received his degree in physics and the Dr.rer.nat. degree from the Technical University in Stuttgart, Germany, in 1951 and 1952, respectively.

From 1952 to 1960 he was with the Research Laboratory of the Siemens-Schuckert-Werke AG in Erlangen, Germany, working in the field of semiconductor compounds. Numerous publications and patents originated during this period. In 1961 he joined IBM Deutschland GmbH in Boeblingen, Germany, where he became instrumental in the buildup of a semiconductor research and development facility. This department formed the nucleus for the manufacturing organization of silicon components at IBM in Germany, an activity which comprised a substantial part of the total manufacturing operation of the company in the years to follow. His development department designed and piloted a multitude of advanced IC's, used worldwide in many IBM systems of several generations. In addition to his managerial duties, he performed several part-time jobs internally and externally. Since 1968, during each summer semester he has served as a Part-Time Lecturer at the University of Stuttgart, Stuttgart, Germany, teaching courses in "Technology of Integrated Semiconductor Circuits." In 1974 he was appointed an Honorary Professor at this University. In 1974, he was appointed an IBM Fellow. In 1978 and 1979 he was a member of IBM's Corporate Technical Committee, IBM's supreme technical advisory board. Currently, he is Manager of the Component Technology organization at the IBM Laboratory in Boeblingen. Professionally, he is interested in the social implications of microelectronics and the limitations of this technology.

Dr. Folberth is member of several national and international scientific and technical societies, in which he participates actively. Especially, for several years he was the Chairman of a steering-committee for the organization of solid-state scientific and engineering conferences in Europe. Further, he was Secretary (1971–1972) and Chairman (1973–1975) of the European Group of the Program Committee for the International Solid State Circuits Conference (ISSCC).