Scanning the Issue

Special Issue on Low-Power RF Systems

Major advances in low-power RF system design over the past decade have enabled a broad spectrum of new and exciting wireless applications that range from low-performance systems such as ID tags, sensors, and location identification devices to high-performance systems that communicate voice, data, and multimedia information. These advances have been enabled by a systems view of the communication problem rather than simply focusing on the basic component technology. This special issue highlights the integrated approach required for the design of low-power RF systems and includes the optimization of the underlying technology and circuit fabrics, radio architectures, communication protocols, and design tools.

Virtually all wireless systems are driven by bandwidth and energy constraints—two resources that are particularly scarce when compared to a tethered environment. However, the approach to RF module design can vary dramatically based on the specific system requirements dictated by the application. For example, the communication rates can vary from a few bits per second for low-rate sensor applications to a few megabits per second for multimedia traffic. This impacts the design of communication fabrics from a low power perspective. Similarly, the required communication latency can have a big impact on the choice of networking protocols. To operate with the minimal possible energy, the radio system must exploit these application-specific attributes instead of designing for general specifications.

The design of RF systems requires optimization at all levels of the system hierarchy—from high-level communication protocols and algorithms down to architectures and physical design. At the highest level, the communication protocols (the multiple-access and link-layer protocols) must be optimized from an energy perspective. For example, in low-rate sensor applications, it is important to create protocols that force the nodes into the sleep state as much as possible to conserve energy. With the growth of home and office networking, there is also a need to construct protocols that support *ad hoc* networking of devices. The communicating devices must also optimally trade off computation and communication. As technology scales, the energy costs of computation will continue to scale down, while fewer gains are expected in communication energy requirements. In many systems, it is possible to take advantage of this by performing more computation to reduce the amount of required communication. At the lowest level, the basic architectures and circuit fabrics must be optimized for low power. This includes decisions such as the location of the A/D in a receiver, required sampling resolution, the choice of component circuit topologies, etc. All of those topics are covered in this issue.

The first few papers in this issue describe the physical layer electronics for low-power RF communication. In "Power-Conscious Design of Wireless Circuits and Systems," Abidi *et al.* address power minimization in wireless systems through appropriate design of both circuits and systems. They use, as examples, radio paging and low-rate distributed microsensors in dense wireless networks—communication nodes that must operate for years using a very small power source. The authors present a systematic approach to power minimization. First, some fundamental relationships are established between the current consumed and the dynamic range of low-noise amplifiers, mixers, oscillators, and filters. This allows a designer to make appropriate tradeoffs between power and required performance. They then show how the pattern in which these devices communicate, that is the communication protocol, can be architected to improve system lifetime. They overview several power aware multiple-access schemes and routing strategies. The authors describe the issues with trading off computation and communication costs. The techniques presented in this paper will find broad application in emerging wireless communication systems.

Baltus and Dekker, in the second paper, "Optimizing RF Front Ends for Low Power," also attack the problem of power minimization in RF circuits. They focus on the front end of the radio transceiver, which often dominates the overall power dissipation. The authors present a simple model that links optimized front-end power dissipation to linearity, gain, and noise, as well as power-efficiency parameters for each of the front-end subcircuits. The front-end power dissipation is reduced through careful system design (e.g., transceiver architecture, partitioning, antenna interface, and diversity schemes) and by improving the power efficiency parameters of the subblocks. A key to power reduction involves reducing the influence of the IC substrate. The authors present

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silicon-on-anything (SOA), an IC technology that eliminates the influence of the substrate in a simple way while maintaining compatibility with standard silicon processing. They demonstrate that the power dissipation using SOA can be reduced by an order of magnitude for bandwidth-limited circuits. The "on-anything" concept can be extended to other IC processes as well, such as CMOS and BiCMOS.

The next three papers in this issue deal with the design of RF circuits for 5-GHz frequencies. In "CMOS RF Integrated Circuits at 5 GHz and Beyond," Lee and Wong describe the design considerations and solutions for wireless networks that operate above 5 GHz. They particularly focus on the issues related to device scaling in CMOS technology and with the quality of on-chip passive components such as spiral inductors, varactors, and transmission lines. This paper considers how these issues affect the design of key RF building blocks, such as low noise amplifiers, oscillators, filters, and frequency synthesizers. The losses at high frequency increase significantly, but are mitigated by the trend toward more interconnect layers. The authors discuss the advantage of coplanar transmission lines and provide projections of CMOS technology for frequencies well beyond 5 GHz. Based on several fabricated high-frequency prototype circuits in standard submicron CMOS, the authors demonstrate that, despite its deficiencies, scaled standard CMOS enables wireless applications well beyond 5 GHz. This will enable the use of high-carrier frequency ISM bands that have significant available spectra.

"Low-Power Multi-GHz and Multi-Gb/s SiGe BiCMOS Circuits," by Soyuer *et al.*, also describes the design of RF circuits for carrier frequencies above 5 GHz. However, the authors focus on the use of SiGe HBT BiCMOS technology for realizing high-frequency RF circuits. Advances in SiGe process technology has extended silicon-based production technology well into the multigigahertz range, opening up an array of wireless network applications and markets. SiGe circuits are being designed in the same space as GaAs MESFETs and HBTs, and potentially offer the yield, cost, stability, and manufacturing advantages associated with conventional silicon fabrication. A variety of RF and microwave circuits are described, including low-voltage, low-noise amplifiers and fully monolithic voltage-controlled oscillators (VCOs) and phase-locked loops (PLLs). The authors present different circuit applications of SiGe BiCMOS technology and describe the performance and power improvements that can be obtained by its employment in highly integrated RF and microwave circuit designs.

The next paper, "Chip-package Codesign of a Low-Power 5-GHz RF Front End," by Donnay *et al.*, describes a package-level integration methodology for implementing high-performance RF circuits. In current RF systems, there are a significant number of external passive components. The authors of this paper claim that single-package integration of complete transceivers based on a multichip module (MCM) technology with integrated passives is a superior alternative to single-chip CMOS integration for low-power wireless communication applications. However, in order to benefit from all the advantages offered by this integration approach, a careful codesign of the active circuits and the integrated passives in the MCM technology is necessary. As a demonstration, the authors present a "system-on-a-package" approach for a Digital European Cordless Telephone (DECT) application and a 5-GHz WLAN front end. These implementations demonstrate the improvements that are possible in system integration and power dissipation for complete RF transceivers.

"Design Considerations for Minimal-Power Wireless Spread Spectrum Circuits and Systems," by Myers *et al.*, describes the design considerations associated with developing a complete low-power wireless LAN system based on spread spectrum modulation techniques. The paper presents the application of wireless technology to the home/office environment with emphasis on the IEEE 802.11 standard. A systems view is taken, demonstrating that power minimization requires optimization at all levels of design, including the system topology, protocol, and radio architecture, and the low-level circuits. Operational requirements such as range, immunity to interference and multipath effects, effective payload rate, and robustness in multiuser applications are also discussed relative to power constraints. Emphasis is also placed on power dissipation driven system partitioning, including a discussion of radio architectures and optimum placement of the analog-to-digital interface. The paper demonstrates that the choice of protocols has the biggest impact on minimizing power dissipation as they enable the transceivers to sleep for a maximum amount of time.

In "A Design System for RFIC: Challenges and Solutions," Miliozzi *et al.* present an innovative framework for the design of RF circuits and systems. The authors describe the computer-aided design (CAD) tools necessary to estimate the performance of an RF circuit, including layout and package parasitic effects. When the circuits are pushed to their performance limits, it is necessary to take all the nonlinearities and second-order effects into account. The design system allows information exchange and interaction between the process development, device modeling, IC design, package development and modeling, parasitic prediction and extraction, and layout design with the goal of minimizing both power consumption and time to market. The authors give a detailed overview of the methods that are currently used for simulation and noise analysis. The generation of RF layout is also presented in detail, as this has a considerable impact on the overall performance. To demonstrate the use of the tools, an example RFIC design is provided for use in the 2.4-GHz band. The use of CAD tools will become very critical, especially as the frequency scales above 5 GHz.

"Advanced Signal-Processing Algorithms for Energy-Efficient Wireless Communications," by Luschi *et al.*, covers an important area of signal-processing algorithm design for wireless communication. In cellular systems such as GSM, one of the key system design objectives in the base station is the maximization of the receiver sensitivity so that the required signal level from the mobile terminals can be minimized. Advanced signal-processing algorithms based on maximum *a posteriori* (MAP) estimation, iterative

(turbo) channel estimation, equalization, and decoding allow for a reduction of the required transmitter power by one-third to one-half. The authors also present techniques to reduce computational complexity of the mobile units for a fixed quality of service (QoS). The idea is to adapt the state complexity of the data estimator to the propagation channel. The algorithms can significantly reduce the computational load of a typical mobile receiver, which implies a decreased power drain on the digital circuits. The signal-processing algorithms that are presented have potential application in different standards, including next-generation time division multiple access (TDMA) wireless systems, and provide the flexibility of designing the best tradeoff between power consumption and QoS.

The final two papers address an important new trend that deals with the design of low-power *ad-hoc* wireless networks. They present two different standards for interconnecting appliances over short distances. "Bluetooth—A New Low-Power Radio Interface Providing Short-Range Connectivity," by Haartsen and Mattisson, describes the protocol architecture for Bluetooth, a complete interface specification for wireless connectivity. The primary objective is minimizing cost and power, with the goal of embedding a radio in every electronic appliance. The protocols are highly optimized from an energy perspective and support setup of the network and communication between different devices. Bluetooth uses the 2.45-GHz frequency band, and each unit can simultaneously communicate with up to seven other units in a piconet. The protocol uses frequency hopping and supports both synchronous links suited for circuit-switched applications like voice communications and asynchronous links suited for packet-switched applications like data. The standard has received broad support and will move toward eliminating the need for wires between cordless or mobile phones, modems, headsets, PDAs, computers, printers, LANs, etc., and paves the way for new and completely different devices and applications.

The final paper, "The Design and Implementation of HomeRF: A Radio Frequency Wireless Networking Standard for the Connected Home," by Lansford and Bahl, describes HomeRF, a wireless networking standard for the home. The HomeRF group has developed an open specification, the Shared Wireless Access protocol (SWAP), that enables RF wireless connectivity between a diverse set of devices and computing resources in and around a typical home. Built around an RF spectrum with worldwide availability, SWAP provides operational support for both managed and *ad hoc* networking of devices. When configured as a managed network, it combines and extends wireless networking and cordless telephony into a single unified protocol, allowing mobile devices to communicate via both voice and data traffic simultaneously. The architectures use a built-in power management algorithm that ensures connection longevity for battery-constrained devices. The authors discuss design decisions and provide detailed descriptions of the network architecture, the channel access protocol, power management algorithms, and technical issues concerning the deployment of SWAP. Similar to Bluetooth, the technology has cost as a primary objective to enable tetherless home networking.

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