Compact Modeling Session 11

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As CMOS technology continues its relentless scaling, new materials are being introduced and novel device structures are being considered. Adequate compact models and simulation techniques are required to account for their impact on circuit characteristics. This session showcases several examples in compact model development, enhancement, and application in connection with the latest technology advances.

The first, invited paper from University of California, San Diego presents a generalized analytical model for multi-gate MOSFETs of various configurations. Fully equipped with quantum- and short-channel effects and terminal charges expressions, the new model has been calibrated and validated by FinFET hardware. The paper also provides a brief review of the overall research activities on multi-gate MOSFET modeling.

The second, invited paper is a joint work from AMD, IBM and Freescale on partially depleted (PD) silicon-on-insulator (SOI) MOSFET model. It presents SOI-specific challenges in SOI MOSFET modeling, parameter extraction, and circuit simulation. The current status of the next-generation SOI model standardization process by Compact Model Council is briefly reviewed.

The third, invited paper from Arizona State University presents an analytical model of ionizing radiation effects on bulk CMOS transistors and integrated circuits that takes into account non-uniform defect distributions through surface potential equations. The new model leads to identification of sidewall doping as the primary technology feature to drive increased radiation tolerance in advanced deep-submicron bulk CMOS.

The fourth paper from IBM describes a new approach to characterize and model FET source/drain diffusion resistance by incorporating electric current trajectory information. The new model is verified with field solver simulations over various parameter values and validated by hardware data from a 65 nm SOI technology.

The final paper from Georgia Tech develops a hybrid technique using hardware-based mobility measurement and device electrostatic simulations to analyze the impact of interfacial oxide thickness variations on metal-gate high-K circuits. It is shown that the interfacial oxide thickness variation needs to be effectively controlled to reduce circuit variability and fully exploit the advantage of metal gate high-k technologies.

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