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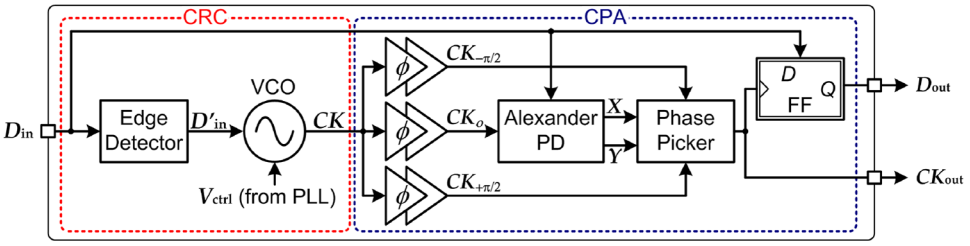

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20-GSample/s (10 GHz × 2 Clocks) Burst-Mode CDR Based on Injection Locking and Space Sampling for Multiaccess Networks

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(Invited Paper)

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Abstract: In this paper, we demonstrate a novel 20-GSample/s burst-mode clock and data recovery (BM-CDR) technique for optical multiaccess networks. The BM-CDR incorporates an injection-locking method for clock recovery and a clock phase aligner employing space sampling with two multiphase clocks at 10 GHz and a phase-picking algorithm for automatic clock phase acquisition. The design provides low latency and fast response without requiring a reset signal from the network layer. The BM-CDR achieves a bit error rate $< 10^{-10}$ while featuring instantaneous (0-bit) phase acquisition for any phase step $(\pm 2\pi$ rad$)$ between successive bursts. We also compare the data with probabilistic theoretical predictions to validate the experimental results.

Index Terms: Access networks, burst mode (BM), clock and data recovery (CDR), clock phase aligner (CPA), injection locking, probabilistic theory, space sampling.

1. Introduction

The past decade has seen profound changes not only in the way we communicate but also in our expectations of what networks will deliver in terms of speed and bandwidth. More specifically, the explosive growth in Internet traffic has spurred the development of fiber-to-the-home (FTTH) systems for high-speed broadband access [1], [2]. Among them, passive optical network (PON) is recognized as the most economical FTTH solution to alleviate the bandwidth bottleneck in access networks [2], [3]. PON standards based on time-division multiplexing (TDM) such as the IEEE 802.3ah gigabit ethernet PON (GEPON) [4] and ITU-T G.984 gigabit-capable PON (GPON) [5] have already been widely deployed worldwide; FTTH rollout has recently surpassed 30 million users on the globe and is continuing to grow at a rapid rate [6]. The coming decade promises to demand more capacity and bandwidth in these networks. In this context, the IEEE802.3av 10G-EPON [7] has recently been standardized to attain a total bandwidth of 10 Gb/s. Related research activities are being aggressively pursued [8], [9] due to 10G-EPON inherent cost-effective user-shared

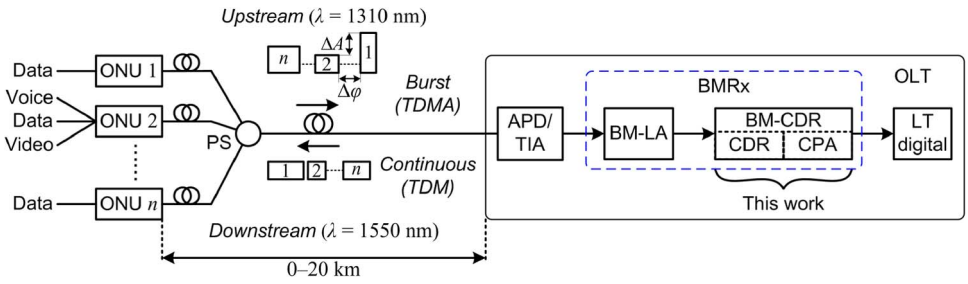

Fig. 1. Generic PON for FTTH showing our work on BM-CDR in context (APD: avalanche photodiode; BM-LA: BM limiting amplifier; BMRx: BM receiver; PS: power splitter; TIA: transimpedance amplifier).

configuration, good backward compatibility, and smooth upgradability from GEPON. It is no longer a question of "if" 10G-EPON holds great promise for next-generation optical access networks (NGA), it is a question of "when."

Fig. 1 is a schematic of a PON system showing our study in context. In the downstream direction, continuous data are broadcast from the optical line terminal (OLT) to the optical network units (ONUs) using TDM. The transmit side of the OLT and the receive side of the ONUs can therefore use continuous-mode integrated circuits (ICs). The challenge in the design of a chip set comes from the upstream data path. In the upstream direction, using time-division multiple access (TDMA), multiple ONUs transmit data to the OLT in the central office (CO). Because of optical path differences, the upstream traffic is inherently bursty with asynchronous phase steps $\Delta\varphi \leq 2\pi$ rad, which exist between the consecutive kth and $(k+1)$th packets. This inevitably causes conventional clock and data recovery (CDR) circuits to lose pattern synchronization leading to packet loss. Preamble bits can be inserted at the beginning of each packet to allow the CDR feedback loop enough time to settle down and thus acquire lock. However, the use of a preamble introduces overhead, reducing the effective throughput and increasing delay. Consequently, an OLT requires a burst-mode (BM) CDR, which is responsible for phase recovery and must be achieved at the beginning of every packet. The most important characteristics of the BM-CDR are its phase acquisition time, which must be as short as possible, and its robustness to long runs of consecutive identical digits (CIDs).

Different approaches have been proposed to build BM-CDRs with short phase acquisition times. The first approach, based on feedback, consists in trading off the loop bandwidth of phase-locked loop (PLL)-based CDR to reduce the settling time [10]. The disadvantages include stability issues, jitter peaking, and limited jitter filtering. The second approach, based on feedforward, consists of gated voltage-controlled oscillators (GVCOs) [11]. Here, clock phase alignment is done by triggering a local clock on each transition of the input data. Phase acquisition is rapid, but this solution is susceptible to pulse distortions and does not filter out input jitter. The last approach is based on oversampling. One can either oversample in the time domain [12]–[14] or in the space domain [9], [15]. Oversampling in time is achieved by using a clock frequency higher than the bit rate. This requires faster electronics operating at twice or thrice the aggregate bit rate resulting in wasted power consumption, in addition to the knowledge of a predefined unique delimiter (start of packet) that is exploited as a signature for phase picking. These BM-CDRs are limited to interpacket phase acquisition—*between* consecutive packets. Oversampling in space requires multiphase clocks with a frequency equal to the bit rate. This requires a generation of multiple (8 to 10) phases of the clock with low skew between them. This technique suffers from high complexity and power consumption.

In this paper, we present a novel BM-CDR architecture based on injection locking and space sampling with a hybrid topology of feedback and feedforward. The BM-CDR uses electronics operated *at* the bit rate with only *two* phase clocks, leading to more efficient power consumption. Furthermore, the BM-CDR requires *no a priori* knowledge of the packet delimiter. Hence, this BM-CDR can also acquire phase in even more stringent conditions; that is, for intrapacket phase acquisition—*within* a packet—making it truly modular across application testbeds. Our 20-GSample/s (10 GHz $\times$ 2 phase clocks) BM-CDR achieves a bit error rate (BER) $< 10^{-10}$ with *instantaneous* (0-bit)

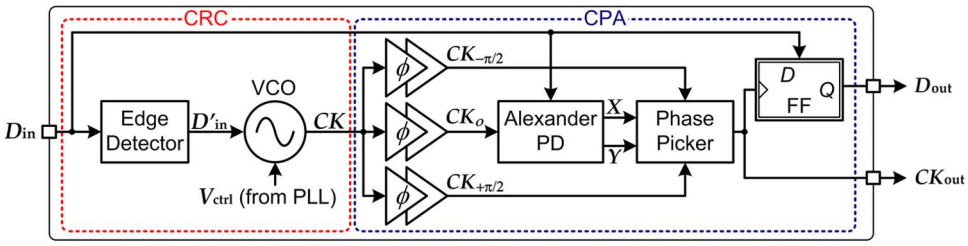

Fig. 2. Block diagram of the BM-CDR architecture based on injection-locking and space sampling.

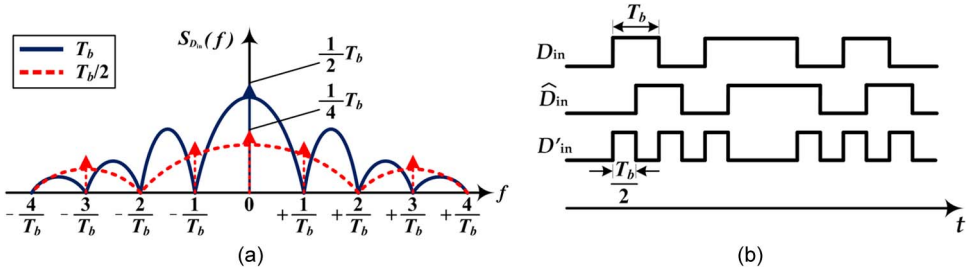

Fig. 3. (a) Power spectral density (in logarithmic scale) of NRZ data for T_b and $T_b/2$ pulse widths. (b) Waveforms of the XOR gate with a half bit-period $(T_b/2)$ pulse width between the two inputs.

phase acquisition for any phase step $|\Delta\varphi| \leq 2\pi$ rad, between consecutive bits, and *no* trading-off in the loop bandwidth.

The rest of this paper is organized as follows: Section 2 details the architecture of the proposed BM-CDR. Section 3 is devoted to the presentation and analysis of the experimental results. Finally, this paper is concluded in Section 4.

2. Novel BM-CDR Architecture

A block diagram of the proposed BM-CDR is shown in Fig. 2. The BM-CDR is composed of a clock recovery circuit (CRC) and a CPA. The CRC employs an injection-locking technique, whereas the CPA is based on oversampling in the space domain with two multiphase clocks and a phase-picking algorithm.

Under ideal conditions, with no intersymbol interference (ISI), error-free data recovery is achieved when the received data are sampled within half-bit period of the nominal sampling point. For a conventional PLL-based CDR, the ideal sampling point by the recovered clock is in the center of the data eye, and the phase error process is modulo-2π rad. For this BM-CDR, with $2\times$-oversampling with multiphase clocks separated by π rad, the sampling points are located at $-\pi/2$ rad and $+\pi/2$ rad, respectively, from the center of the data bit. In this case, the phase error process is modulo-π rad.

2.1. Clock Recovery

PON systems employ a simple binary amplitude modulation data format—nonreturn to zero (NRZ)—for ease of detection. Random NRZ data have characteristic properties that directly influence the design of CRCs. The power spectral density (PSD) $S_{\mathrm{NRZ}}(f)$ of an NRZ data sequence with normalized average power of unity is expressed as

$$S_{\mathrm{NRZ}}(f) = \frac{T_b}{2}\left[\frac{\sin(\pi f T_b)}{\pi f T_b}\right]^2 \tag{1}$$

where f is the frequency parameter, and T_b is the bit period. The spectrum of the NRZ data, as depicted in Fig. 3(a) (solid curve), exhibits no spectral component (nulls) at integer multiples of the

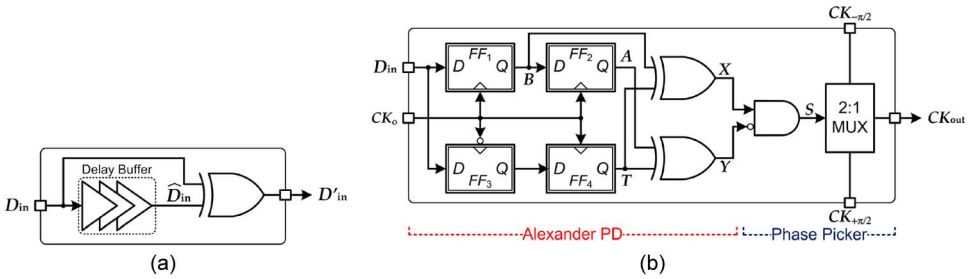

Fig. 4. Hardware implementation of the (a) edge detector and (b) Alexander PD with phase picker.

bit rate frequency $f = n/T_b,\ n = 1, 2, \ldots$; thus, providing no direct information for clock extraction. This implies that a CRC can lock to these spurious signals instead of the bit rate frequency or not at all. Furthermore, a linear time-invariant (LTI) operation cannot extract a periodic clock from these data [16]. However, the information about the frequency of the data can be extracted from the *spacing* between the data transitions. These transitions appear as the rising and falling edges of the data signal. Thus, a nonlinear function may be used to recover the clock.

In Fig. 2, clock recovery is performed by using a method comprised of a nonlinear element—an edge detector—in front of the data signal. The edge detection is performed by an XOR gate operating on the input data D_{in} and its delayed replica $\widehat{D}_{\text{in}}$, as illustrated in Fig. 4(a). Fig. 3(b) shows that pulse D'_{in}, generated by the XOR gate indicates the data transitions. Furthermore, since the transition of a random data sequence is still random, the spectrum of the generated pulses resembles that of a return to zero (RZ). That is, the spectrum of pulse D'_{in} displays as a square of sinc function with strong clock spectral lines at the data rate and its harmonics, as depicted in Fig. 3(a) (dotted curve). From (1), the spectrum for a bit-period (T_b) pulse nulls at $1/T_b$, whereas the spectrum for a half-bit-period $(T_b/2)$ pulse expands twice wider (nulls at $2/T_b$) but with lower magnitude. Consequently, this facilitates the injection locking of the subsequent VCO to the date rate or even its harmonics [17]. Theoretical derivations indicate that by maintaining a $T_b/2$ delay between the two inputs of the XOR gate yields the strongest injection [16]. As shown in Fig. 2, the clock signal *CK* is recovered from the edge-detected waveform by passing through the PLL-based VCO tuned near the clock frequency. In order to reduce jitter on the recovered clock signal, the VCO should have a good selectivity to suppress the unwanted data-dependent signal that results in amplitude and phase modulation. The recovered clock is then fed to the CPA.

2.2. CPA

The CPA utilizes multiphase clocks at the bit rate and a novel phase-picking algorithm based on an "early–late" detection principle that is simple, fast, and effective. As illustrated in Fig. 2, the CPA is based on a feedforward topology and comprises of phase (ϕ-) shifters, an Alexander phase detector (PD), a phase picker, and a D flip-flop (D-FF). The ϕ-shifters utilize the clock recovered by the CDR *CK* to provide multiple clocks, i.e., CK_o, $CK_{-\pi/2}$, and $CK_{+\pi/2}$, with low skew and different phases, i.e., 0 rad, $-\pi/2$ rad, and $+\pi/2$ rad, respectively, with respect to *CK*. Next, an Alexander PD [18], which inherently exhibits *bang-bang* (binary) characteristics, is used to strobe the data waveform D_{in}, with consecutive clock CK_o edges, at multiple points in the vicinity of expected transitions. This results in three data samples as shown in Fig. 5(a): 1) previous bit *A*; 2) the current bit *B*; and 3) a sample of the current bit at the zero crossing *T*. Depending on the phase difference between the consecutive packets, the PD aided by these samples, i.e., $X \equiv T \oplus B$ and $Y \equiv A \oplus T$, can determine the location of the clock edge with respect to the data edge as follows: 1) if $A \neq T = B$ ($X \downarrow$ and $Y \uparrow$), then CK_o lags D_{in} (is late) when $-\pi < \Delta\varphi < 0$ rad [see Fig. 5(b)]; 2) if $A = T \neq B$ ($X \uparrow$ and $Y \downarrow$), then CK_o leads D_{in} (is early) when $0 < \Delta\varphi < +\pi$ rad [see Fig. 5(c)]; 3) if $A = T = B$ ($X \downarrow$ and $Y \downarrow$), then no data transition is present due to CIDs; and 4) if $A = B \neq T$ ($X \uparrow$ and $Y \uparrow$), then no decision is possible as CK_o is either in-phase with D_{in} when $\Delta\varphi = 0$ rad or antiphase with D_{in} when $|\Delta\varphi| = \pi$ rad. The

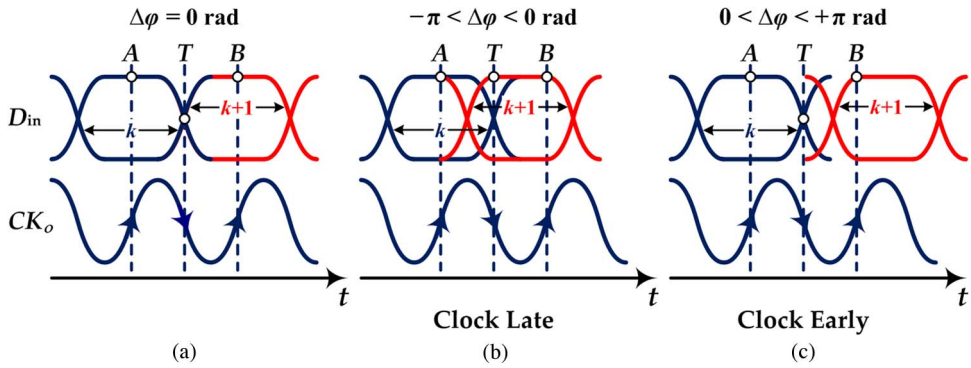

Fig. 5. Alexander PD three-point sampling scheme for different phases between consecutive packets: (a) $\Delta\varphi = 0$ rad, CK_o in-phase with D_{in}, (b) $-\pi < \Delta\varphi < 0$ rad, CK_o lags D_{in} (is late), and (c) $0 < \Delta\varphi < +\pi$ rad, CK_o leads D_{in} (is early).

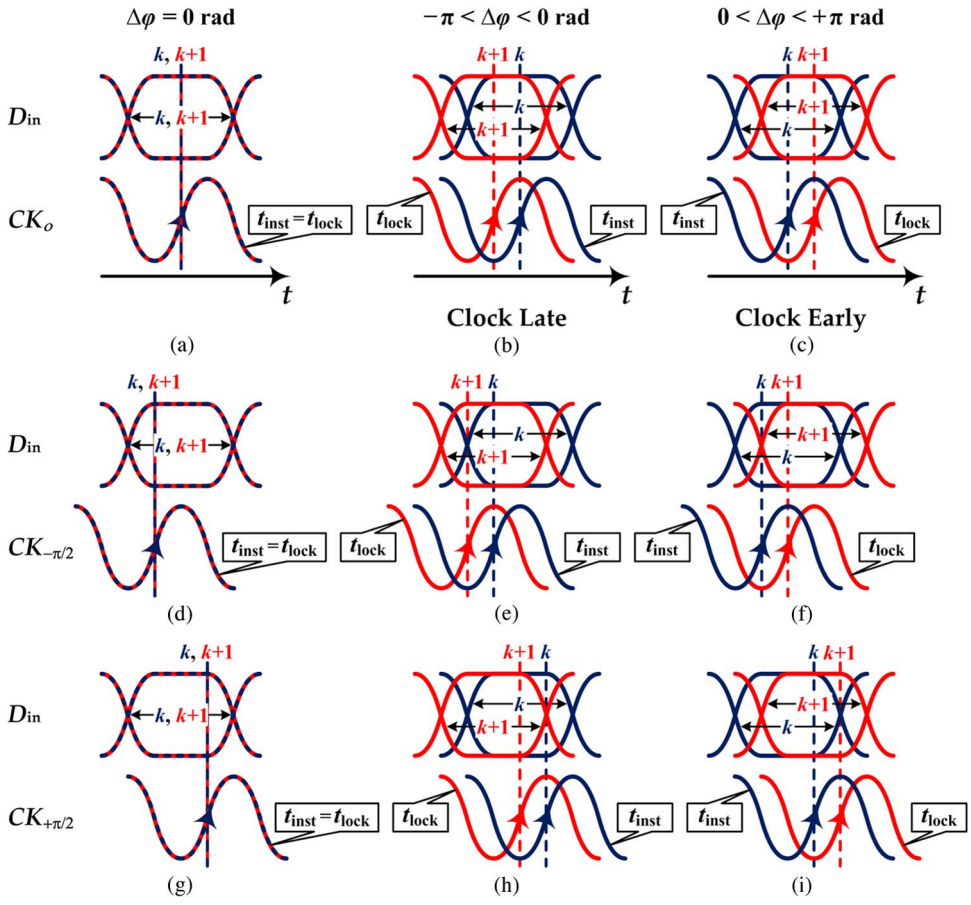

Fig. 6. CPA phase-picking algorithm. Three different phase steps between consecutive packets are considered: $\Delta\varphi = 0$ rad, $-\pi < \Delta\varphi < 0$ rad, and $0 < \Delta\varphi < +\pi$ rad.

clock CK_o early–late information (X and Y), together with the multiphase clocks $CK_{-\pi/2}$ and $CK_{+\pi/2}$, is provided to the phase picker.

With the aid of eye diagrams we illustrate the idea behind the phase-picking algorithm. Fig. 6 depicts the response of sampling the data D_{in}, with the unshifted clock CK_o, and the multiphase clocks $CK_{-\pi/2}$ and $CK_{+\pi/2}$. Let t_{inst} be the instantaneous clock that is in-phase with the last bit of the

TABLE 1

CPA (Alexander PD AND ϕ-Picker) logic

Data Condition	CK_o	XY	CK_{out}
$-\pi < \Delta\varphi < 0$ rad	Late	$\downarrow\uparrow$	$CK_{-\pi/2}$
$0 < \Delta\varphi < \pi$ rad	Early	$\uparrow\downarrow$	$CK_{+\pi/2}$
$\Delta\varphi \in \{0, \pm\pi$ rad$\}$ or CIDs	$\times$	$\uparrow\uparrow, \downarrow\downarrow$	$CK_{-\pi/2,+\pi/2}$

kth packet and out-of-phase by $|\Delta\varphi| \leq 2\pi$ rad with the first bit of the $(k+1)$th packet. To achieve instantaneous phase acquisition, the CPA must use the instantaneous clock t_{inst} to correctly sample the bits of the $(k+1)$th packet. Note, in the case of a conventional PLL-based CDR, its feedback loop would need finite time to settle down and acquire lock; that is, align the instantaneous clock t_{inst} to the lock state t_{lock} so as to sample in the middle of the data bit.

When there is no phase difference between the consecutive packets $\Delta\varphi = 0$ rad, either of clocks $CK_{-\pi/2}$ or $CK_{+\pi/2}$ will correctly sample the data bits of the phase shifted $(k+1)$th packet [see Fig. 6(d) and (g)]. This is also true for an antiphase step $\Delta\varphi = \pm\pi$ rad, (not shown in Fig. 6 because the scenario is similar to the 0-rad phase step—a modulo-π process). For a phase step $-\pi < \Delta\varphi < 0$ rad, clock CK_o will lag the data [see Fig. 6(b)]; clock $CK_{+\pi/2}$ will sample the bits on or close to the transitions of the data eye [see Fig. 6(h)] and thus corrupt the data. On the other hand, clock $CK_{-\pi/2}$ will correctly sample the data [see Fig. 6(e)]. Similarly, for a phase step $0 < \Delta\varphi < +\pi$ rad, clock CK_o will lead the data [see Fig. 6(c)]; clock $CK_{-\pi/2}$ will sample the bits on or close to the transitions [see Fig. 6(f)], whereas clock $CK_{-\pi/2}$ will correctly sample the data [see Fig. 6(i)]. That is, regardless of any phase step $|\Delta\varphi| \leq 2\pi$ rad, there will be at least one sampling clock, either $CK_{-\pi/2}$ or $CK_{+\pi/2}$, that will yield an accurate sample. The phase picker then selects the most accurate sampling clock CK_{out}, from these two possibilities for driving the D-FF to retime the data; that is, sample the noisy data yielding an output D_{out}, with less jitter. The foregoing concepts on the Alexander PD and phase picker are summarized in Table 1, leading to the circuit topology in Fig. 4(b). The result is that the CPA achieves instantaneous phase acquisition (0 bit) for any phase step $|\Delta\varphi| \leq 2\pi$ rad; that is, no preamble bits $(I = 0)$ at the beginning of the packet are necessary. Next, we provide an experimental demonstration for this, backed by a probabilistic theoretical prediction.

3. Results and Discussion

The proposed BM-CDR is built from low cost/complexity commercial off-the-shelf (COTS) components rated at 13 Gb/s. It is built by integrating the following evaluation boards from Hittite Microwave: XOR gate (HMC721LC3C), ϕ-shifters (HMC538LP4), Alexander PD (HMC6032LC4B), AND gate (HMC722LC3C), 2:1 selector (HMC678LC3C), and D-FF (HMC723LC3C).

The BM-CDR is tested in a conventional BM test setup [9], [10]. Bursty traffic is generated from an Anritsu pattern generator by adjusting phase $\Delta\varphi$ in between packets or within a packet with a phase shifter. The packets are formed from guard bits, preamble bits, delimiter bits, $2^{15} - 1$ pseudorandom binary sequence (PRBS) payload bits, and comma bits. The phase steps can be set between $\pm$125 ps with a 1-ps resolution, corresponding to a $\pm$1.25 unit interval (UI) at 10 Gb/s. Note that 1 UI or 2π rad corresponds to 100 ps (1-bit period) at 10 Gb/s.

The plots in Fig. 7 depict the BER performance of a conventional CDR and the proposed BM-CDR at 10 Gb/s as a function of the phase step $|\Delta\varphi| \leq 2\pi$ rad, between two consecutive data bits, for a *zero* preamble length. For the CDR, we observe two bell-shaped curves centered at approximately $\pm$50 ps [see Fig. 7(a)]. As expected, these represent the half-bit periods corresponding to the worst-case phase steps at $\Delta\varphi = \pm\pi$ rad, respectively. It follows that the CDR is sampling near the edge of the data eye, resulting in a loss of lock. At relatively small phase shifts (near) $\Delta\varphi \in \{0$ rad$, \pm 2\pi$ rad$\}$, we can easily achieve error-free operation, BER $< 10^{-10}$, because the CDR is almost sampling at the middle of each data bit. For our BM-CDR, we achieve error-free operation for any phase step $|\Delta\varphi| \leq 2\pi$ rad with *zero* preamble bits allowing for instantaneous phase acquisition [see Fig. 7(a)]. Additionally, we note that the BM-CDR can support up to 1000 CIDs with error-free operation. As the

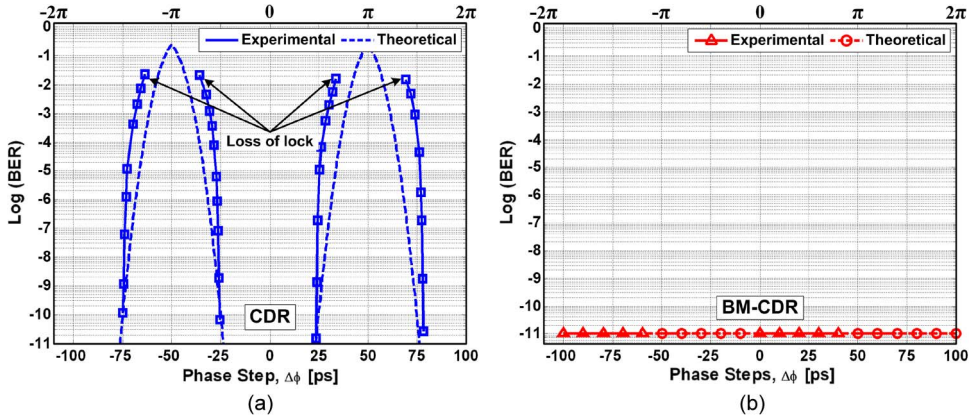

Fig. 7. BER performance versus phase step for a zero preamble length (solid lines for experimental curves; dashed line from theoretical predictions). (a) Conventional CDR. (b) Proposed BM-CDR.

length of the CIDs is increased to ~2000 bits, the phase error between the successive bursts can accumulate up to $|\Delta\varphi_e| = \pi$ rad, resulting in a BER ~ 0.5.

At this point, it is interesting to compare the experimental results with probabilistic theoretical predictions to draw some important conclusions. The sampling error probability P_s of the CDR in presence of phase steps $|\Delta\varphi| \leq 2\pi$ rad and an I-bit preamble can be expressed as [12]

$$P_s(|\Delta\varphi|) = \frac{1}{2}\left\{Q\left(\frac{\pi - (|\Delta\varphi| - \psi)(1-\eta(I))}{2\pi\sigma_{t_s}[\text{UI}]}\right) + Q\left(\frac{\pi + (|\Delta\varphi| - \psi)(1-\eta(I))}{2\pi\sigma_{t_s}[\text{UI}]}\right)\right\} \tag{2}$$

where $Q(\cdot)$, called the "Q function," is the normalized Gaussian-tail probability defined as

$$Q(x) \triangleq \frac{1}{\sqrt{2\pi}}\int_x^\infty \exp\left(-\frac{\lambda^2}{2}\right)d\lambda \tag{3}$$

where σ_{t_s} is the root mean square (RMS) jitter on the sampling clock in UI, ψ is the correcting factor introduced to account for the symmetrical performance about the edges of the data bit at $-T_b/2$ and $+T_b/2$ as

$$\psi = \begin{cases} 0, & \text{if } |\Delta\varphi| \leq \pi \text{ rad} \\ 2\pi, & \text{if } \pi < |\Delta\varphi| \leq 2\pi \text{ rad} \end{cases} \tag{4}$$

and $\eta(I)$ measures the CDR's lock acquisition time, analytically derived to be [16]

$$\eta(I) = 1 - \exp(-I\zeta\omega_n T_b) \times \left\{\cosh(I\omega_n T_b\sqrt{\zeta^2-1}) - \frac{\zeta}{\sqrt{\zeta^2-1}}\sinh(I\omega_n T_b\sqrt{\zeta^2-1})\right\} \tag{5}$$

where $\zeta > 0$ is the "damping ratio" and ω_n in radians per second is the "natural frequency," both being functions of the CDR circuit parameters [16].

Moving forward, the Alexander PD's probability of correctly determining an early or late clock CK_o can be written as

$$\Pr(CK_o) = \Pr(A) \times \Pr(B) \times \Pr(T) \tag{6}$$

and the probabilities of correctly sampling points A, B, and T can be given as:

$$\Pr(A) = \Pr(B) \times [1 - P_s(|\Delta\varphi|)] \tag{7}$$

$$\Pr(B) = 1 - P_s(|\Delta\varphi|) \tag{8}$$

$$\Pr(T) = \{1 - \vartheta[P_s(|\Delta\varphi| - \pi) + P_s(|\Delta\varphi| + \pi)]\} \times [1 - P_s(|\Delta\varphi|)] \tag{9}$$

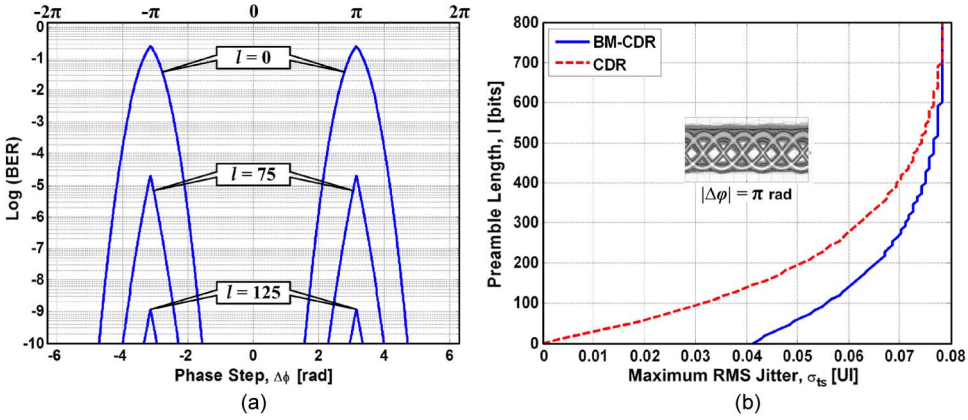

Fig. 8. (a) BER performance of a conventional CDR versus phase step with increasing preamble length. (b) Preamble length versus maximum allowable RMS jitter to achieve a BER $\leq 10^{-10}$ for the worst-case phase step $|\Delta\varphi| = \pi$ rad.

where $P_s(|\Delta\varphi|) = P_s(|\Delta\varphi|, l = 0)$ sampling error probability of a bit, and ϑ is another correcting factor introduced to account for the symmetrical performance about the edges of the data bit as

$$\vartheta = \begin{cases} \frac{1}{2}, & \text{if } |\Delta\varphi| \leq \pi \text{ rad} \\ 1, & \text{if } \pi < |\Delta\varphi| \leq 2\pi \text{ rad.} \end{cases} \tag{10}$$

The sampling points of the multiphase clocks $CK_{-\pi/2}$ or $CK_{+\pi/2}$ are located at $t_k \in \{-\pi/2, +\pi/2\}$, respectively, about the center of the data eye. The sampling error probabilities P_s^k of the multiphase clocks can be calculated by convolving $P_s(|\Delta\varphi|)$ in (2), with the sampling points t_k, as

$$P_s^k = P_s(|\Delta\varphi|) \otimes \delta(|\Delta\varphi| - t_k) \tag{11}$$

where

$$\delta(|\Delta\varphi| - t_k) \triangleq \begin{cases} 1, & \text{if } |\Delta\varphi| = t_k \\ 0, & \text{if } |\Delta\varphi| \neq t_k \end{cases} \tag{12}$$

is the Dirac-delta function. It follows from the sifting property

$$P_s^k = \int_{-\infty}^{+\infty} P_s(|\Delta\varphi| - \lambda)\delta(\lambda - t_k)d\lambda = P_s(|\Delta\varphi| - t_k).$$

The phase-picking algorithm determines the clock sample $CK_{-\pi/2}$ or $CK_{+\pi/2}$, closest to the center of the data eye upon detecting an early or late clock CK_o, with respect to data D_{in}. Consequently, the sampling error probability of the BM-CDR $P_s^{\text{BM-CDR}}$ can be expressed as

$$P_s^{\text{BM-CDR}} = \Pr(CK_o) \times \min\{P_s(|\Delta\varphi| - t_k)\}. \tag{13}$$

Finally, we define the BER, denoted as P_e, of the CDR and BM-CDR, from the sampling error probabilities in (2) and (13), respectively, as follows:

$$\text{BER} \equiv P_e \triangleq \begin{cases} P_s(|\Delta\varphi|), & \text{for PLL-based CDR} \\ P_s^{\text{BM-CDR}}, & \text{for BM-CDR.} \end{cases} \tag{14}$$

We compare the experimental results with the theoretical predictions for the CDR and the BM-CDR from (2) and (13) in Fig. 7(a) and (b), respectively. For BER $< 10^{-6}$, the results are in close agreement. However, for the CDR, the theoretical bound is optimistic for BER $> 10^{-6}$ as the probabilistic model accounts for the jitter input to the receiver and not for jitter generated by the

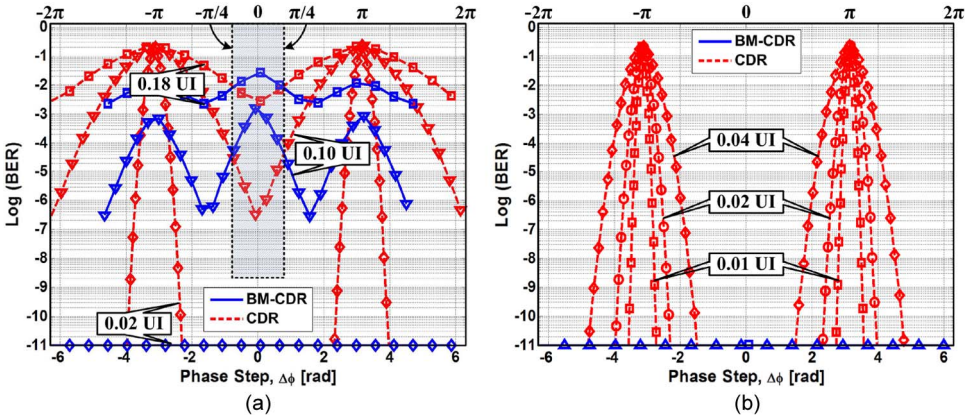

Fig. 9. BER performance of the BM-CDR and CDR versus phase step for different RMS jitter and zero preamble bits. (a) $\sigma_{t_s} > 0.04$ UI depicting the tradeoff region in the range $|\Delta\varphi| \leq \pi/4$ rad. (b) $\sigma_{t_s} \leq 0.04$ UI.

circuitry. This may be a result of VCO phase noise in the CDR and data bits being asymmetric with different rise and fall times leading to different jitter distribution on the edges of the data eye.

To measure the phase acquisition time of the CDR, preamble bits ("1010 . . ." pattern) can be inserted at the beginning of the packet to help the PLL of the CDR to settle down and acquire lock until error-free operation is achieved. In Fig. 8(a), as the preamble length is increased, there is an improvement in the BER. After 125 preamble bits, we perceive error-free operation for any phase step. However, the use of a preamble introduces overhead, reducing the effective throughput and increasing delay.

To compare the jitter tolerance of the CDR with the proposed BM-CDR, examine the plots in Fig. 8(b), which show the number of preamble bits required to obtain a BER $\leq 10^{-10}$ as a function of the maximum allowable RMS jitter for the worst-case phase step $|\Delta\varphi| = \pi$ rad. Our BM-CDR is able to achieve instantaneous phase acquisition $(l = 0)$ when the RMS jitter $\sigma_{t_s} \leq 0.04$ UI. This is true for any phase step $|\Delta\varphi| = 2\pi$ rad, as shown in Fig. 7(b). This is not the case for the CDR as the tolerance to jitter is 0 UI to obtain instantaneous phase acquisition for the worst-case phase step. This implies that it is not feasible for the CDR to obtain instantaneous phase acquisition since a jitter-free sampling clock is practically impossible. These theoretical limits can be summarized as:

$$\lim_{l\to 0}\sigma_{t_s}^{\max} = \begin{cases} 0 \text{ UI}, & \text{for CDR} \\ 0.04 \text{ UI}, & \text{for BM-CDR} \end{cases} \quad \text{for} |\Delta\varphi| = \pi \text{ rad}. \tag{15}$$

With increasing preamble length, the jitter tolerance of the CDR and BM-CDR on the sampling clock increases for a given phase step. It tends to become independent of the phase step in the presence of a large number of preamble bits

$$\lim_{l\to\infty}\sigma_{t_s}^{\max} = 0.08 \text{ UI}, \quad \text{for all } |\Delta\varphi| \leq 2\pi \text{ rad}. \tag{16}$$

In Fig. 9, we plot the BER performance of the CDR and BM-CDR as a function of phase steps for different RMS jitter and zero preamble bits. When the RMS jitter is $\sigma_{t_s} > 0.04$ UI, the shaded area in Fig. 9(a) depicts the tradeoff region with the phase steps $|\Delta\varphi| \leq \pi/4$ rad, where the CDR has a better jitter tolerance than the BM-CDR. This is expected as the CDR's recovered clock is sampling closer to the middle of the data bit compared with the BM-CDR's multiphase clocks, which are sampling further away from the center of the data eye for phase steps $|\Delta\varphi| \leq \pi/4$ rad (see Fig. 6). However, for phase steps $\pi/4 < |\Delta\varphi| \leq \pi$ rad, the BM-CDR has a better jitter tolerance. Furthermore, Fig. 9(b) shows that, while the BM-CDR achieves instantaneous phase acquisition for any phase step $|\Delta\varphi| \leq 2\pi$ rad when the RMS jitter $\sigma_{t_s} \leq 0.04$ UI, the CDR performance degrades with increasing RMS jitter.

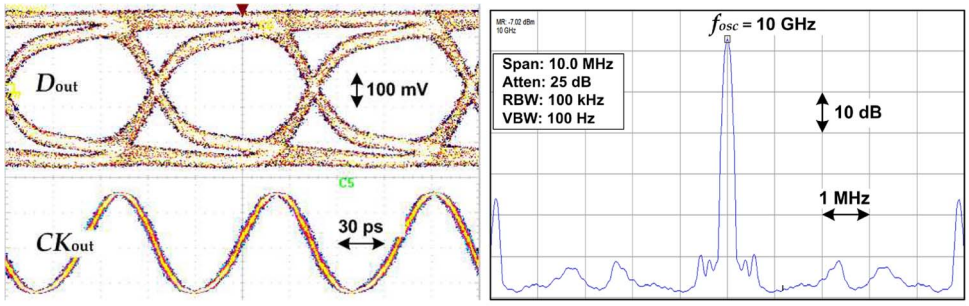

Fig. 10. (a) Eye diagram of recovered data and clock. (b) Spectrum of recovered clock (Atten: attenuation; RBW: resolution bandwidth; and VBW: video bandwidth).

Fig. 10(a) shows the eye diagram of the recovered data and clock in response to a $2^{15} - 1$ PRBS pattern. The RMS jitter of the recovered clock and data is 1.75 ps and 2.5 ps with a peak-to-peak voltage swing of 435 mVp-p and 300 mVp-p, respectively. The output spectrum of the recovered clock is shown in Fig. 10(b). The phase noise at 100, 500, and 1000 kHz offset is approximately -24, -62, and -68 dBc/Hz, respectively.

4. Conclusion

We have demonstrated a novel 20-GSample/s BM-CDR for optical multiaccess networks. The BM-CDR is based on an injection-locking technique for clock recovery and a CPA employing space sampling with two multiphase clocks at 10 GHz and a phase-picking algorithm for automatic clock phase acquisition. In summary, the BM-CDR achieves a BER $< 10^{-10}$ while featuring instantaneous (0 preamble bit) phase acquisition for any phase step $|\Delta\varphi| \leq 2\pi$ rad, without trading off its loop bandwidth (jitter tolerance). Thus, the BM-CDR could also find applications in future high-speed optical burst/packet switched networks, which may require a cascade of BM-CDRs that each consumes some of the overall jitter budget of the system.

Instantaneous phase acquisition can be used to improve the physical efficiency of the PON traffic, reduce the BM sensitivity penalty, and increase effective throughput of the system by increasing the information rate. Our eloquent solution leverages the design of components for long-haul transport networks using low-complexity commercial electronics, thus providing a cost-effective solution for PON BM-CDRs. These components are typically a generation ahead of the components for multiaccess networks. Thus, our solution will scale with the scaling for long-haul networks.

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