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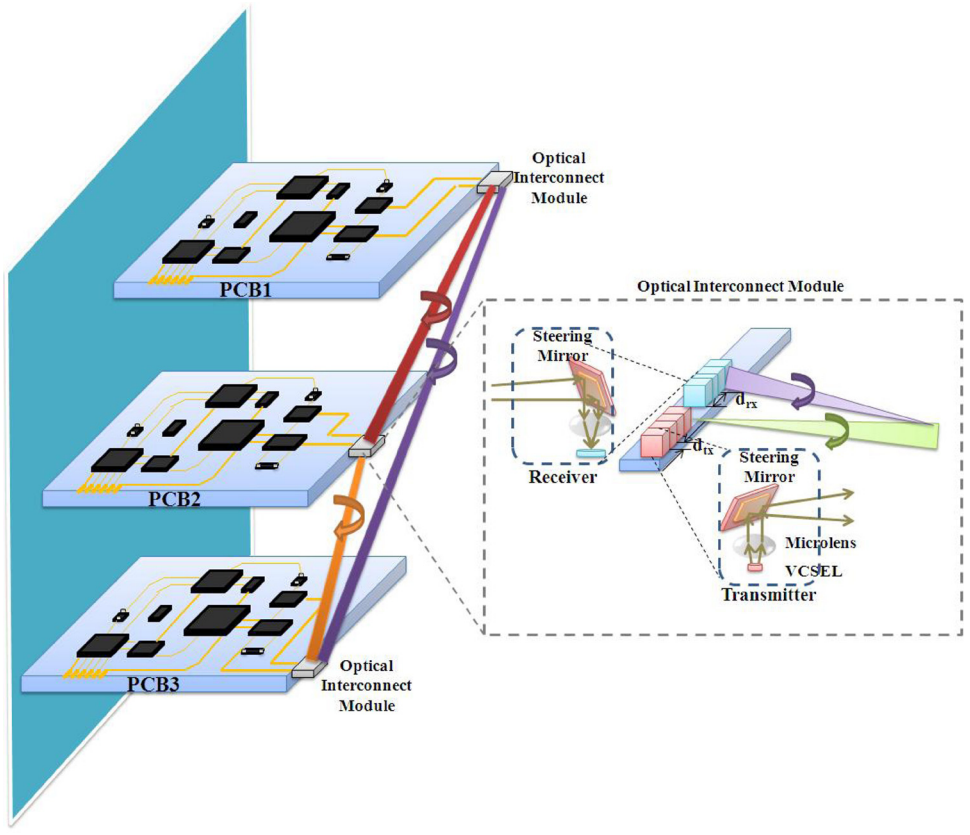

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High-Speed Reconfigurable Free-Space Card-to-Card Optical Interconnects

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Abstract: A reconfigurable free-space-based card-to-card optical interconnect architecture employing MEMS-based steering mirror arrays in conjunction with VCSEL and photodiode arrays is proposed and demonstrated in this paper. Theoretical studies and simulations indicate that error-free [bit error rate (BER) of $< 10^{-6}$] optical interconnects with a range on the order of tens of centimeters can be achieved, and the major factors limiting the performance are the VCSEL beam divergence and interchannel optical crosstalk. The tradeoff between the BER performance and the channel spacing of the receiver MEMS mirror array is also investigated. A proof-of-concept 3×10 Gb/s reconfigurable optical interconnect architecture is developed, demonstrating a BER of $\sim 10^{-6}$ and a receiver sensitivity better than ~ -11.5 dBm. Both the port-to-port and board-to-board reconfigurability of the proposed architecture are also experimentally demonstrated, opening the way for attaining higher throughputs through highly dense 3-D parallel optical interconnects.

Index Terms: Card-to-card interconnects, free-space optics, reconfigurable optical interconnects.

1. Introduction

With the continuous miniaturization of transistors into submicrometer range [1], the computing capability supported by a single chip has increased considerably, and the multicore architecture has been widely deployed for high-performance computing [2]–[4]. Sustained improvement in multichannel on-chip and on-board interconnection has been demonstrated [5]–[8]. However, the capacity of interconnection between cards and racks has not kept the pace. Conventionally, copper-based cables are used for data transmission between cards and racks. However, the electrical technologies are not suitable for future high-throughput interconnects due to the fundamental limitations, including the electric power consumption, heat dissipation, transmission latency, and electromagnetic interference [9].

To overcome the electrical card-to-card interconnect bandwidth limitation, the use of parallel short-range optical links has been proposed and studied [10]–[14], and most of the reported optical interconnect schemes are based on the use of polymer waveguides [10], [11] and multimode fiber (MMF) ribbons [12]–[14]. In particular, the fully integrated bidirectional parallel optical interconnect

structure reported by Schow *et al.* [11] employed polymer waveguides fabricated using a conventional low-cost printed circuit board (PCB) technology and demonstrated an aggregate data rate of 240 Gb/s. The MMF-ribbon-based optical interconnect architecture reported by Doany *et al.* [14] demonstrated a data transmission throughput of up to 1 Tb/s using 48 parallel interconnect channels in conjunction with a single complementary metal–oxide–semiconductor (CMOS)-compatible holey chip. However, such point-to-point interconnection schemes are inherently nonreconfigurable, and their flexibility in dynamically interconnecting electronic cards is very limited.

Several reconfigurable high-speed card-to-card interconnect structures based on free-space optics have been proposed and investigated [15]–[17], where the modulated optical signal of each interconnect channel directly propagates in free space and is switched along different directions via a link-selection block, thus adding significant flexibility to the communications between various cards. The 1.25-Gb/s free-space card-to-card optical interconnect architecture reported by Henderson *et al.* [15] employed a liquid crystal on silicon (LCoS) processor in conjunction with a polarization beam splitter as the link-selection block, while the architecture reported by McArdle *et al.* [16] used a prism together with a lens and a spatial light modulator (SLM) as the link-selection block. Furthermore, the use of an Opto-very-large-scale integration (Opto-VLSI) processor as the link-selection block has been reported by Aljada *et al.* [17], where a 3×3 2.5-Gb/s reconfigurable optical interconnect architecture was experimentally demonstrated. While such structures successfully demonstrated the concept of reconfigurable optical interconnects, they all suffer from low link-selection efficiency, considerably complicated tuning mechanism, limited tuning range as well as low bit rates that are insufficient for future-generation card-to-card interconnects.

In this paper, we propose and demonstrate the concept of a novel free-space reconfigurable card-to-card optical interconnect architecture that offers flexibility and high speed simultaneously. The proposed architecture employs VCSEL and photodiode (PD) arrays in conjunction with MEMS-based steering mirror arrays that serve as the link-selection block. Compared with the previously reported link-selection methods [15]–[17], MEMS-based mirrors provide higher selection efficiency, simpler tuning mechanism, and wider tuning range. Theoretical investigations and simulations show that optical interconnections can be established over free-space ranges on the order of tens of centimeters with a bit error rate (BER) of $< 10^{-6}$. The major limiting factors in the proposed architecture are the optical beam divergence in free space and the optical crosstalk induced by adjacent channels. The tradeoff between the BER performance and the MEMS mirror spacing is also investigated. In addition, a proof-of-concept 3×10 Gb/s PCB-based reconfigurable free-space optical interconnect demonstrator is developed, demonstrating both the port-to-port and board-to-board reconfigurability with a BER of $\sim 10^{-6}$ over up to 30-cm card-to-card distances and a receiver sensitivity as low as ~ -11.5 dBm. This reconfigurable card-to-card optical interconnect architecture can easily be scaled up to highly dense 3-D parallel optical interconnects.

This paper is organized as follows: In Section 2, the proposed free-space-based reconfigurable card-to-card optical interconnect architecture is briefly introduced; in Section 3, theoretical investigations and simulation results are presented, and the major factors limiting the system performance are discussed; in Section 4, the experimental setup for demonstrating the concept of reconfigurable card-to-card optical interconnects is presented, and the experimental results are discussed; and finally, conclusions are given in Section 5.

2. Proposed Reconfigurable Free-Space Card-to-Card Optical Interconnect Architecture

The proposed reconfigurable free-space card-to-card optical interconnect architecture is shown in Fig. 1, where a dedicated optical interconnect module is integrated onto each card (typically a PCB). This optical interconnect module mainly consists of a VCSEL array, a PD array, two microlens arrays, and two MEMS-based steering mirror arrays. At the transmitter side, the electrical signal from the attached card first modulates the VCSEL optical beam, and then, the modulated optical beam is collimated by the associated microlens. To minimize the VCSEL beam divergence, the distance between the VCSEL and microlens is made equal to the focal length of the microlens.

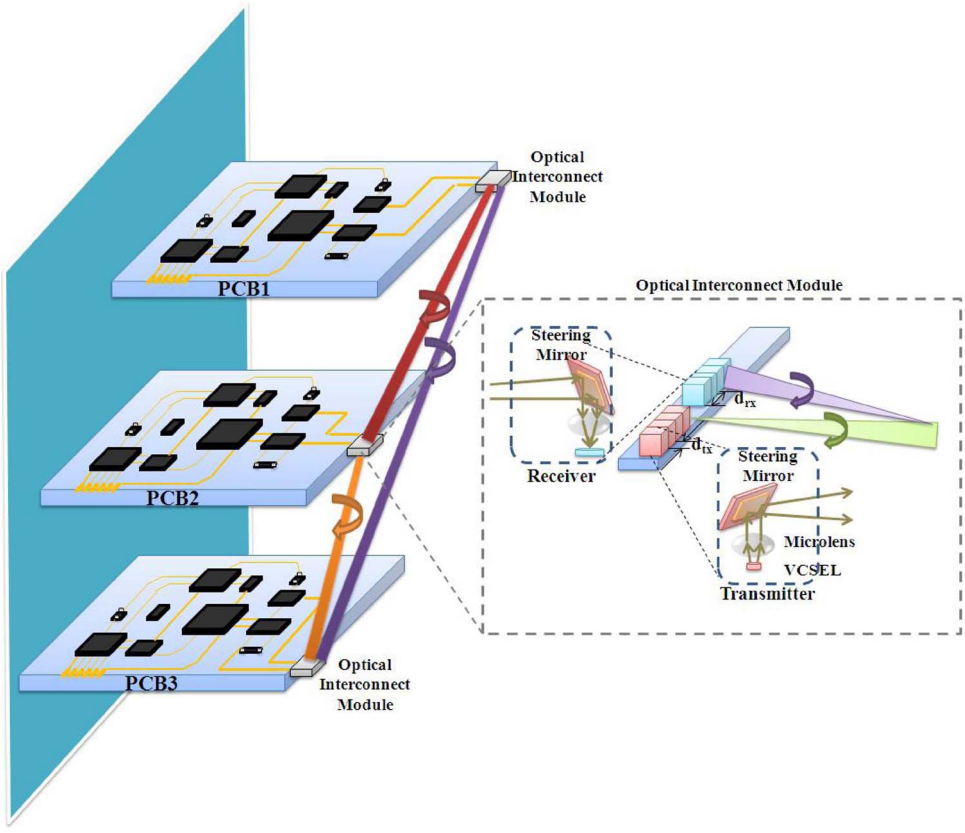

Fig. 1. Architecture of proposed reconfigurable free-space card-to-card optical interconnect.

Subsequently, the optical signal is steered toward the corresponding receiver with a steering MEMS mirror element. At the receiver side, the modulated optical signal is appropriately steered with another MEMS mirror element and focused onto the corresponding PD element. With analog steering mirrors being used, the transmitted optical beam can dynamically be steered along arbitrary directions, realizing adaptive optical interconnection with receivers at arbitrary locations within a communication range. In addition, inside a typical rack, the electrical cards are placed in parallel and the free-space link may be blocked if the optical interconnect modules are placed at the same position with respect to the adjacent cards. Since the proposed optical interconnect module is small in size, this possible blockage problem can be avoided by installing the module at different positions of the cards, as shown in Fig. 1.

Conventional optical interconnects employ VCSEL and PIN-PD arrays operating at the same wavelength [10]–[14]. We adopt the same approach for the realization of reconfigurable free-space optical interconnects because it i) is cost-effective, ii) eliminates the need for complex circuitry for the precise control of the wavelength of the VCSEL elements, and iii) increases the aggregate bit rate.

In the proposed reconfigurable optical interconnect architecture, since the VCSEL beams propagate in free space, their diameter expands as the transmission distance increases. Therefore, severe interchannel crosstalk is induced, leading to a degraded BER performance. This crosstalk issue can be suppressed by using a receiver MEMS steering mirror array with a large spacing between the elements. This is because i) the intensity of a Gaussian beam drops rapidly with the radial distance from the center of the beam and ii) the crosstalk signal induced by a Gaussian beam illuminating a MEMS element does not strike the other MEMS elements at their optimum incidence angles that maximize the optical coupling efficiency and signal detection by their associated PD elements.

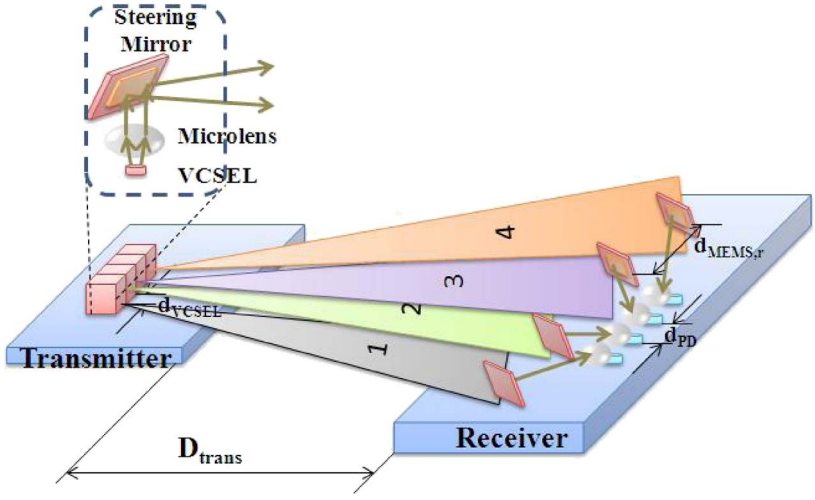

Fig. 2. Simulated card-to-card optical interconnect architecture.

3. Theoretical Studies and Simulations

Theoretical studies and simulations were undertaken to investigate the feasibility of the proposed reconfigurable free-space card-to-card optical interconnect architecture. The investigated interconnection configuration is shown in Fig. 2, where a 1×4 VCSEL array of element spacing d_{VCSEL} is used to realize parallel interconnects. The VCSEL optical beam is considered a Gaussian beam of divergence angle θ_{VCSEL}. Therefore, the beam waist $\omega_{0,\text{VCSEL}}$ can be expressed as [18]

$$\omega_{0,\text{VCSEL}} = \frac{\lambda}{\pi\theta_{\text{VCSEL}}} \tag{1}$$

where λ is the wavelength. A microlens array with a pitch size $d_{\text{lens}} = d_{\text{VCSEL}}$ is then aligned and mounted on top of the VCSEL array to collimate the VCSEL beams. The height difference between the VCSELs and the corresponding microlenses h_{lens} is made equal to the focal length f of the microlens in order to minimize the beam divergence after collimation. Therefore, the beam waist $\omega_{0,\text{lens}}$ and divergence angle after the microlens θ_{lens} can be calculated from the following expressions [19]

$$\omega_{0,lens} = \frac{f \cdot \lambda}{\pi\omega_{0,\text{VCSEL}}} \tag{2}$$

$$\theta_{\text{lens}} = \frac{\omega_{0,\text{VCSEL}}}{f}. \tag{3}$$

Subsequently, the collimated optical signal beams are mapped to the corresponding receiver MEMS-based steering mirror elements whose pitch size is similar to that of the VCSEL and microlens arrays. After propagating a free-space transmission distance d_{trans}, a central part of each optical beam is steered by a receiver MEMS-based mirror element onto the corresponding microlens element and focused onto the active window of its associated PD element. As discussed in the previous section, in order to reduce the interchannel optical crosstalk, the pitch size of the receiver MEMS-array, $d_{r,\text{MEMS}}$, can be chosen to be larger than the PD array pitch size, d_{PD}. In this case, each receiver MEMS element is steered along the appropriate angle that focuses and couples the received optical beam into the PD active areas. The intensity of the optical beam at the receiver side remains approximately Gaussian and can be described as [18]

$$I(r) = \frac{2P_t}{\pi\omega_r^2}\exp\left(-\frac{2r^2}{\omega_r^2}\right) \tag{4}$$

where P_t is the VCSEL output power at the transmitter side, and ω_r is the beam waist at the receiver side. The detected signal power $P_{s,i}$ and crosstalk power $P_{c,i}$ for channel i $(i = 1, 2, 3, \text{ or } 4)$ can be calculated using the following equation

$$P_{s,i} = \frac{2P_{t,i}}{\pi\omega_{r,i}^2} \cdot S_{\text{lens},i} \tag{5}$$

$$P_{c,i} = \sum_{j=1}^{4} \frac{2P_{t,j}}{\pi\omega_{r,j}^2} \cdot \exp\left(-\frac{2d_{c,ji}^2}{\omega_{r,j}^2}\right) \cdot S_{\text{eff},ji}, (j \neq i) \tag{6}$$

where $S_{\text{lens},i}$ is the aperture of the receiving microlens i, $d_{c,ji}$ is the distance from MEMS mirror i to the beam center of channel j, and $S_{\text{eff},ji}$ is the effective aperture of microlens i illuminated by optical beam j. Since $d_{r,\text{MEMS}} > d_{\text{lens}}$, the crosstalk signal does not strike other MEMS elements at the optimal incidence angle. Therefore, the crosstalk power induced by beam j into the microlens i is significantly smaller than the signal power, because most of the crosstalk beam is routed outside PD $i(S_{\text{eff},ji} < S_{\text{lens},i})$.

The performance of proposed reconfigurable free-space optical interconnect is best characterized by signal-to-noise ratio (SNR) and BER parameters. The SNR for channel i can be expressed as (on–off keying/OOK modulation format is used for simplicity) [20]–[22]

$$\text{SNR}_i \text{ (dB)} = 10 \times \log_{10} \frac{P_{s,i}}{P_{c,i} + \text{NEP}_i\sqrt{B_i}} \tag{7}$$

$$\text{BER}_i = \frac{1}{2}\text{erfc}\left(\sqrt{\frac{\text{SNR}_i}{2}}\right) \tag{8}$$

where NEP_i is the noise-equivalent power of the photodetector-amplifier i thermal noise, and B_i is the bandwidth of channel i. The photodetector-amplifier-induced noise variance σ_{pre}^2 can be calculated from the following equation [23]

$$\sigma_{\text{pre}}^2 = \frac{4kT}{R_F} I_2 B + \frac{4kT\Gamma}{g_m}(2\pi C_T)^2 I_3 B^3 \tag{9}$$

where g_m is the amplifier transconductance; Γ is a noise factor associated with channel thermal noise and gate-induced noise in the amplifier; C_T is the total input capacitance consisting of the PD and stray capacitance; I_2 and I_3 are the weighting functions, which are dependent only on the received optical pulse shape and the equalized output pulse shape, respectively; R_F is the feedback resistance; k is the Boltzmann's constant; and T is the absolute temperature.

Using (1)–(9) and the optical interconnect architecture parameters shown in Table 1, the simulated BER versus the horizontal distance between the transmitter and receiver is shown in Fig. 3 for the four channels of the proposed interconnect architecture illustrated in Fig. 2. Here, it should be noted that the horizontal distance is smaller than the total optical transmission distance from the VCSEL element to the corresponding PD element, due to the additional vertical propagation distances from the VCSEL and PD elements to the MEMS mirror elements at both the transmitter and receiver sides. It is clear from Fig. 3 that channels 1 and 4 have similar BER performances and so do channels 2 and 3, and this can be attributed to the symmetric configuration.

Furthermore, it is obvious that by increasing the horizontal distance between the transceivers, the BER also increases. This is because the diameter of Gaussian beams increases with the propagation distance, resulting in a smaller collected signal power and more interchannel crosstalk power being coupled into the PD element under consideration, thus degrading the BER performance. The impact of crosstalk can also be seen from the BER performance difference between channel 1 and channel 2, since channel 2 VCSEL/PD element is in the middle of the array, thus more susceptible to more crosstalk from the adjacent channels 1 and 3. From the results shown in Fig. 3, it is clear that the discrepancy BER between channels 1 and 2 increases with the horizontal distance, and this means that the impact of interchannel crosstalk is more pronounced.

TABLE 1

Optical interconnect architecture parameters used in simulations

Symbol	Quantity
d_{VCSEL}, d_{lens}, $d_{t,MEMS}$	250 μm
$d_{r,MEMS}$	2.5 mm
f, h_{lens}	656.5 μm
λ	850 nm
θ_{VCSEL}	17°
$P_{t,i}$ (i = 1, 2, 3, or 4)	2 mW
a_{lens} (radius of micro-lens)	118 μm
B	9.6 GHz
d_{PD}	250 μm
a_{PD} (radius of PD active window)	30 μm
C_T	0.17 pF
Γ	1.5
I_2	0.562
I_3	0.0868
g_m	0.2 mS

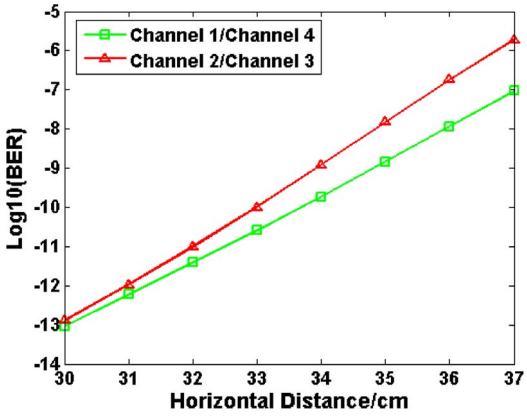

Fig. 3. Simulation BER performance versus the horizontal distance between the transceivers. Receiver MEMS mirror spacing is 2.5 mm, and VCSEL output power is 2 mW.

Fig. 4 shows the receiver sensitivity (at a BER of $< 10^{-9}$) versus the horizontal distance between the transmitter and receiver for all channels. It is clear from the figure that, in order to achieve the same BER performance, a larger received power is required as the horizontal distance increases. This is due to the fact that more interchannel crosstalk being induced into the receiving PD. Furthermore, channel 1 and channel 4 always have a better receiver sensitivity than channel 2 and channel 3, and this is consistent with the results shown in Fig. 3. In addition, for all channels, the receiver sensitivity degrades with increasing the transmission distance, and this is mainly due to the stronger interchannel crosstalk as discussed earlier.

Simulations were also carried out to demonstrate the reconfigurability of our proposed free-space optical interconnect architecture. In the second interconnection scenario, VCSEL elements 1, 2, 3, and 4 were interconnected to PD elements 3, 2, 4, and 1, respectively. The BER versus the horizontal distance between the transmitter and receiver for this configuration is shown in Fig. 5. With reference to the results shown in Fig. 3, it is clear from Fig. 5 that the BER performances for all four channels are almost similar. Furthermore, channel 3 and channel 4 slightly outperform channel 1 and channel 2. This is because the PD elements associated to channel 1 and channel 2 are in the center of the PD array and hence more susceptible to interchannel crosstalk.

As mentioned earlier, we purposely increased the pitch size of the MEMS-based steering mirror array at the receiver side to mitigate the impact of crosstalk. However, it is important to note that in

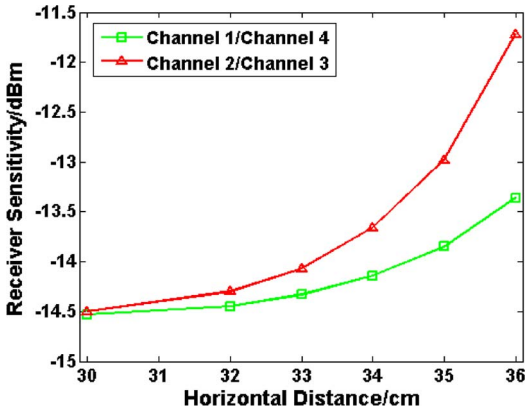

Fig. 4 Simulated receiver sensitivity versus the horizontal distance between the transceivers. Receiver MEMS mirror spacing is 2.5 mm, and bit rate is 10 Gb/s.

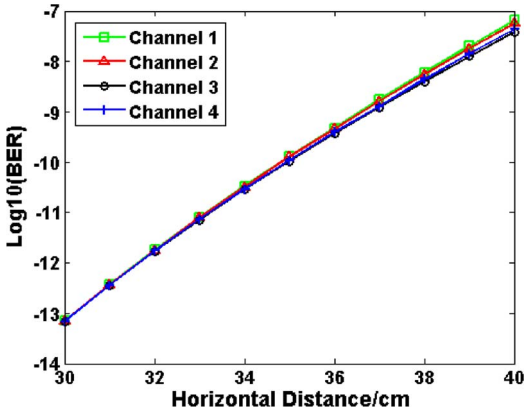

Fig. 5. Simulated BER performance versus the horizontal distance between the transceivers for the second configuration. Receiver MEMS mirror spacing is 2.5 mm.

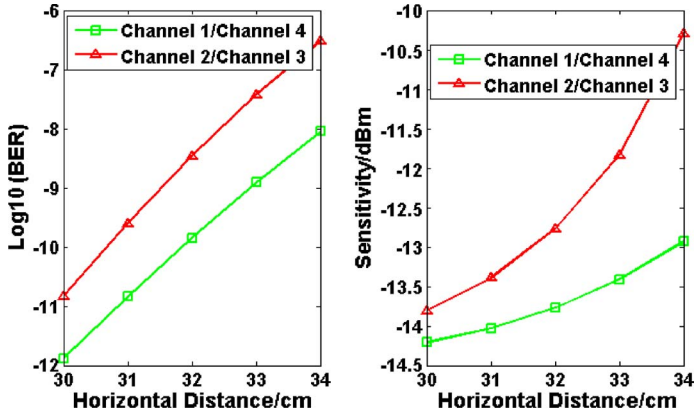

Fig. 6. Simulated BER and receiver sensitivity versus the horizontal distance between the transceivers for the second configuration. Receiver MEMS mirror spacing is 1.5 mm.

order to attain dense optical interconnects, it is more favorable to use an array with a small pitch size. The simulated BER performance as well as the receiver sensitivity versus the horizontal distance between the transmitter and receiver is shown in Fig. 6 (based on the configuration shown

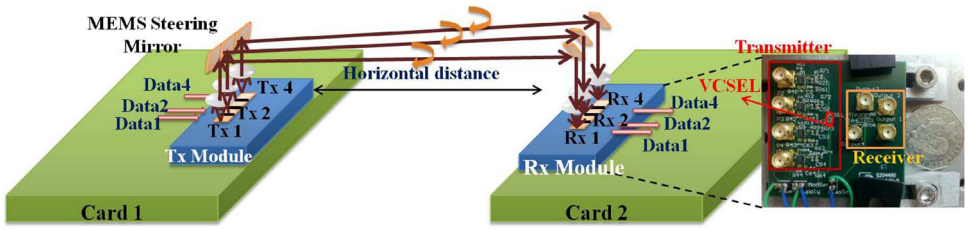

Fig. 7. Experimental setup (not to scale) for demonstrating the concept of reconfigurable card-to-card optical interconnect.

in Fig. 2), for a spacing between the MEMS-based steering mirrors at the receiver side of 1.5 mm. Comparing the results shown in Fig. 6 with the results presented in Figs. 3 and 4, it is clear that when the channel spacing is reduced, the BER performance and receiver sensitivity become worse. This is attributed to stronger interchannel crosstalk being induced as the intensity of a Gaussian beam is higher around its center.

4. Experiments and Discussions

4.1. Experimental Setup

In addition to the theoretical studies and simulations, experiments were set up, as shown in Fig. 7, to demonstrate the concept of our proposed reconfigurable free-space card-to-card optical interconnect architecture. In the experiments, an optical interconnect module was designed, fabricated, and integrated onto a PCB, as displayed in the inset of Fig. 7. Specifically, a 1×4 VCSEL array, the corresponding VCSEL driver circuits (four packaged drivers), a 1×4 PD array, and four transimpedance amplifier (TIA) chips were integrated onto a single small-size PCB. A microlens array was then aligned and mounted on top of the VCSEL array and the PD array to collimate the VCSEL beams and focus received optical beams onto the active windows of the PD elements. Each of the microlens arrays was attached to an XYZ translational stage, and the distance between the VCSEL/PD plane and the lens was changed manually. It should be noted that in real applications, the microlens array can be placed on a spacer of height equal to the focal length of the microlenses. Furthermore, separate MEMS steering mirror chips with < 5 ms point-to-point switching time and $> 96\%$ reflectivity were used to switch the optical beams to various cards, as illustrated in Fig. 1. The MEMS mirror chips were attached to XYZ translational stages and dynamically steered by changing the voltage applied to their activators.

In the experiment, an 850-nm VCSEL array with a 250-μm pitch was used and wire-bonded onto the PCB. The average divergence angle of the VCSEL beams was $\sim 17^{\circ}$ and varied slightly among the four elements of the array. The maximum bit rate of the VCSEL driver chips was 11.3 Gb/s. The VCSEL and PD microlens arrays had a pitch of 250 μm, a clear aperture of ~ 236 μm, a refractive index of ~ 1.45, and a focal length of ~ 656.5 μm. Microlens arrays with a comparatively high fill factor (large clear aperture) were chosen to minimize the diffraction effect at the transmitter side and to collect enough optical power at the receiver side. The PD array had also a pitch of 250 μm. Each PD element had an active aperture diameter of 60 μm and a responsivity of ~ 0.61 A/W at 850 nm and was wire-bonded onto a TIA chip. The 3-dB bandwidth of the TIA was ~ 12.6 GHz, and its differential transimpedance was ~ 5 kΩ. In addition, the size of the MEMS mirror was larger than the pitch of VCSEL and PD arrays, so only three out of the four available channels were used (the third VCSEL and PD elements were not used).

During the measurements, the bit rate for each channel was set to 10 Gb/s, and on–off keying (OOK) modulation was used. The output power from each VCSEL element was set to 2 mW using a dc bias current of ~ 6.5 mA. At the receiver side, to suppress the crosstalk, 2.5-mm spacing between the MEMS steering mirrors was chosen. Furthermore, the vertical distances between the microlens array and the MEMS steering mirror array were ~ 1.5 cm at the transmitter side and

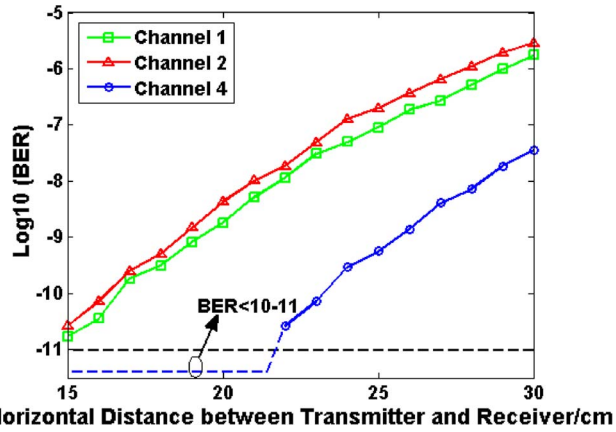

Fig. 8. BER versus horizontal distance between the VCSEL and PD PCBs, for three optical interconnects. Bit rate = 10 Gb/s, MEMS mirror spacing at receiver side = 2.5 mm, and VCSEL output power = 2 mW.

$\sim$10 cm at the receiver side, respectively. The larger distance used at the receiver side was necessary to increase the spacing of the receiver MEMS mirrors. While this approach led to slight reduction in detected signal power due to the longer propagation distance between the interconnected VCSEL and PD elements, it, however, reduced the crosstalk induced at other PD elements significantly.

4.2. Experimental Results and Port-Level Reconfigurability Demonstration

To demonstrate the concept of reconfigurable optical interconnect architecture on the port-level, two scenarios were considered. First, VCSEL element i $(i = 1, 2, \text{ or } 4)$ was interconnected to PD i. The measured BER versus the horizontal distance between the transmitter and receiver PCBs is shown in Fig. 8. Here, it should be noted that the horizontal distance is smaller than the total optical transmission distance from the VCSEL element to the corresponding PD element. It is clear from Fig. 8 that by increasing the horizontal distance between the VCSEL and PD PCBs, the BER also increases, for all three channels. This is because the diameter of the Gaussian beam increases with the propagation distance, resulting in a smaller collected signal power (the transmission power from VCSELs was fixed) and more interchannel crosstalk power being coupled into the various PD elements, thus degrading the BER performance. In addition, it can be seen from Fig. 8 that the performance of channel 4 is much better than the other two channels. This is because channel 4, which is relatively far from other channels, is less susceptible to crosstalk induced by channels 1 and 2. Furthermore, for all the three channels, even when the horizontal distance is 30 cm, which is typical for data center card-to-card interconnects, a BER of $\sim 10^{-6}$ can still be achieved. Therefore, better error-free (BER of $< 10^{-9}$ or even $< 10^{-12}$) high-speed optical wireless interconnections can be attained by additionally using forward-error-correction (FEC) codes [24].

Fig. 9 shows the measured BER versus the received optical power (obtained by changing the output power levels of the VCSEL elements) for different horizontal distances between the transmitter and receiver PCBs. It is clear that for horizontal distances of 25 cm [see Fig. 4(a)] and 30 cm [see Fig. 4(b)] between the transmitter and receiver PCBs, channel 4 receiver displays a better sensitivity (less than -11.92 dBm at a BER of $< 10^{-9}$) than the other two channels, and this is consistent with the results shown in Fig. 8. In addition, it is noticed that the receiver sensitivity degrades when the horizontal distance between the transmitter and receiver PCBs increases, mainly due to stronger interchannel crosstalk as discussed earlier. Furthermore, although the interchannel crosstalk in the experiments is weaker (one of the two channels in the center of the VCSEL/PD arrays was not used), the receiver sensitivity (at a BER of $< 10^{-9}$) is still worse by $\sim$3 dB, in comparison with the corresponding simulated sensitivity shown in Fig. 4. This is mainly due to the capacitance induced by the bonding wire used to connect the PD array to the TIA chips and PCB.

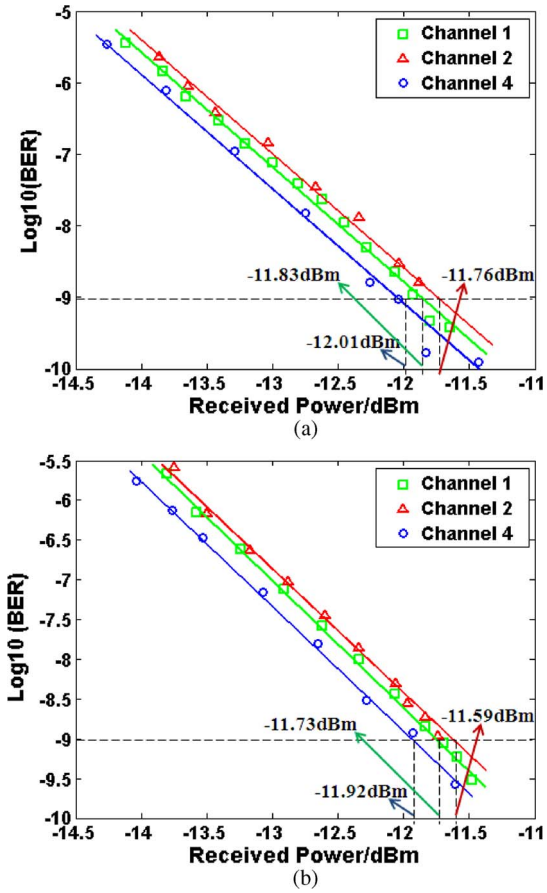

Fig. 9. BER versus received optical power for the three optical interconnects. Horizontal distance between the transmitter and receiver modules is (a) 25 cm and (b) 30 cm. Bit rate = 10 Gb/s.

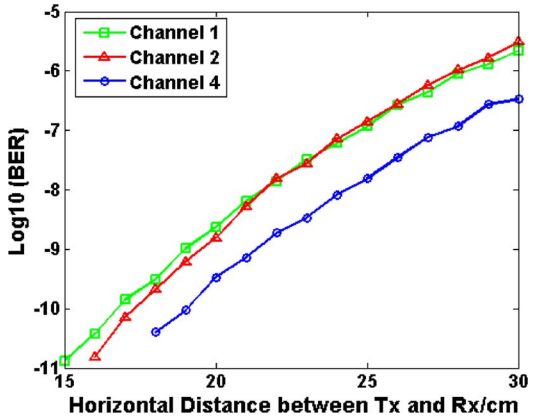

Fig. 10. BER versus horizontal distance between the VCSEL and PD PCBs. Channels 1, 2, and 4 correspond to interconnecting VCSEL elements 1, 2, and 3 to PD elements 2, 4, and 1, respectively. Bit rate = 10 Gb/s.

The second interconnection scenario was used to demonstrate the port-level reconfigurability of our proposed card-to-card optical interconnects, where VCSEL elements 1, 2, and 4 were interconnected to PD elements 2, 4, and 1, respectively. The measured BER versus the horizontal distance between the transmitter and receiver PCBs is shown in Fig. 10, for the three interconnects.

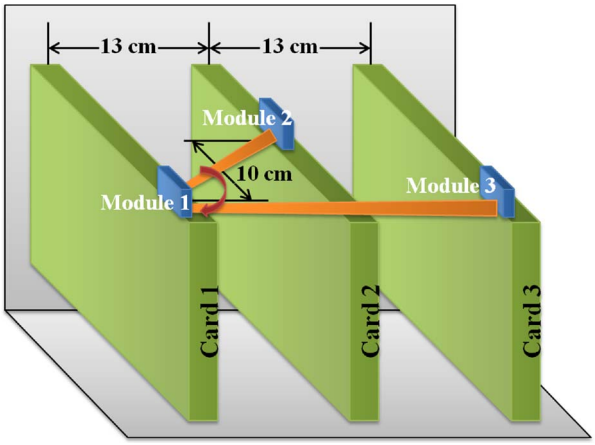

Fig. 11. Experimental setup (not to scale) for demonstrating the card-level reconfigurability of the proposed optical interconnect architecture.

TABLE 2

Measured BER performance

	Module 1 to Module 2	Module 1 to Module 3
$\log_{10}$(BER) (ch1)	-9.71	-6.39
$\log_{10}$(BER) (ch2)	-9.43	-6.16
$\log_{10}$(BER) (ch4)	$<$ -11	-8.44

Comparing the results shown in Figs. 8 and 10, insignificant penalty in BER performance is displayed for the second interconnection scenario, demonstrating that the proposed 3 $\times$ 10 Gb/s reconfigurable card-to-card optical interconnect architecture can arbitrarily connect any VCSEL element of a transmitter card to any PD element of a receiver card, and attain a BER of $\sim 10^{-6}$ for card-to-card horizontal distances of up to 30 cm. In addition, the BER performance for channel 4 shown in Fig. 10 is worse than that shown in Fig. 8. This is mainly due to the fact that when PD 1 is receiving the signal from VCSEL 4, the distances from the other VCSEL elements to PD 1 are relatively small, thus stronger interchannel crosstalk is induced, and the BER performance is degraded.

4.3. Card-Level Reconfigurability Demonstration

In addition to the port-level reconfigurability demonstration, experiments were also carried out to investigate the feasibility of reconfiguring the proposed optical interconnect architecture among different cards. The experimental setup is shown in Fig. 11. Three integrated interconnect modules were used, and similar to the setup shown in Fig. 7, in each module, the third VCSEL/PD elements were not used. The bit rate was still set at 10 Gb/s for each channel with OOK modulation format, and the transmission power from each VCSEL was 2 mW as well.

Table 2 shows the measured BER performances for all channels when module 1 was interconnected to module 2 and module 3, respectively. Inside the two interconnected transmitter and receiver modules, VCSEL element i $(i = 1, 2, \text{ or } 4)$ was interconnected to PD i. It is clear from the table that a BER of $< 10^{-6}$ was always realized, and the reconfigurability on the card-level was successfully demonstrated.

5. Conclusion

A novel high-speed reconfigurable free-space card-to-card optical interconnect architecture has been proposed in this paper. The concept is based on the utilization of MEMS-based steering mirror

arrays as an efficient and simple link-selection mechanism. Theoretical studies and simulations have been carried out to demonstrate the feasibility of the proposed scheme. Simulation results have shown that card-level interconnection ranges of up to tens of centimeters can be achieved and that the major performance limiting factors are the interchannel crosstalk as well as the divergence of the VCSEL beam propagating in free space from the transmitter side to the receiver side. In addition, the tradeoff between the BER performance and the MEMS-based steering mirror channel spacing has been studied.

Experiments have also been carried out, demonstrating a 3×3 10-Gb/s reconfigurable card-to-card optical interconnect structure integrated onto different PCBs. A BER of $\sim 10^{-6}$ has been realized for interconnected VCSEL and PD elements spaced horizontally at up to 30 cm, and a receiver sensitivity better than ~ -11.5 dBm has been attained. Furthermore, the reconfigurability of the proposed architecture on both port-level and card-level has also been verified. Compared with previous results on reconfigurable optical interconnect schemes, a much higher bit rate has been achieved with the proposed architecture in this paper, and the overall structure and reconfiguring mechanism is simpler.

Finally, to achieve a higher bit rate in our proposed interconnect scheme, a higher number of parallel channels should be integrated in each interconnect module. For the transmitter, the MEMS steering mirror array has the same pitch size as the VCSEL array, and dense integration is possible for a much higher aggregate bit rate. For the receiver side, the pitch size of the MEMS mirror array needs to be larger to reduce crosstalk. However, as indicated in the simulation, reducing the receiving MEMS mirror array pitch only results in slight degradation in the BER performance, due to the nonoptimal incident angle of interfering signals. Therefore, the proposed architecture can be scaled up by using highly dense 3-D parallel optical interconnects.

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