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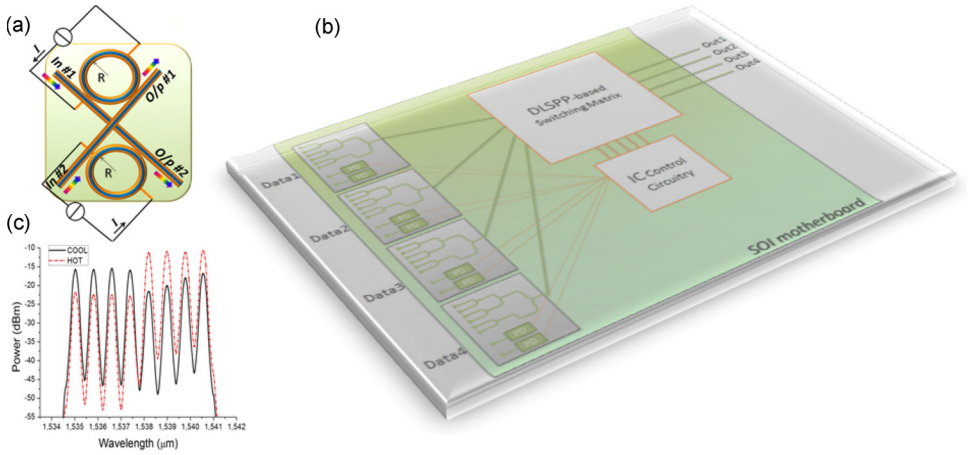

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Optical Interconnects Using Plasmonics and Si-Photonics

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(Invited Paper)

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Abstract: Optical interconnects have continued to experience significant advances during the last year, exploiting mainly relevant progress in silicon photonics technologies. This year has also marked the first attempts toward integrating silicon photonics with plasmonics and enabling the introduction of the small-size power-effective plasmonic structures in true interconnect applications. The first successful silicon–plasmonic coupling configurations have been reported, and switching by miniaturized thermo-optic plasmonic modules has been realized, resulting in the first efforts for high-throughput on-chip silicon–plasmonic router architectures.

Index Terms: Optical interconnects, optical routing, plasmonics, silicon photonics.

During the first decade of the 2000s, the field of optical communications has witnessed some of the most dramatic changes in both its application areas and its enabling technology quiver. Optical technology has gradually penetrated into shorter distance transmission links well below the 10-m range and is currently rapidly replacing copper cables in High-Performance Computing (HPC) and Data Center interconnects [1]. As parallel processing has turned to the accepted methodology for boosting HPC performance improvements, multiple processing cores are required to exchange a vast amount of information that can simply not be sustained by bandwidth-limited electrical interconnects [1]. This reality extends along a clearly shaped roadmap to finally bring optics "into-the-box" in order to address the steadily growing bandwidth need in the field of computing without leading, however, to new size and power consumption explosions. Today's world-leading Supercomputers already employ thousands of km's of optical fiber for their inter-rack connections in order to cope with aggregate data rates of several hundreds of gigabits per second and deliver Peta-flops computational powers [2], [3], requiring, however, a total area of a few hundreds of meters squared and several megawatts of power.

Facing the era of Exascale processing powers [2], [4], HPC size and power consumption emerge as the main set of barriers in trying to accommodate increased aggregate traffic rates. This has spurred intense research over the last five years toward completing the turn to optically interconnected processing machines and deploying photonic chips for the entire range of hierarchical system-levels: inter-rack, backplane, on-card, and even on-chip [1], [6]. The potential to drive down

energy and footprint requirements when increasing the utilization degree of optics has been recently highlighted by the demonstration of an 8 × 8 hybrid optoelectronic router for 10-Gb/s optical packets [7], which has led to a 10-fold reduction in energy consumption compared with the respective purely electronic routing solutions. Similar benefits were also demonstrated by the OSMOSIS optical packet switch prototype that offers a throughput of 2.5 Tb/s and extends complexity and line-rate capabilities to 64 input/output ports and 40 Gb/s, respectively, bringing great promise for utilization in supercomputer infrastructures [8]. To this end, major microelectronic vendors have started to heavily invest in research on novel next-generation computing architectures relying on the employment of nanophotonics and photonic Network-on-Chip (NoC) configurations [9]. The "Corona" [10] and "PROPEL" [11] research projects are recent examples that exploit hybrid optoelectronic routing with nanophotonic switching matrices for routing data in Chip Multi- and Many Processor (CMP) architectures with hundreds of interconnected cores. Respective efforts pursued at Columbia University have been reported during the last year to evaluate the scalability, performance, and realizability of photonic NoC-supported CMP designs [9], also taking into account physical-layer performance analysis [12].

The technology of choice for next-generation chip-level optical interconnection seems to come again from the silicon industry [5], [13]. Silicon photonics is considered as the mainstream integration platform for optical circuitry, offering attractive characteristics like low-loss optical signal propagation, high integration densities, and CMOS-compatible fabrication processes [14]–[16]. Silicon waveguides with sub-micron dimensions can serve as broadband optical gateways with more than 200 nm bandwidth [17] and typical optical loss coefficients lower than 2 dB/cm [18], [19]. Moreover, they have been demonstrated to successfully host most of the critical functions required for optical interconnect applications, including wavelength selective filtering elements [20], optical modulators [21], high-speed Ge-on-Si photodiodes [22], optical switching modules [23], and even optical lasing sources [24]. These rapid advances are gradually bringing silicon photonics into maturity so that this is now considered as the ideal low-loss interconnection platform.

The research outcomes of 2010 have additionally strengthened this belief, yielding some major technology breakthroughs: IBM's Terabus project demonstrated a 24-channel transceiver module that is capable of providing Tbps-class bidirectional aggregate data rates for board-level interconnects [25]. Intel has succeeded in demonstrating Wavelength Division Multiplexed (WDM) Photonic Integrated Circuit (PIC) devices with up to 200-Gb/s aggregate traffic rate capabilities [26] and active optical cable configurations with 4-wavelength 50-Gb/s transceiver hardware [27]. Fabrication processes have also made significant strides reporting sub-nanometer linewidth uniformities using CMOS technologies [28]. An important step has also been made toward highly functional modules through the integration of silicon with different material structures: Nonlinear organic materials combined with silicon waveguide technology have led to the successful demonstration of electrooptic modulation devices for higher modulation formats up to 100-Gb/s rates [29]. Similar remarkable achievements have also been made toward on-chip optical logic and memory circuits, originating through heterogeneous integration of III–V microdisk lasers on silicon-on-insulator (SOI) and leading to a novel optical flip-flop configuration with record low power consumption and footprint values [30].

However, with footprint and power consumption being the driving forces in next-generation chip-scale broadband interconnects, the search for disruptive enabling technologies capable of driving performance even beyond the limits of silicon photonics has already been initiated. Plasmonics have recently emerged as a very promising technology platform for driving down optical circuitry size [31], accompanied by expectations to address on-chip territories that lie beyond the reach of photonics and electronics [32], [33]. This new discipline relies on the propagation of electromagnetic waves known as Surface Plasmon Polaritons (SPPs) along a metal-dielectric interface. This leads to strong optical mode confinements, allowing for the deployment of optical structures with sub-wavelength dimensions, breaking, in this way, the size barriers of traditional diffraction-limited optics. On the same line, they allow for seamless interfacing of optical beams with electronic control signals through the underlying metallic film, providing, in this way, a natural energy efficient platform for merging broadband optical links with intelligent electronic processing, as currently considered to be the mainstream approach in CMP chip-scale architectures.

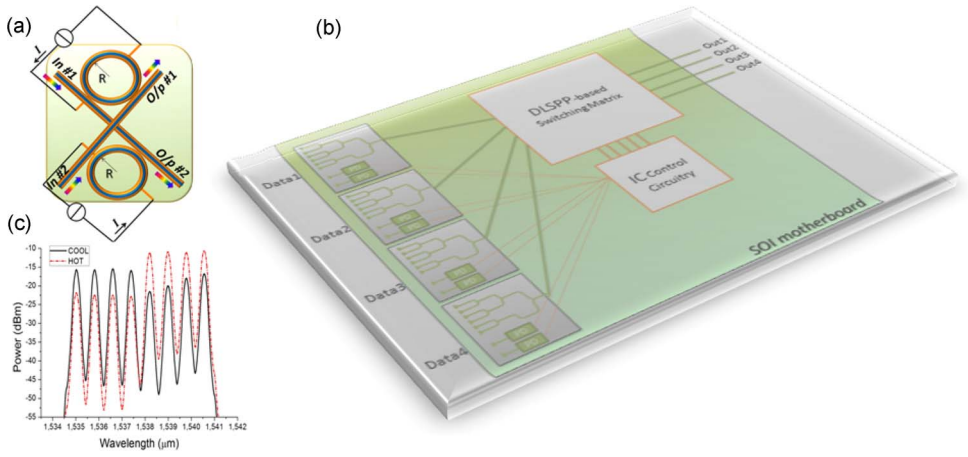

Fig. 1. (a) The layout of a dual-ring 2 × 2 DLSPP switch serving as the switching matrix on an SOI motherboard, shown in (b) in its design toward terabit-per-second routing interconnect applications. (c) 8 × 40 Gb/s-channel spectrum for both heated and unheated states of the switch at one output of the 2 × 2 silicon-plasmonic router, revealing extinction ratio values higher than 5 dB for all eight channels.

The interest in plasmonics has rapidly taken up during the last decade as a whole new class of plasmonic devices found its way to experimental demonstrations, mostly extending along different waveguiding [34]–[40] and passive filtering circuitry [41], [42]. Moreover, the area of "active plasmonics" has also made its first important steps toward allowing the control of plasmon propagation [43], also resulting in the demonstration of the first plasmonic nanolaser cavities [44]. However, the aim for bringing plasmonics intro true practical system-level applications at chip-scale environments is certainly still in its infant years, with the main achievement reported so far coming from a Korean consortium that demonstrated four-channel × 2.5 Gb/s board interconnects with Long-Range SPP waveguides serving as the transmission lines [45]. The main limiting factor in pushing plasmonics to additional system-level advances stems certainly from their high propagation losses, as most plasmonic waveguide structures restrict signal propagation over a few tens of micrometers due to internal damping of radiation in metal.

In this perspective, 2010 can be designated as a milestone toward turning plasmonics into practical circuitry for interconnect applications. The interfacing of plasmonic structures with the outer world has been realized for the first time, demonstrating effective optical fiber input and output coupling [46]. At the same time, efforts for coping with the high plasmonic propagation losses have concentrated on interfacing them with low-loss photonic waveguides, allowing for purpose-driven switching between photonic and plasmonic modes. Within this frame, a conductor-gap-Silicon SPP waveguide structure [47] and a polymer-on-gold DLSPP ring resonator end-coupled to SOI waveguides have been presented [48], both reporting on low coupling losses of 1 dB.

These achievements have raised expectations for the combined exploitation of silicon photonics and plasmonics for interconnection purposes, with plasmonics being used only where active functionality is required, while turning to low-loss silicon photonic structures when passive circuitry is needed. This concept is currently pursued by the European research project PLATON that has been initiated by the authors and was launched at the beginning of 2010. PLATON envisions the deployment of terabit-per-second router fabrics relying on the deposition of DLSPP-based switching matrices on a SOI motherboard that will host all necessary waveguiding, multiplexing, filtering, and signal detection elements, as well as the electronic control driving circuit [49] (see Fig. 1). This consortium has already achieved remarkable advances in DLSPP switching configurations both at the experimental [50], [51] and at the theoretical level [52]–[54], exploiting thermo-optics to alter the state of DLSPP waveguide ring resonator or Mach–Zehnder interferometric switching elements. We have also presented the first silicon–plasmonic 2 × 2 router architecture that is capable of providing up to 320 Gb/s throughput performance [49], relying on the employment of a novel dual-ring

DLSPP switching module and indicating the potential for driving down size and power consumption metrics. On the same line, the efforts to advance and benefit from the functional portfolio of DLSPPs have led to the demonstration of power monitoring [55], as well as to a new type of Long-Range DLSPP waveguides that can enhance the propagation length of plasmons, allowing for increased interaction lengths between optical and electrical signals [56]. These advances can only suggest that the successful merger of plasmonics with silicon photonics toward true interconnect routing applications is indeed headed in the right direction, rendering the next few years as a very promising period for on-chip silicon–plasmonic router implementations.

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