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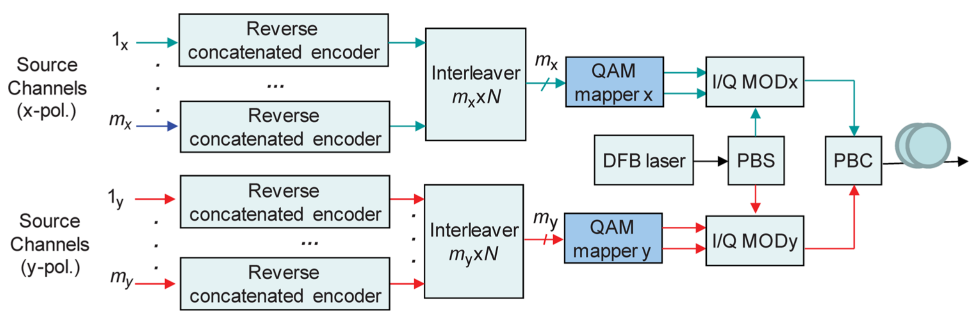

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Reverse Concatenated Coded Modulation for High-Speed Optical Communication

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Abstract: We propose the reverse concatenated code as a forward error correction (FEC) scheme suitable for beyond 100-Gb/s optical transmission. In this scheme, BCH code is used as inner code and low-density parity-check (LDPC) code as outer code. The BCH decoder is implemented based on maximum *a posteriori* (MAP) decoding such as the BCJR/Ashikmin's algorithm, and an LDPC decoder is based on a min-sum-with-correction-term algorithm. Because maximum *a posteriori* (MAP) decoding is used as the inner decoder, it provides high accuracy reliabilities to be used in LDPC decoding. We show that proposed FEC scheme performs comparably with much longer LDPC codes of girth 12 for a smaller number of LDPC decoder iterations. Because the outer LDPC code is of medium length and the number of required iterations is low, the proposed concatenated scheme represents an interesting candidate to be used in beyond 100-Gb/s optical transmission. The net coding gain (NCG) of concatenated LDPC(16935,14819)-BCH(64,57) code is 9.62 dB at a bit error rate (BER) of 10^{-9}, whereas the expected NCG at BER of 10^{-13} is 11.38 dB. This concatenated code outperforms the corresponding turbo-product counterpart with a Chase II decoding algorithm by 0.94 dB at BER of 10^{-9}.

Index Terms: Fiber-optics communications, forward error correction (FEC), low-density parity-check (LDPC) codes, coded modulation, reduced-complexity decoding.

1. Introduction

As the response to high-bandwidth demands due to rapid growth of data-centric and multimedia applications and deployment of broadband access networks, network operators are upgrading their dense wavelength division multiplexing (DWDM) networks from 10 Gb/s per wavelength channel to more spectrally efficient 40 Gb/s and 100 Gb/s [1]. In order achieve beyond 100 Gb/s per wavelength optical transmission using commercially available equipment operating at lower speed, we have recently proposed the use of low-density parity-check (LDPC) coded modulation [2]–[4]. In particular, the LDPC-coded modulation based on large girth (> 10) LDPC codes provides excellent performance. The codeword lengths are unfortunately too high for quasi-cyclic (QC) LDPC code design, and corresponding decoders are difficult to implement with currently available field programmable gate array/very large scale integrated hardware. On the other hand, through the use of concatenated codes, the target net coding gains (NCGs) can be achieved, even with shorter LDPC code of lower girth (6 or 8). Unfortunately, short LDPC codes of low girth (6 or 8) and reasonable LDPC decoder complexity (column weight 3 with min-sum-with-correction-term algorithm) exhibit an error floor in the region of interest for optical communications. In a series of articles by Mizuochi *et al.* [5]–[7], the girth 6 LDPC codes were used as inner codes, and RS codes were used as outer codes. With this approach, the error floor of low girth LDPC codes is lowered, and the target NCGs are obtained. However, the NCG is far below that of large girth LDPC codes.

In order to achieve the bit error rate (BER) performance of large girth LDPC codes with short concatenated codes, we propose to use the LDPC code of girth 8 and column weight 3 as outer LDPC code and BCH or Reed–Muller (RM) code as the inner code. Because BCH and RM codes can be efficiently decoded using maximum *a posteriori* (MAP) probability due to the Ashikhmin and Litsyn [8] or the BCJR algorithm [9], the reliable bit log-likelihood ratios (LLRs) can be forwarded to outer LDPC decoder. It will be shown later in the paper that with reasonable short LDPC codes, we can achieve the BER performance and NCG comparable with large girth LDPC codes with such reverse concatenated code. Notice that the proposed scheme is different from reverse concatenated scheme due to Bliss [11], which is used in constrained (modulation) coding systems [12]–[14]. In conventional constrained coding, the inner code is constrained code, while outer coded is an FEC code. In the reverse constrained concatenation scheme, the inner code is systematic FEC code in which information bits are unchanged so that they can be encoded by outer constrained code. Further, an additional constrained code is used to impose channel constraints on parity bits from the FEC code. This scheme is used to deal with propagation errors introduced by the constrained decoder. The reverse concatenation scheme proposed in this paper is related to channel codes only and is based on different principles from constrained coding.

The paper is organized as follows. In Section 2, the proposed reverse concatenated coded modulation scheme, which is suitable for beyond 100 Gb/s optical transmission, is described. In Section 3, we study the performance of the proposed scheme. Some important concluding remarks are provided in Section 4.

2. Reverse Concatenated Coded Modulation for High-Speed Optical Transport

The polarization-multiplexed (PolMUX) coded quadrature amplitude modulation (QAM) scheme that is suitable for beyond 100 Gb/s per wavelength optical transmission is shown in Fig. 1. The $m_x + m_y$ (index x (y) corresponds to x- $(y$-$)$ polarization) independent data streams are encoded using different reverse concatenated codes [see Fig. 1(a)] of code rates $R_i = K_i/N$ $(i \in \{x, y\})$, where $K_x(K_y)$ denotes the number of information bits used in the binary concatenated code corresponding to x- $(y$-$)$ polarization, and N denotes the codeword length. The m_x (m_y) input bit streams from m_x (m_y) different information sources pass through identical concatenated encoders of code rate R_x (R_y). The reverse concatenated code is implemented, as shown in Fig. 1(c), based on LDPC code as the outer code and either BCH or RM code as the inner code. The outputs of the encoders are then bit-interleaved by an $m_x \times N(m_y \times N)$ bit-interleaver, where the sequences are written row-wise and read column-wise from a block-interleaver. The mapper maps each m_x (m_y) bits, taken from the interleaver, into a 2^{mx}-ary (2^{my}-ary) QAM signal constellation point based on the lookup table (LUT). The QAM mapper x (y) assigns m_x (m_y) bits to a constellation point represented in polar/Cartesian coordinates as $\boldsymbol{s}_{i,x} = |\boldsymbol{s}_{i,x}|\exp(j\phi_{i,x}) = (\boldsymbol{s}_{i,x}^{(\mathrm{I})}, \boldsymbol{s}_{i,x}^{(\mathrm{Q})})[\boldsymbol{s}_{i,y} = |\boldsymbol{s}_{i,y}|\exp(j\phi_{i,y}) = (\boldsymbol{s}_{i,y}^{(\mathrm{I})}, \boldsymbol{s}_{i,y}^{(\mathrm{Q})})]$, where we used I and Q indices to denote in-phase and quadrature channels, respectively. To facilitate implementation at high speed, we use $(m_x + m_y)$ encoders/decoders operating in parallel at a data rate of R_b instead of only one encoder/decoder operating at date rate of $(m_x + m_y)R_b$, which is a common approach in wireless communications.

At the receiver side [see Fig. 1(b)], the outputs at the I- and Q-branches in two polarizations are sampled at the symbol rate, while the symbol LLRs are calculated as follows:

$$\lambda(\boldsymbol{q}) = \log\left[\frac{P(\boldsymbol{q}|\boldsymbol{r})}{P(\boldsymbol{q}_0|\boldsymbol{r})}\right] \tag{1}$$

where $\boldsymbol{q}$ and $\boldsymbol{r}$ denote the transmitted signal constellation point and received symbol at time instance i (in either x- or y-polarization), respectively, and $\boldsymbol{q}_0$ represents the reference symbol. The turbo equalization principle [3] is used to compensate for various channel impairments such as

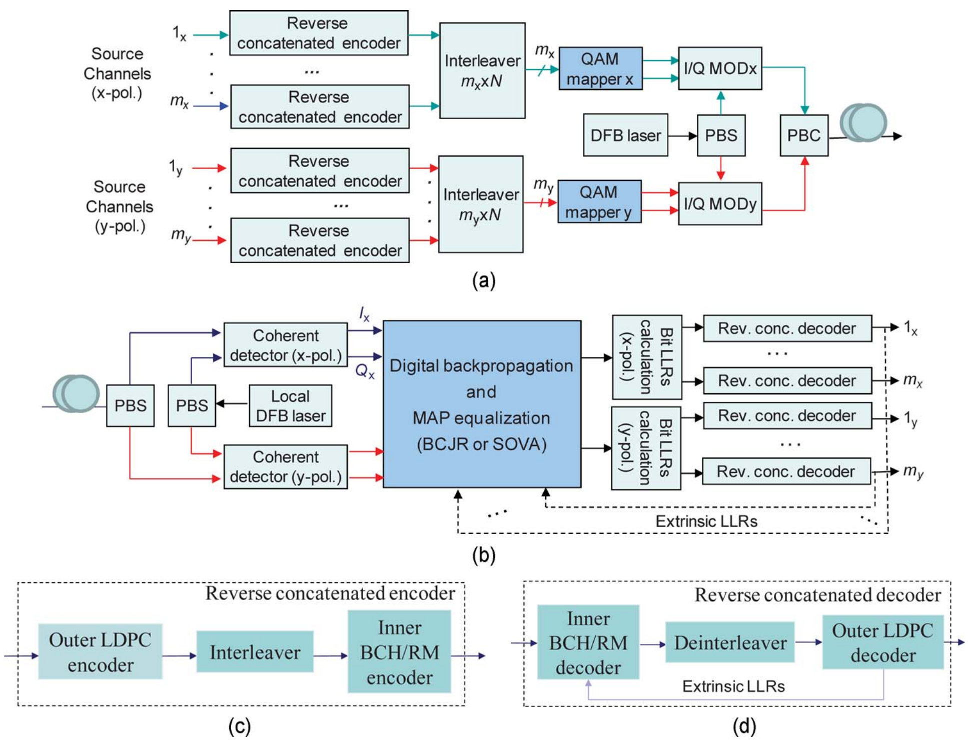

Fig. 1. PolMUX reverse concatenation coded QAM scheme. (a) Transmitter configuration, (b) receiver configuration, (c) reverse concatenated encoder, and (d) reverse concatenated decoder.

polarization-mode dispersion (PMD), residual chromatic dispersion, and fiber nonlinearities. Since turbo equalization is not the topic of this paper, we assume that channel impairments are ideally compensated for. The receiver side digital back propagation can also be used in combination with turbo equalization. For more details on turbo equalization and digital back-propagation, see [15]. Let us denote by c_j the jth bit in the observed symbol $\boldsymbol{q}$ binary representation $\boldsymbol{c} = (c_1, c_2, \ldots, c_l)$. The bit LLRs $L(c_j)$ are determined from symbol LLRs by

$$L(c_i) = \log \frac{\sum_{c:c_i=0} \exp[\lambda(q)] \exp\left(\sum_{c:c_j=0, j\neq i} L_a(c_j)\right)}{\sum_{c:c_i=1} \exp[\lambda(q)] \exp\left(\sum_{c:c_j=0, j\neq i} L_a(c_j)\right)} \tag{2}$$

and forwarded to the concatenated decoder. Therefore, the ith bit reliability is calculated as the logarithm of the ratio of a probability that $c_i = 0$ and a probability that $c_i = 1$. In the nominator, the summation is done over all symbols q having 0 at the position i, while in the denominator, it is over all symbols q having 1 at the position i. With $L_a(c_j)$, we denoted *a priori* information determined from the concatenated decoder extrinsic LLRs. The inner summation in (2) is performed over all bits of symbol q, which have been selected in the outer summation, for which $c_j = 0$, $j \neq i$. By iterating the extrinsic reliabilities between MAP detector and concatenated decoder, the overall BER performance can be improved. The reverse concatenated decoder is shown in Fig. 1(d) and is composed of BCH/RM decoder as the inner decoder, deinterleaver, and outer LDPC decoder. The BCH/RM decoder is implemented based on BCJR or Ashikmin's algorithms and LDPC decoder on the min-sum-with-correction-term algorithm [10]. Therefore, there are two key differences of the proposed scheme with respect to the conventional concatenated schemes due to Mizuochi *et al.*: 1) The positions of LDPC code and BCH code are reversed, and 2) the BCH decoder is implemented as soft MAP decoder, while the RS decoder in [5]–[7] is based on the Massey–Berlekamp hard-decision decoding algorithm [3]. Notice that one may want to use the concatenation scheme with soft decoding in a conventional

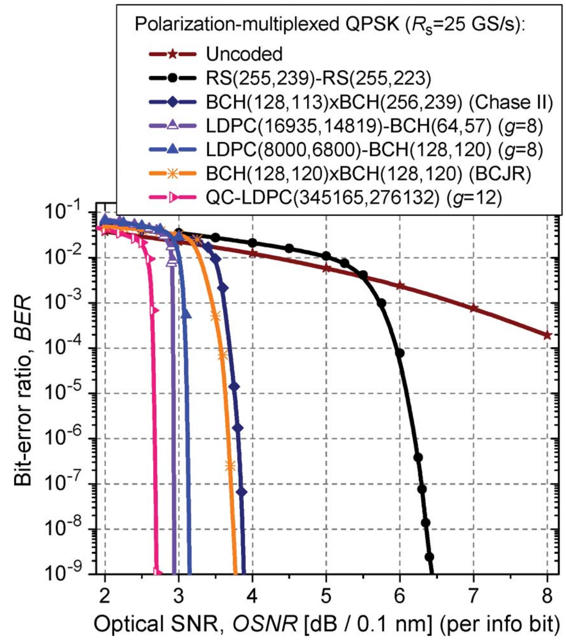

Fig. 2. BER performance of PolMUX concatenated LDPC-BCH coded QPSK. (R_s denotes the information symbol rate.)

way. However, LDPC decoding is based in sub-optimum belief-propagation algorithms so that it is not suitable to be used as inner code. To improve the performance of the concatenated decoder, we allow the iteration of extrinsic LLRs between the BCH/RM decoder and the LDPC decoder. For example, the extrinsic LLR of the jth bit for the BCH decoder in the kth iteration is determined by

$$L_{\mathrm{BCH},e}\left(c_j^{(k)}\right) = L_{\mathrm{LDPC}}\left(c_j^{(k)}\right) - L_{\mathrm{LDPC}}\left(c_j^{(k-1)}\right) \tag{3}$$

where $L_{\mathrm{LDPC}}(c_j)$ is corresponding LLR of bit c_j after LDPC decoding, while indices k and $k-1$ are used to denote the current and previous iterations. Another option to determine the extrinsic information for the BCH decoder is as the difference between the LDPC decoder output and input LLRs.

3. Performance Evaluation

The results of simulations of PolMUX based BCH-LDPC coded quadrature phase-shift keying (QPSK) scheme with 100 Gb/s in aggregate data rate are shown in Fig. 2. Corresponding encoders, decoders, mappers, and demappers operate at data rate ~32 Gb/s, depending on the code rate of the concatenated scheme, while ensuring that the aggregate data rate is 100 Gb/s. The aggregate data rate is obtained as $2 \times 2 \times R \times R_s$ (the first factor 2 originates from two orthogonal polarizations, the second factor 2 from 2 bits carried per single QPSK symbol, R denotes the code rate, and R_s denotes the symbol rate). The symbol rate is varied so that the aggregate rate of 100 Gb/s is achieved.

Notice that the complexity of the BCJR algorithm is about two to three times higher than that of the Viterbi algorithm and imposes no implementation difficulty for reasonably short BCH codes considered in this paper. Nevertheless, to reduce the complexity of the BCJR decoding algorithm, one may use the lower complexity algorithm described in [8] or some other reduced complexity BCJR algorithm such as the M*-BCJR algorithm [16] or the heuristic survivors selection reduced complexity BCJR-type algorithm [17].

The concatenated LDPC(16935,14819)-BCH(64,57) code, for five outer BCH-LDPC iterations and 10 LDPC inner iterations, outperforms the corresponding turbo-product counterpart with the Chase II decoding algorithm by 0.94 dB at BER of 10^{-9}. The component LDPC code is of girth 8 and column weight 3, and it is obtained by modified progressive edge growth [18]. We have shown in [18], that this class of LDPC codes performs comparably with the QC LDPC code design [3, ch. 11, Sec. 11.1]. The equivalent QC LDPC(16920,14805) code has the following parameters: column weight 3, row weight 24, and permutation block size 705. The same concatenated code outperforms the product BCH(128,120)xBCH(128,120) code, which operates based on the BCJR algorithm with 10 iterations by 0.81 dB. The improvement over the conventional RS(255,239)-RS(255,223) code is 3.49 dB. The NCG of the LDPC(16935,14819)-BCH(64,57) code is 9.62 dB at the same BER, while the NCG at BER of 10^{-13} is 11.38 dB. The proposed concatenated code is only 0.25 dB away from girth-12 QC-LDPC code of length 345165, column weight 3, row weight 15, and permutation matrix size of 23011. The girth-12 LDPC decoder operates with 50 iterations in the corresponding log-domain sum-product algorithm. Notice that the complexity of sum-product algorithm is dominated by the check-node update rule, which requires $15(d_c - 2) \times (n - k)$ additions, where d_c is the check-node degree. Therefore, the complexity of the LDPC(16935,14819) code is 32.16 times lower than that of the LDPC(345165,276132) code. In addition, since the length of the girth-12 LDPC code is 20.38 times longer, it will occupy much more space in a real silicon-device. Moreover, the decoding latency will be much higher for long LDPC code.

4. Conclusion

The reverse concatenated BCH-LDPC code is proposed as an FEC scheme that is suitable for beyond 100 Gb/s optical transport. Contrary to the conventional concatenated schemes, in this scheme, the BCH code is used as inner code and the LDPC code as outer code. The BCH decoder is implemented based on MAP decoding, while the LDPC decoder is based on the min-sum-with-correction-term algorithm. Because the MAP decoding is used as the inner decoder, it provides high accuracy reliabilities to be used in LDPC decoding.

We show that proposed FEC scheme performs comparably with much longer LDPC codes of girth 12 for a smaller number of LDPC decoder iterations. Because the outer LDPC code is of medium length, and the number of required iterations is low, the proposed concatenated scheme represents an interesting candidate to be used in beyond 100 Gb/s optical transmission. The NCG of concatenated LDPC(16935,14819)-BCH(64,57) is 9.62 dB at BER of 10^{-9}, while the expected NCG at a BER of 10^{-13} is 11.38 dB. The same concatenated code outperforms the corresponding turbo-product counterpart with the Chase II decoding algorithm by 0.94 dB at a BER of 10^{-9}.

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