SSCS-Green Mountain Organizes 17th IEEE North Atlantic Test Workshop

IEEE NATW Special Session on Solid-State Circuits & System Test Held on 14-16 May, 2008

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For the first time this year, the IEEE North Atlantic Test Workshop (NATW) included a special session on solid-state circuits and system test. Sponsored by the SSCS-Green Mountain chapter at the Holiday Inn in Boxborough, Mass. on May 14-16, 2008, the conference served as a forum for discussions on the latest issues relating to high quality, economical, and efficient testing methodologies and designs.

Special SSCS Session Highlights System Resiliency

The special SSCS session discussed both technical and business implications of technological and system resiliency challenges, featuring presentations on three aspects of this crucial problem:

- Advances in Built-in Self-Test for 65nm and 45nm technology nodes
- Adaptive Test
- On-product reliability testing.

The contributions in these papers demonstrated significant technical advances toward addressing system resiliency challenges and covered issues, possibilities, limitations and future needs.

High reliability, fault protection and high resiliency are key requirements for high-performance systems. Embedded processors and embedded memory macros are having an ever increasing impact on system resiliency, not only in servers, high-performance computing, enterprise storage and data centers, but also in gaming and digital multimedia applications.

"Improving Memory BIST Value in a Tough Real Estate Market," by M. Ouellette, M. Ziegerhofer, V. Chickanosky, S. Granato, P. Rachakonda, C. Mirashi, S. Jinagar and K. Gorman (IBM)

A programmable BIST architecture and fuse circuit design that supports at-speed test with reduced test/repair circuit overhead, this paper featured an embedded serial BIST control interface allowing for in-system and diagnostic capabilities.

"Cost-Benefit Analysis for Functional Pattern Test Time Management," by M. Lee, M. Grady, M. Johnson (IBM)

A cost-benefit analysis methodology for test pattern efficiency, identifying actions that could be taken to help keep test escapes and quality impacts to a minimum while allowing adaptive test pattern reduction.

"On-Chip Circuit for Monitoring Degradation Due to NBTI," by K. Stawiasz, K. Jenkins and P-F. Lu (IBM)

A circuit implementation with sufficient accuracy, resolution and power supply noise immunity to enable the characterization of NBTI-induced frequency degradation on product chips under typical product operating voltage and temperature.

More information about the 2008 NATW can be found at: www.ewh.ieee.org/r1/vermont/



SSCS-Green Mountain Chair Pascal Nsame presented certificates of appreciation to Mike Ouellette (left), Matt Grady (center) and Kevin Stawiasz (right) at the special SSCS session of the IEEE North Atlantic Test Workshop (NATW) in May, 2008.