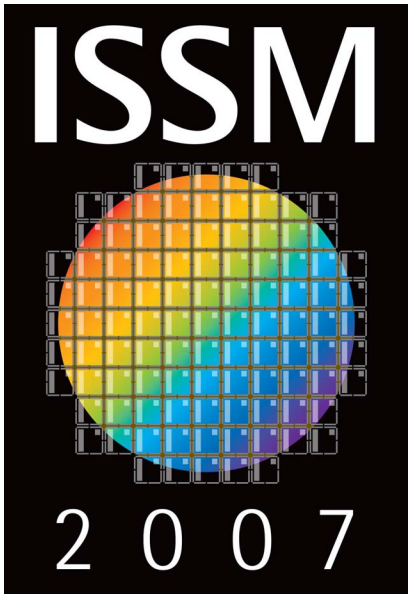

2007 International Symposium on Semiconductor Manufacturing

Conference Proceedings

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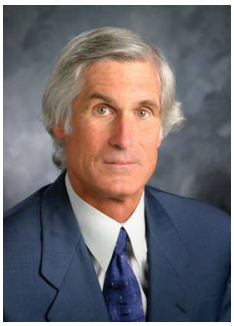
Message from the ISSM 2007 Executive Committee Chair

Jim Doran
International Executive Committee
COO
Spansion, Inc.



I would like to welcome all of you who have come from all over the world to the 16th Annual 2007 International Symposium on Semiconductor Manufacturing with representation from approximately fourteen countries. It is really a great pleasure to have you all here.

Those of us who have built careers in this industry know it as an exciting industry....one where a day rarely goes by when we can't say "I learned something new today." Where else could you work where you could literally learn something new every day of your life? The manufacturing side of our industry is also a fascinating blend of technology, people, teams, and business.

This year we are trying something unique. In addition to what I sincerely hope are great opportunities to learn something about semiconductor manufacturing, we have a rich lineup of CEO executives from our industry to provide context for all of us on what the challenges facing us are and how the CEOs of the world's leading companies plan to deal with those challenges. For the first time ever, we've also added a panel of the top analysts and financial experts who follow, analyze, report, advise, and invest in our industry so you can receive and understand their perspectives on what the driving forces are behind our industry and why some of the changes you read about are happening. It is our hope as an executive committee (and my personal hope), that you find this a rich environment in which to learn something you can apply at your company to keep our industry alive and vibrant. It could result in one of the principal driving forces that shape our world as a better place to live and work.

Sincerely,

Jim Doran, COO
Spansion Inc.

Message from ISSM Japan Committee

Michihiro Inoue
Chairman of ISSM Japan Executive Committee
Technical Advisor
Semiconductor Company
Matsushita Electric Industrial Co., Ltd.

On behalf of the International Symposium on Semiconductor Manufacturing (ISSM) Japan Organizing Committee, Japan Executive Committee, and Japan Program Committee, it is a great pleasure and honor for us to have you at the sixteenth annual ISSM.

The ISSM made its debut in 1992 in Tokyo under strong support by the leaders of semiconductor industries and academia and has been held annually in the U.S. and Japan alternatively. With the motto, "Making know-how to science," the symposium has been aiming to systematize and universalize the semiconductor manufacturing technologies which had required know-how and experiences on the job, and to contribute to the continuous further growth of semiconductor industries. The industry where “Moore’s Law” has played a core role is now shifting to “More than Moore”. We are now reaching a significant milestone where the industry will be driven by different factors. The device scaling and large wafer diameter used to be a vital to the development of the advanced semiconductor technology and contribute to the cost reduction, however they are not driving the industry growth any more as they did in the past. Our mission plays more important role.

Recently many emerging manufacturing technologies such as new process and equipment control technologies, fault detection & classification (FDC) technology, design for manufacturability (DFM) technology, advanced metrology, and virtual metrology have been developed and implemented to achieve the improvement of productivities. Those epoch-making technologies do not just deal with the issues of manufacturing technologies but also require more collaborative solution with design and device development areas. Furthermore, it is strongly expected to be discussed from the various view points including environment, safety, and health, supply chain, and information processing. ISSM will continue to provide the opportunity to discuss those core issues to the global semiconductor industry and to contribute to further growth of the industry.

Japan has decreased drastically its global market share of device manufacturing , however, still continues to be responsible for further global development of semiconductor manufacturing technologies with its high level of technology strength of entire semiconductor supply chain including device, equipment, materials, and components. ISSM Japan committees recognize the value of Japan in its responsibility and continue to contribute to globalize and universalize of semiconductor manufacturing technologies through ISSM.

The 17th annual ISSM in 2008 will be held in Japan on October 29-31, 2008. The ISSM has been engaged in continuous challenging for advanced technologies from global view points and bringing the developed technologies to the real market.

I sincerely hope that ISSM 2007 will provide an exciting and interactive discussion among the engineers and scientists from all over the world in the semiconductor manufacturing related areas.

ISSM 2007
Committee Membership

The ISSM organization is governed by committees in both the US and Japan. Committees members include individuals representing several semiconductor manufacturing related companies. Each year, members dedicate significant time to ensuring that the ISSM conference is successful in bringing people together to learn the latest innovations and advancement in the industry.

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CPMT IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY	**IEEE Components, Packaging, and Manufacturing Technology Society (CPMT)** The CPMT Society encompasses the materials science, chemical processes, reliability technology, mathematical modeling, education and training utilized in the design and production of discretes, hybrids, and electronic packaging. Also included are fiber optics, connector technology, and semiconductor processing. Manufacturing technology includes systems, concepts, management, and quality as they relate to electronic component manufacturing.
	Japan Society of Applied Physics (JSAP) JSAP was established as an official academic society in 1946, and since then, it has been a leading academic society in Japan. The society's interests cover a broad variety of scientific and technological fields, and JSAP continues to explore state-of-the-art and interdisciplinary topics.
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ISSM 2007: Program-at-a-Glance

Marriott Hotel ~Santa Clara, CA U.S.A.
October 15-17, 2007

Monday, October 15, 2007	
7:00-9:00AM	**Registration Desk Open for Check-in** *California Ballroom Registration Desk*
7:00-7:45 AM	**Speaker Breakfast (for speakers and co-chairs scheduled on Monday)** *Hall of Cities- Seattle*
	General Assembly Begins- California Ballroom, Salon 6
8:00 AM	**Welcome** *Tom Sonderman, International Program Committee Chairman*
8:10 AM	**Twelve Types of Innovation That Will Save Your Company** *Keynote Speaker: Rich Karlgaard, Publisher of Forbes*
9:05 AM	**Rising Role of Indirect Materials for Semiconductor Manufacturing** *Keynote Speaker: Susuma Kohyama, President and CEO, Covalent Materials Corp.*
10:00AM	**Break** ***Sponsored by WeSRCH.com***

	Track 1 *California Ballroom, Salon 6*		**Track 2** *California Ballroom, Salon 4*
10:15 AM - 11: 55 AM	***MS: Manufacturing Strategy and Operations Management Session***	**10:15 AM – 11:55 AM**	***PC: Process and Equipment Control Session Starts***
12:00 PM	**Attendee Lunch** *Hall of Cities*		
	General Assembly- California Ballroom, Salon 6		
1:00 PM	**Less is More** *Keynote Speaker: Paul Westbrook, Senior Technologist, Texas Instruments*		
2:00 PM- 2:48 PM	***Track 1: 3-minute Poster Session Presentations (MS, PT, DM)***	**2:00 PM- 2:48 PM**	***Track 2: 3-minute Poster Session Presentations (PC)***
2:55 PM- 3:35 PM	***SC: Supply Chain Integration Session***	**2:55 PM- 3:35 PM**	***PC: Process and Equipment Control Session Continues***
3:35 PM	**Break**		
3:45 PM- 5:45 PM	***PE: Advanced Process and Metrology Equipment Session***	**3:45 PM- 5:25 PM**	***Process and Equipment Control Session Completes***
6:15 PM – 8:00 PM	**Attendee Dinner Reception** *To be held at the Pool and Courtyard Area* Executive Committee Comments begin promptly at 6:15 PM Drawing and Announcement of Winner for Wild Photons Gift Certificate ***Entertainment sponsored in part by Spansion***		

ISSM 2007: Program-at-a-Glance

Marriott Hotel ~Santa Clara, CA U.S.A.
October 15-17, 2007

Tuesday, October 16, 2007	
7:00-9:00AM	**Registration Desk Open for Check-in** *California Ballroom Registration Desk*
7:00-7:45 AM	**Speaker Breakfast (for speakers and co-chairs scheduled on Tuesday)** *Hall of Cities- Seattle*
	General Assembly Begins- California Ballroom, Salon 6
8:00 AM	**Welcome** *Tom Sonderman, International Program Committee Chairman* *Award Presentation: IEEE Transactions on Semiconductor Manufacturing Best Paper for 2006*
8:15 AM	**Optimizing Memory Operations at the Leading Edge** *Keynote Speaker: Mark Durcan, COO, Micron*
9:10 AM	**Challenges and Opportunities Facing the Semiconductor Industry** *Keynote Speaker: Jackson Hu, CEO, UMC*
10:05 PM	**Break**

	Track 1 *California Ballroom, Salon 6*		**Track 2** *California Ballroom, Salon 4*
10:20 AM- 11:20 AM	***FD: Factory Design and Automated Material Handling Session***	**10:20 AM- 12:00 PM**	***MC: Manufacturing Control and Execution Session***
11:25 AM- 12:00 PM	***PT: Advanced Packaging and Test Session***		
12:05 PM	**Attendee Lunch** *Hall of Cities*		
	General Assembly- California Ballroom, Salon 6		
12:50 PM	**Technology and the Equipment Industry** *Keynote Speaker: Nick Bright, Executive Vice President Products, LAM Research*		
2:00 PM- 3:08 PM	***Track 1: 3-minute Poster Session Presentations (ES, MC, PO)***	**2:00 PM- 3:12 PM**	***Track 2: 3-minute Poster Session Presentations (PE, YE, FD)***
3:15 PM	**Break**		
3:30 PM- 4:50 PM	***DM: Design for Manufacturing Session***	**3:30 PM- 4:50 PM**	***ES: The Green Factory- The Role ESH Session***
5:15PM – 7:30PM	**Interactive Poster Session Reception** *Grand Ballroom*		

ISSM 2007: Program-at-a-Glance

Marriott Hotel ~Santa Clara, CA U.S.A.
October 15-17, 2007

Wednesday, October 17, 2007	
7:00-9:00AM	**Registration Desk Open for Check-in** *California Ballroom Registration Desk*
7:00-7:45 AM	**Speaker Breakfast (for speakers and co-chairs scheduled on Wednesday)** *Hall of Cities- Seattle*
7:00–8:00 AM	**Attendee Breakfast** *Hall of Cities- Newport Beach, Santa Barbara, Portland* ***Sponsored by SEMI***
	General Assembly Begins- California Ballroom, Salon 6
8:00 AM	**Welcome** *Tom Sonderman, International Program Committee Chairman*
8:10 AM	**Optimizing Fab Performance** *Keynote Speaker: Michael Splinter, CEO, Applied Materials*
9:05 AM	**"One Touch" Supply Chain** *Keynote Speaker: Susan Graham Johnston, Vice President, Volume System Operations, Sun Microsystems*
10:00AM	**Break**

Track 1 *California Ballroom, Salon 6*		Track 2 *California Ballroom, Salon 4*	
10:15 AM- 11:55 AM	***YE: Yield Enhancement & Contamination Control Session Starts***	**10:15 AM- 11:55 AM**	***PO: Process and Material Optimization Session Starts***
12:00 PM	**Lunch (not provided)**		
1:00 PM	**General Assembly Begins- California Ballroom, Salon 6** **"Going Private… Or Remaining Public?"** **Financial Panel Discussion** ***Moderators:*** • Mihir Parikh, President & CEO, Aquest Systems • Frank Quattrone, Chairman of the Board, Tech Museum of Innovation ***Panelists:*** • Michael Grimes -- Morgan Stanley, Head of Global Technology Investment Banking • Chip Schorr - Blackstone, Senior Managing Director, Private Equity Group • Rex Sherry - Bear Stearns, Senior Managing Director, Head of West Coast Technology Investment Banking • Dipanjan "DJ" Deb - Francisco Partners, Managing Partner		
2:00 PM- 2:40 PM	***YE: Yield Enhancement & Contamination Control Session Completes***	**2:00 PM- 3:00 PM**	***PO: Process and Material Optimization Session Completes***
3:05 PM	**Final Note - Conference Ends**		

2007 Invited Speakers

Thank you to our invited speakers.
(listed in alphabetical order)

Presentation time:
Tuesday,
October 16th
12:50pm
California Ballroom-Salon 6

Nick Bright

Executive Vice President Products, Lam Research Corporation

"History & Future of the Semiconductor and Equipment Industries"

As the industry faces increased pressures and a more competitive operating environment staying on the edge of innovation is more important than ever before. Attend this presentation to learn more about how we can leverage the equipment industry to maximize operational efficiencies at the leading edge.

Historically, Moore's Law has been used as the guiding light for cost and performance in the semiconductor industry. Will this be the case going forward? If not, how will it affect the equipment companies?

Related ISSM Topics: Manufacturing Strategy and Operations Management, Process & Material Optimization

Biography

Nick Bright is executive vice president of products at Lam Research Corporation, focusing on new business opportunities and markets. Nick joined the company in 1998 and successfully led Lam's 2300 ® businesses from research and development to market positioning and penetration. He has held various management positions within the company, including executive vice president of global products and regional operations, vice president of technology and engineering, and senior vice president and general manager of products.

Prior to joining Lam, Bright spent 16 years at Applied Materials, Inc., where he held a variety of management positions in engineering and technology groups within etch, ion implant, and automation. Before joining Applied Materials, Bright held management positions at General Electric Co. in the United Kingdom and ABB in Sweden.

Bright holds bachelor of science and master's degrees in electrical and electronics engineering from Brunel University in England.

Lam is a major supplier of wafer fabrication equipment and services. The leader in dry etch for the past several years, Lam has expanded its activities into adjacent market segments like single wafer wet clean, bevel clean, strip, and patterning enhancement to extend the capability of advanced lithography.

Presentation time:
Tuesday,
October 16th
8:15am
California Ballroom-Salon 6

Mark Durcan

Chief Operating Officer, Micron Technology, Inc.

"Optimizing Memory Operations at the Leading Edge"

The memory industry continues scaling with Moore's law and in some instances exceeds the historical trend. Capital investment to support manufacturing scale at the leading edge also continues to grow. As a result, carefully optimizing manufacturing capacity while synchronizing with the most effective process technology solutions is critical. World class efficiency requires methodical coordination of process and product roadmaps from conception to end-of-life, while also considering manufacturing capacity and transitions.

Related ISSM Topics: Manufacturing Strategy and Operations Management, Manufacturing Control and Execution, Process & Material Optimization, Design for Manufacturing, Advanced Processing Technology

Biography

Mark Durcan is Chief Operating Officer for Micron Technology, a leading provider of advanced semiconductor and CMOS image sensor solutions. He joined Micron in 1984 as a diffusion engineer and has held a variety positions including process integration engineer, process integration manager, process development manager, Chief Technical Officer, and Vice President of Research and Development.

Durcan is responsible for Micron's worldwide manufacturing, and currently serves on the boards of the IM Flash, LLC; Tech Semiconductor, MP Mask, LLC; and the EUV LLC.

Durcan holds a bachelor of science degree and a master's degree in chemical engineering from Rice University.

Presentation time: Tuesday, October 16th 9:10am California Ballroom- Salon 6

Dr. Jackson Hu

Chairman and Chief Executive Officer,
United Microelectronics Corporation

"Challenges and Opportunities Facing the Semiconductor Industry"

Several factors are affecting the semiconductor industry today and the dynamics of IDM, fabless design companies and foundries will be discussed.

IDMs are increasingly adopting a "fab-lite" or even fabless approach due to the tremendous investment associated with developing and manufacturing today's most advanced ICs. This trend certainly offers many opportunities for the foundry sector. However, putting a fab-lite strategy into practice is no simple matter. At the same time, leading fabless design companies face the pressures caused by limited design resources and the need to enhance competitiveness by establishing multiple sources for product manufacturing.

As process technologies shrink, the introduction of new materials and equipment continues unabated. This has led to uncertainties in process technology development that could slow the cycles observed by Moore's Law. As a result, these challenges have made design for manufacturability (DFM) even more critical. Although the smaller geometries allow the possibility of an entire system to be implemented on a single chip, the design community may have underutilized the shrinking process geometry in the rush to embrace the next node associated with Moore's law. These factors will require the design, EDA and manufacturing communities to re-examine their approach going forward.

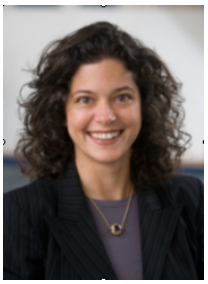
Related ISSM Topics: Manufacturing Starategy and Operations Management, Design for Manufacturing, Advanced Processing Technology

Biography

Dr. Jackson Hu is the Chairman and CEO of UMC, a worldwide leading semiconductor foundry. Dr. Hu possesses extensive experience in the IC design industry in the fields of microprocessors, graphics, and wireless communications. In his capacity as Chairman and CEO, he has leveraged his design expertise to assist UMC to develop comprehensive solutions enabling the production of leading-edge SOCs in a cost-effective foundry environment.

Before joining UMC, Dr. Hu served as President and CEO of SiRF Technology, a fabless communications IC and IP company focused on GPS-based location technology. Dr. Hu also helped found two start-up companies IC Ensemble and Verticom. Prior to SiRF, Dr. Hu worked at S3, a leading fabless PC graphic chipset and software provider, helping to grow the company into a market leader.

Dr. Hu earned his bachelor's degree in electrical engineering from National Taiwan University and his master's and doctorate degrees in computer science from the University of Illinois, Urbana. He also received an MBA from Santa Clara University.



Presentation time: Wednesday, October 17th 9:05am California Ballroom- Salon 6

Susan Graham Johnston

Vice President, Volume System Operations, Sun Microsystems, Inc.

"One Touch" Supply Chain

When discussing a company's prospects for growth or cost savings, supply chain efficiency is rarely first on the list. However, streamlining and increasing the efficiency of the supply chain, can improve customer response times, and better your business.

Like most global manufacturers, Sun needed to find a way to increase the efficiency and predictability of their supply chain in order to cut costs and satisfy customer demand for fast delivery of low-priced, high-quality products. This keynote presentation will examine Sun's "one touch" supply chain model, including considerations necessary to execute the model successfully.

Related ISSM Topics: Supply Chain Integration, Manufacturing Strategy and Operations Management, Process & Material Optimization

Biography

Sue Graham Johnston is Vice President, Volume System Operations at Sun Microsystems, Inc. The Volume Systems Operations team determines the sourcing and manufacturing strategies and manages operational performance for Sun's AMD, Intel and SPARC products. The Volume Systems portfolio encompasses entry to midrange servers, blades, and workstations. Her responsibilities also include Software Operations, Configurator Engineering, and Value Engineering. Johnston returned to Sun from E2open, Inc., a supply chain software company, where she held the position of Vice President of Account Operations, managing multinational deployments of B2B software integration. She began her Sun career in 1997 and has held various leadership positions in supplier management, value engineering, and quality. Prior to joining Sun, Johnston spent several years as a management consultant for Bain & Company. She holds an MBA, MS Eng in Manufacturing Systems, and BS in Mechanical Engineering and Product Design from Stanford University.

Rich Karlgaard

Publisher of Forbes

"Twelve Types of Innovation That Will Save Your Company"

Managers today must face a harsh truth: no company is immune from the pressures of commoditization and global price competition. Low-cost will always win if a product or service is not differentiated in its market. The challenge for companies located in high-cost countries is to create competitive advantage through innovation. Where and how, precisely, should companies innovate?

Related ISSM Topics: Manufacturing Strategy and Operations Management, Process & Material Optimization

Presentation time: Monday, October 15th, 8:10am California Ballroom- Salon 6

Biography

Rich Karlgaard is the publisher of *Forbes* - the world's most popular business and financial magazine, read by 4.5 million people per issue. He also is the author of the book, Life 2.0 How People Across America Are Transforming Their Lives by Finding the Where of Their Happiness, which was an Amazon and *Wall Street Journal* business best-seller.

In every issue of *Forbes*, Karlgaard writes a column called "Digital Rules". It appears in the front pages of *Forbes*, directly after columns by Steve Forbes. In his "Digital Rules" column, Karlgaard writes about technology, entrepreneurship, regional and economical development, and the future of business and work. He frequently lectures on these subjects and is a regular guest on the Fox News Channel's Forbes on Fox. In 2005, Karlgaard began writing a daily blog, which appears on the homepage of Forbes.com.

Karlgaard joined *Forbes* in 1992 to start *Forbes ASAP*, a technology magazine, along with Forbes CEO and editor-in-chief Steve Forbes, and the futurist and writer George Gilder. At *Forbes ASAP* Karlgaard commissioned original works by Tom Wolfe, John Updike and other notable American writers.

Karlgaard is an accomplished entrepreneur. He has co-founded two companies (Garage Technology Ventures, in 1997; and Upside Magazine in 1988) and one civic organization (the 5,500-member Churchill Club in 1985). For the latter, Karlgaard was a co-winner of the Ernst & Young Northern California "Entrepreneur of the Year" award.

Karlgaard was raised in Bismarck, North Dakota and graduated from Stanford University with a B.A. in Political Science. Currently, he lives with his wife and two children in Northern California. When he is not working or spending time with his family, Karlgaard likes to fly his single-engine airplane around the country and meet the people who make America unique and great.

Dr. Susumu Kohyama

President and CEO, Covalent Materials Corporation

"Rising Role of Indirect Materials for Semiconductor Manufacturing"

Presentation time: Monday, October 15th 9:05am California Ballroom-Salon 6

Smaller device geometry and larger wafer size have almost always resulted in effective cost reduction. However, further device miniaturization together with 300mm wafer process started to create various "Manufacturability" issues. In order to solve or ease such problems, role of indirect materials is increasing so rapidly, therefore collaborations among device manufacturers, semiconductor equipment manufacturers, and also materials and components suppliers become so critical and essential.

Among various indirect materials, inorganic materials or Ceramics in wider definition are demonstrating rapid and steady progress recently. In addition to traditional ceramics and their combinations, ceramics compound with rare-earth element also started to play a unique role, especially in extreme environment such with active plasma. Fundamental material characteristics, mechanical accuracy both body and surface, and all related physical and chemical interactions should be studied and optimized under much wider collaborations in the industry.

Related ISSM Topics: Manufacturing Strategy and Operations Management, Supply Chain Integration, Design for Manufacturing

Biography

Dr. Susumu Kohyama is president and CEO of Covalent Materials Corporation, formerly Toshiba Ceramics Co. Ltd. Covalent Materials is a leading edge parts and materials manufacturer serving primarily the semiconductor and LCD industries.

Dr. Kohyama joined Toshiba Research and Development in 1969 and has spent most of his career in the area of semiconductors. He has held various management positions, including executive vice president Semiconductor Group, chief technology officer Electronic Devices Group and chief strategy officer Toshiba Corporation. In June 2004, Dr. Kohyama left Toshiba Corporation to take on his current role as president and CEO of Toshiba Cermaics Co. Ltd. which recently went through a management buy-out and was renamed Covelent Materials corporation. Dr. Kohyama has B.S., M.S. and Doctorate degrees from the University of Tokyo. He is currently the Chairman of VLSI Symposia Executive Committee, representing Japan and Asia.

Michael Splinter

Chief Executive Officer, Applied Materials

"Optimizing Fab Performance"

An analysis and vision for the next generation of wafer fabs, highly efficient, lower energy and environmentally sound.

Related ISSM Topics: Manufacturing Strategy and Operations Management, Manufacturing Control and Execution, The Green Factory

Presentation time: Wednesday, October 17th, 8:10am California Ballroom-Salon 6

Biography

Mike Splinter is president and chief executive officer, as well as member of the Board of Directors of Applied Materials, the global leader in nanomanufacturing technology solutions for the electronics industry. He has focused the Company on expanding its leadership with a strong growth strategy by increasing market share and offering a breadth of products and service solutions.

Splinter, a 30-year veteran of the semiconductor industry, has led some of the largest semiconductor manufacturing operations in the world, during which time he has been at the forefront of many of the industry's most significant technology innovations and transitions.

Prior to joining Applied Materials, Splinter was an executive at Intel Corporation for nearly 20 years. Most recently, he was executive vice president and director of Sales and Marketing worldwide. He was responsible for the critical development of manufacturing technologies for major industry transitions, including the move to 300mm wafers and the shift to 130nm devices. An engineer and technologist, Splinter began his career at Rockwell International in the firm's Electronics Research Center. During his tenure, he became manager of Rockwell International's Semiconductor Fabrication Operations and was awarded two patents.

As a key member of the Technology CEO Council, an elite group of nine top high-tech CEOs, Splinter is helping drive new U.S. federal public policy. He serves on the board of Semiconductor Equipment and Materials International (SEMI), a global association representing the collective interests of the equipment and materials industry. He also is Chair of the board of directors for the Silicon Valley Leadership Group, an organization of CEOs focused on housing, transportation, environment and other quality of life issues affecting their employees.

Internationally, Splinter is a member of the Governors' Council of the World Economic Forum, which consists of the most influential and forward-thinking business, government, media and intellectual leaders. For more than 30 years, the council has been at the heart of the global business community, working to sustain economic and social prosperity worldwide. Author of numerous papers and articles, Splinter earned both bachelor of science and master of science degrees in electrical engineering from the University of Wisconsin, Madison.

Presentation time: Monday, October 15th 1:00pm California Ballroom-Salon 6

Paul Westbrook

Senior Technologist, Texas Instruments – International Facilities

"Less is More"

We have been conditioned to think that more is always the answer – in power, speed, time, and of course money. It's been said before, but it's often true - "Less is More." From an energy perspective it's almost always cheaper to save energy than it is to produce more – and that doesn't even count the often ignored cascading effects from additional production. Optimizing systems and running at the highest efficiency wrings the most from every dollar spent on resources – from raw materials to energy and water. It's not as sexy as solar panels on the roof or wind turbines on the lawn, but it works. It not only works well, but it continues to pay dividends year after year.

Waste is the largest growth industry in the US – and probably the world. The companies that recognize this and best optimize their operations will gain an advantage over their competition. Get two uses out of a drop of water where your competition only gets one. That business advantage will continue to grow as resources become scarce and the prices increase accordingly. And sustainability doesn't have to cost more. If optimization is a design goal from the start of a new project then it often can reduce initial cost too.

Related ISSM Topics: Process & Material Optimization, The Green Factory

Biography

Paul Westbrook is the Sustainable Development Manager for Texas Instruments. He has worked for TI since graduating from LSU with a BSME in 1982. Westbrook's roles at TI have ranged from facilities design engineer to facilities manager. In 2002, he moved to TI's International Facilities organization and began working on sustainable development ideas and plans. He headed the sustainable effort for TI's new 300mm semiconductor manufacturing plant in Richardson, TX. He is a LEED Accredited Professional and a Senior Member of the Technical Staff at TI. Westbrook designed his own passive/ active solar home which won the 1996 NAHB Energy Value Housing Award for Innovative Design.

Financial Panel Discussion

"Going Private… Or Remaining Public?"

Wednesday
October 17, 2007
1:00pm
California Ballroom- Salon 6

ISSM 2007 presents an executive-level panel discussion focused on the increasing need for the semiconductor industry to look outward for new perspectives both in manufacturing and in the financial world. The panelists, which include managing directors of global technology investment banking from Morgan Stanley, Blackstone, Bear Stearns, and Francisco Partners, have each been chosen due to their unique experience on this topic.
This panel will discuss the benefits, risks and management challenges in taking a high tech company 'private' or in keeping it 'public' - especially in a technology intensive, cyclical industry like semiconductor and semiconductor equipment.

Moderators

Mihir Parikh is the founder, President & CEO of Aquest Systems Corporation, a privately held semiconductor automation company with strategic technology partnerships and operations in the U.S., Japan, Taiwan and India. In 1984, Dr. Parikh also founded Asyst Technologies, Inc. and served as CEO for 18 years, until 2002. Under his leadership, Asyst became a $500M global public company with its products becoming a standard for all IC manufacturing. From 1974 to 1984, Dr. Parikh held various engineering management positions with IBM and Hewlett-Packard. Dr. Parikh graduated from the University of California at Berkeley with a B.S. degree in engineering physics in 1969 and with a Ph.D. in engineering science in 1974. Dr. Parikh is the recipient of the Silicon Valley Engineering Hall of Fame Award and the SEMI Award for his contributions to the IC industry.

Frank Quattrone has dedicated his 23-year business career to advising technology companies on financings, mergers & acquisitions. Mr. Quattrone worked for 17 years with Morgan Stanley, where he was an early member of the firm's Technology Group, helping to build it from a virtual start-up in 1982 to the firm's largest industry group in 1995. He headed Morgan Stanley's West Coast Technology Group from 1986-1990, and its Global Technology Group from 1991-1996. In 1996 Mr. Quattrone co-founded DMG Technology Group, a technology-focused investment banking business for Deutsche Bank. As CEO, Mr. Quattrone led DMG Technology Group from a startup to a $200M business in two years. Mr. Quattrone has advised on the IPOs of Amazon.com, Ascend Communications, Cisco, Intuit, Linear Technology, Netscape, ST Microelectronics, Synopsys and Xilinx. He has also advised on other financing and M&A assignments for Adobe, Agilent, AOL, Apple, Applied Materials, Cypress Semiconductor, Hewlett-Packard, IBM, Intel, KLA-Tencor, National Semiconductor, Oracle, VeriSign and Veritas.
Mr. Quattrone serves as Chairman of the Board of The Tech Museum of Innovation (an interactive science/technology educational center) and as a Trustee of Castilleja School. He also serves on the Advisory Boards of The Northern California Innocence Project (a free legal clinic at Santa Clara Law School that works to exonerate wrongfully convicted prisoners by proving their innocence) and the John Burton Foundation for Children Without Homes.
Mr. Quattrone graduated summa cum laude from The Wharton School of the University of Pennsylvania with a Bachelor of Science in Economics degree in 1977, and was an Arjay Miller Scholar at Stanford University Graduate School of Business, where he received his Masters in Business Administration degree in 1981.

Panelists

Michael Grimes is Morgan Stanley's Head of Global Technology Investment Banking. Mr. Grimes has been in the technology investment banking business for 20 years and joined Morgan Stanley in 1995.

Mr. Grimes has been responsible for hundreds of technology transactions aggregating over $100 billion in value, including initial public offerings, mergers & acquisitions, and other debt and equity financings. He has been involved with many of the largest and highest profile technology transactions in history, including AMD's $5.4 billion acquisition of ATI, HP's $13.6 billion spin-off of Agilent Technologies, Google's $1.9 billion IPO and $4.4 billion follow-on offering, Skype's $2.6 billion acquisition by eBay, Oracle's $5.8 billion acquisition of Siebel, VeriSign's $21 billion merger with Network Solutions, and Seagate's $20.5 billion transaction with Veritas Software and Silver Lake Partners. Mr. Grimes has been recognized by Forbes as the top ranked technology investment banker in 2004, 2005, 2006, and 2007. Mr. Grimes holds a BS degree in Electrical Engineering and Computer Science from the University of California at Berkeley.

Dipanjan "DJ" Deb is a Managing Partner of Francisco Partners. Prior to founding Francisco Partners in 1999, Mr. Deb was a principal with Texas Pacific Group. Earlier in his career, Mr. Deb was director of semiconductor banking at Robertson Stephens & Company and a management consultant at McKinsey & Company. Mr. Deb serves on the board of directors of AMI (AMIS), CBA Group, MagnaChip, Metrologic Instruments, Inc., SMART Modular (SMOD) and was previously on the board of Conexant (CNXT), Globespan, Legerity, NPTest/Credence (CMOS), ON Semiconductor (ONNN), Ultra Clean Technology (UCTT). Mr. Deb holds a BS degree in Electrical Engineering and Computer Science from U.C. Berkeley, and an MBA degree from the Stanford Graduate School of Business.

Paul C. Schorr IV ("Chip") is a Senior Managing Director in the Private Equity group, where he principally concentrates on investments in technology. Before joining Blackstone in 2005, Mr. Schorr was a Managing Partner of Citigroup Venture Capital in New York where he was responsible for the firm's technology/ telecommunications practice. Mr. Schorr was instrumental in such transactions as Fairchild Semiconductor, ChipPAC, Intersil, AMI Semiconductor, Worldspan, NTelos and MagnaChip. He had been with Citigroup Venture Capital for nine years. Mr. Schorr received his MBA with honors from Harvard Business School and a BSFS magna cum laude from Georgetown University's School of Foreign Service. He is Chairman of the Board of Directors of Travelport Inc., and a member of the board of directors of Freescale Semiconductor, AMI Semiconductor, and MagnaChip.

Rex Sherry is Senior Managing Director, Head of West Coast Technology Investment Banking at Bear Stearns. Mr. Sherry joined Bear Stearns in 2006 from Merrill Lynch, where he was Vice Chairman Technology Investment Banking. Mr. Sherry began his career at Montgomery Securities and was with the firm from 1987-2000, his most recent position was Managing Director, Technology Investment Banking. He has completed over 80 initial public offerings, 200 additional equity and debt financings as well as over $20 billion of mergers and acquisitions for technology companies. Mr. Sherry graduated with a BA degree in Business Economics and Finance from the University of Washington.

ISSM 2007
Marriott Hotel ~Santa Clara, CA U.S.A.
October 15-17, 2007

Monday, October 15, 2007

General Conference Activities

7:00 AM	Registration Desk Open for Check-in	California Ballroom Registration Desk
7:00 AM	Speaker Ready Room available for speaker review and preparation	
7:00 AM	Speaker Breakfast (for speakers/ co-chairs scheduled on Monday)	Hall of Cities- Seattle
12:00 PM	Attendee Lunch	Hall of Cities
6:15 PM	Attendee Dinner Reception	Pool and Courtyard

Keynote Speeches and Addresses — California Ballroom, Salon 6

8:00 AM — Tom Sonderman, International Program Committee Chairman
Welcome Note

8:10 AM — Rich Karlgaard, Publisher of Forbes
Twelve Types of Innovation That Will Save Your Company

9:05 AM — Susuma Kohyama, President and CEO, Covalent Materials Corp.
Rising Role of Indirect Materials for Semiconductor Manufacturing *77*

1:00 PM — Paul Westbrook, Senior Technologist, Texas Instruments
Less is More *79*

Monday, Track 1 Oral Presentations — California Ballroom, Salon 6

10:15 AM	**MS-O-243**	**300mm Prime Gaps That Need to be Addressed to Boost Productivity** ..... **267** Les Marshall, AMD
10:35 AM	**MS-O-139**	**Evolutionary Business Models and Inter-Firm Engineering Processes Between the Foundry and Fabless in the Semiconductor Industry** ..... **275** Ruey-Shan Guo, National Taiwan University
10:55 AM	**MS-O-049**	**Managing Sunset & Closure of a Semiconductor Technology parallel to aggressive new process Ramp** ..... **271** Sylvain Bouhnik, Intel
11:15 AM	**MS-O-083**	**Method of Overall Consumables Effectiveness** ..... **279** Kenji Kikuchi, Spansion
11: 35 AM	**MS-O-071**	**Economic Analysis of 450mm Wafer Migration** ..... **283** Tzu-Ching, Alan Chang, TSMC
2:00 PM	**MS-P-126**	**Real Option Analysis for Capacity Investment Planning for Semiconductor Manufacturing** ..... **305** Chih-Chiang Chen, TSMC
2:04 PM	**MS-P-226**	**Characterizing the Operating Curve - How Can Semiconductor Fabs Grade Themselves?** ..... **289** Asser Fayed, Cypress Semiconductor

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Monday, Track 2 Oral Presentations — California Ballroom, Salon 4

2:44 PM	**PC-P-101**	**Process Start/End Event Detection and Dynamic Time Warping Algorithms for Run-by-Run Process Fault Detection**.....**413** Ja Young Choi, Yonsei University
2:55 PM	**PC-O-218**	**Automated Statistical Process Matching Across the Virtual Fab** .....**338** Girish S. Nirgude and Diaa Eldin Nassar, Intel
3:15 PM	**PC-O-159**	**Qualification of Immersion Double Patterning**.....**342** Amir Widmann, KLA-Tencor
3:45 PM	**PC-O-186**	**Virtual Metrology for Plasma Particle in Plasma Etching Equipment**.....**346** Shin-ichi Imai, Matsushita Electric (Panasonic)
4:05 PM	**PC-O-045**	**Comprehensive interconnect etch tool qualification methodology for high volume mixed technology node production**.....**350** Peter Frankwicz, National Semiconductor
4:25 PM	**PC-O-090**	**Development of an Automatic CD Control system for Cu damascene etching** .....**354** Hidetaka Nambu, NEC Electronics
4:45 PM	**PC-O-098**	**Application of Cathodoluminescence to SiGe Epitaxial Process Control** .....**358** Tatsuhiko Koide, SANYO Electronics
5:05 PM	**PC-O-233**	**On The Use of Wafer Positional and Spatial Pattern Analysis To Identify Process Marginality and to De-Convolute Counterintuitive Experimental Results**.....**362** Greg Klein, Spansion

Tuesday, October 16, 2007

General Conference Activities

7:00 AM	Registration Desk Open for Check-in	California Ballroom Registration Desk
7:00 AM	Speaker Ready Room available for speaker review and preparation	
7:00 AM	Speaker Breakfast (for speakers/ co-chairs scheduled on Tuesday)	Hall of Cities- Seattle
12:05 PM	Attendee Lunch	Hall of Cities
5:15 PM	Interactive Poster Session Reception	Grand Ballroom

Keynote Speeches and Addresses — California Ballroom, Salon 6

8:00 AM	Tom Sonderman, International Program Committee Chairman ***Welcome Note***
8:15 AM	Mark Durcan, COO, Micron ***Optimizing Memory Operations at the Leading Edge***
9:10 AM	Jackson Hu, CEO, UMC ***Challenges and Opportunities Facing the Semiconductor Industry***.....***27***
12:50 PM	Nick Bright, Executive Vice President Products, LAM Research ***Technology and the Equipment Industry***

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Marriott Hotel ~Santa Clara, CA U.S.A.
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Tuesday, Track 1 Oral Presentations — California Ballroom, Salon 6

Tuesday, Track 2 Oral Presentations — California Ballroom, Salon 4

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3:50 PM	**ES-O-010**	**Update of The EPSON Method for PFC Measurement using FT-IR.....160** Isamu Namose, Seiko Epson
4:10 PM	**ES-O-216**	**Manufacturing Constraints - Reducing Volatile Organic Compound Emissions .....151** Scott Stewart, Intel
4:30 PM	**ES-O-130**	**Estimate on CO2 Emissions Reduction Effect Achieved by the Adoption of a Water Spray Humidification System to Clean Rooms .....164** Satoshi Uemura, Tohoku University

Wednesday, October 17, 2007

General Conference Activities

7:00 AM	Registration Desk Open for Check-in California Ballroom Registration Desk
7:00 AM	Speaker Ready Room available for speaker review and preparation
7:00 AM	Speaker Breakfast (for speakers/ co-chairs scheduled on Wednesday) Hall of Cities- Seattle
7:00 AM	Attendee Breakfast Hall of Cities

Keynote Speeches and Addresses California Ballroom, Salon 6

8:00 AM	Tom Sonderman, International Program Committee Chairman ***Welcome Note***
8:10 AM	Michael Splinter, CEO, Applied Materials ***Optimizing Fab Performance***
9:05 AM	Susan Graham Johnston, Vice President, Volume System Operations, Sun Microsystems ***"One Touch" Supply Chain.....53***
1:00 PM	Financial Panel Discussion ***"Going Private… Or Remaining Public?"***
3:05 PM	Tom Sonderman, International Program Committee Chairman ***Final Note***

Wednesday, Track 1 Oral Presentations California Ballroom, Salon 6

10:15 AM	**YE-O-157**	**Dynamic Defect-Limited Yield Prediction by Criticality Factor .....551** Vicky Svidenko, Applied Materials
10:35 AM	**YE-O-030**	**Enhancement of Voltage Contrast Inspection Signal Using Scan Direction.....555** Oliver D. Patterson, IBM

Wednesday, Track 2 Oral Presentations California Ballroom, Salon 4

Keynote

Challenges and Opportunities Facing the Semiconductor Industry

Dr. Jackson Hu
Chairman and Chief Executive Officer,
United Microelectronics Corporation

9:10am
Tuesday, October 16, 2007

California Ballroom, Salon 6

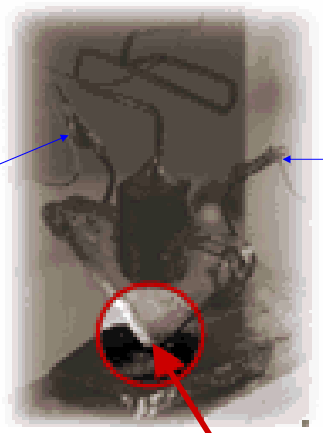
Challenges and Opportunities Facing the Semiconductor Industry

ISSM 2007

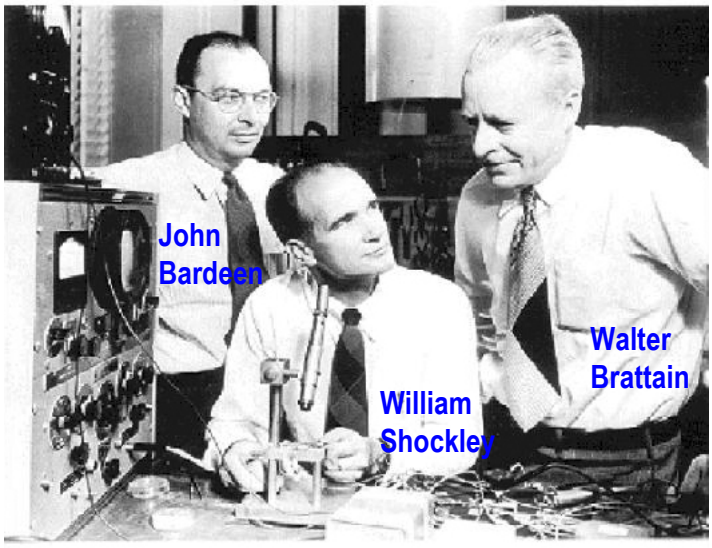
Jackson Hu
Chairman & CEO
UMC

Impact of Moore's Law Evolution

The First Transistor – Christmas Eve, 1947



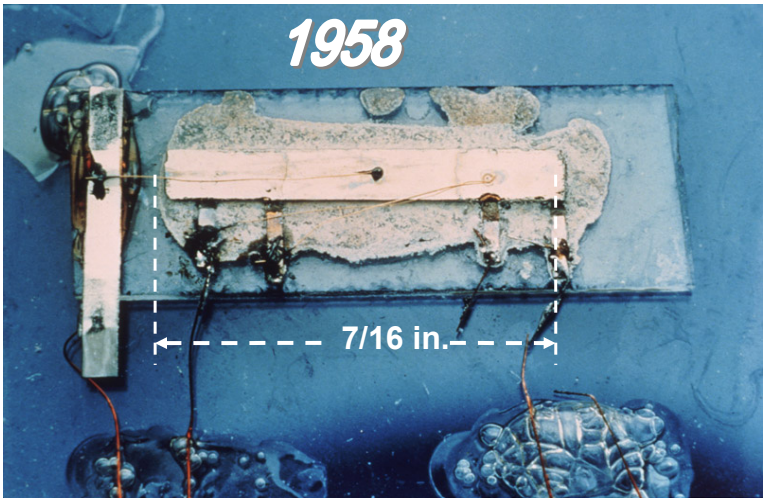
Source: AT&T Bell Labs



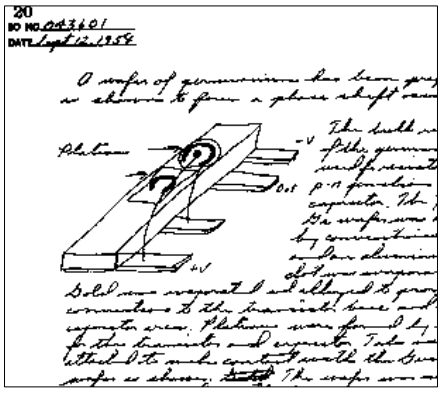
1956 Nobel Prize Winners

Source: AT&T Bell Labs

The First IC



Source:Texas Instruments

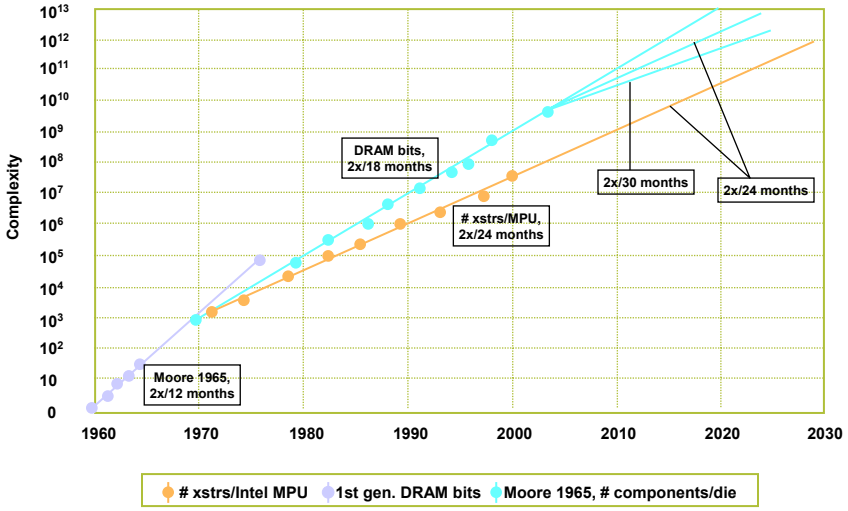


September 12,1958

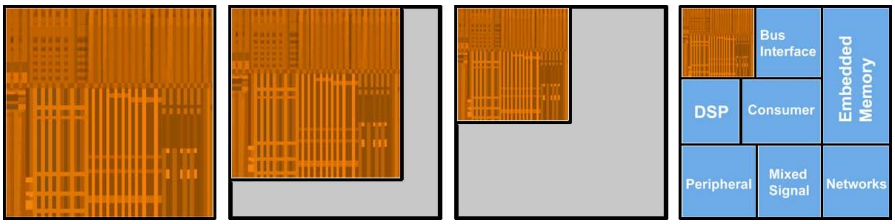
Jack Kilby
Nobel Prize Winner, 2000

Source:Texas Instruments

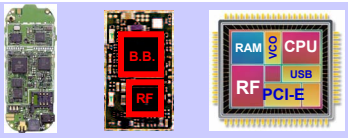
Moore's Law



Shrinking Geometry Allows Higher & Higher Levels of Integration

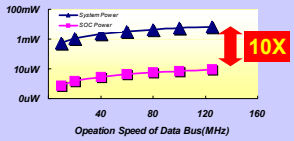


Benefits Enabled by SoC Integration



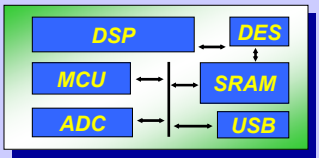
Cost Reduction

- Less Packaging
- Less Assembly



Power Saving

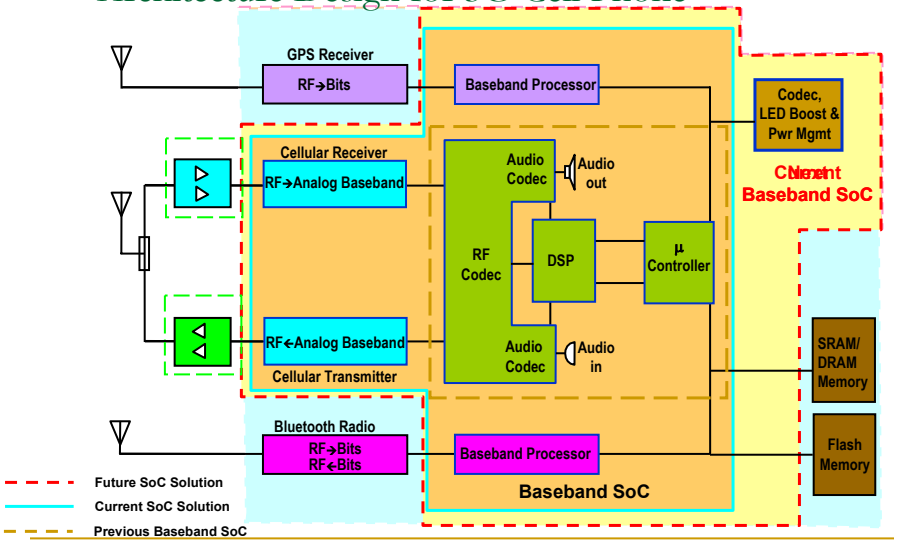
- Operating Conditions on System Bus
  - Swing: 3.3V vs 1.0V
  - Loads: 5pF vs 5fF



Performance Increase

- Data Throughput
  - System DDR400: 200MHz
  - Intra-SoC: 500MHz in 90nm

Analog, Digital, and RF in SoC
- Architecture Design for 3G Cell Phone



Functions Offered by a 3G Phone

3D Graphics

FM, MP3, DAB

GPS, EOTD

MPEG4, JPEG

Speech to Text, Voice Recognition

GSM-GPRS-EDGE-WCDMA/CDMA2000 /STD-SCDMA (RISC, DSP, Protocol Stack, System BIST)

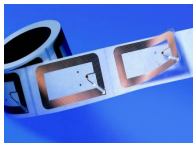
WiFi, Bluetooth

Communications

Cell Phone

Bluetooth

Wi-Fi



RF ID

ADSL

Cable Modem

VoIP

Ethernet

Consumer

DTV/STB

LCD TV

DVD Player

DVD Recorder

Digital Camera

Digicam

Game Console

MP3

Computing

PC

Notebook

Graphics Card

Opt. Disk Drive

Hard Disk Drive

Card Reader

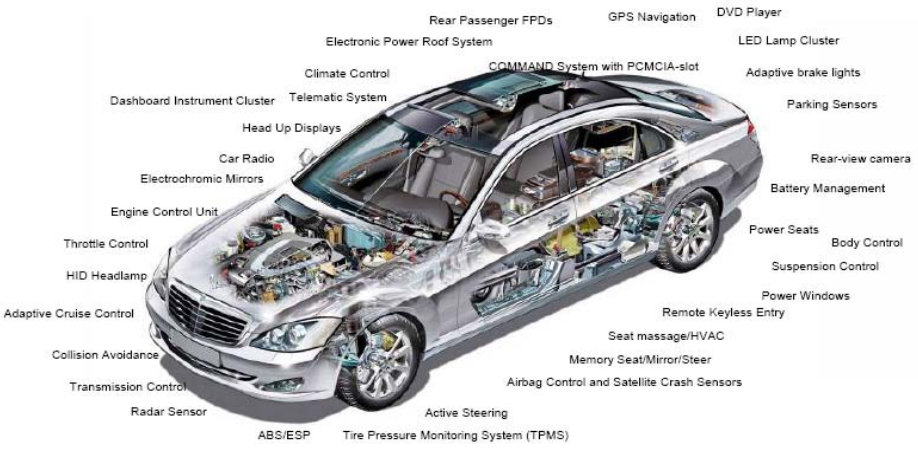
Server

Printer

DRAM Module

USB storage

Automotive Semiconductor



Myth of Moore's Law

For many years, all the players along the semiconductor value chain followed Moore's Law loyally. If they hadn't, they would have been perceived as falling behind the competition.

However, ….

Myth of Moore's Law

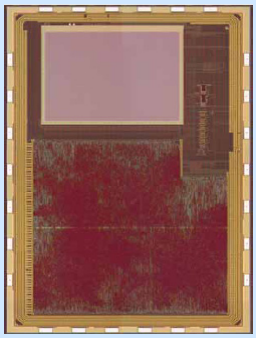
Does advanced technology always equal innovation?

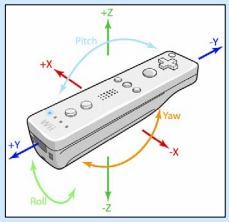
Wii outsells PS3

PS3 has excellent graphics quality!

Source: PS3 HD game "GT HD"

PixArt Multi Object Tracking (MOT) sensor





Are today's SOC designs taking full advantage of advanced technologies?

- In many cases, the answer is no!
- Many designs use advanced technologies for cost reduction at the chip level, but not necessarily at the system level.
  - Architecture partition is not optimal
  - Integration level is not optimal

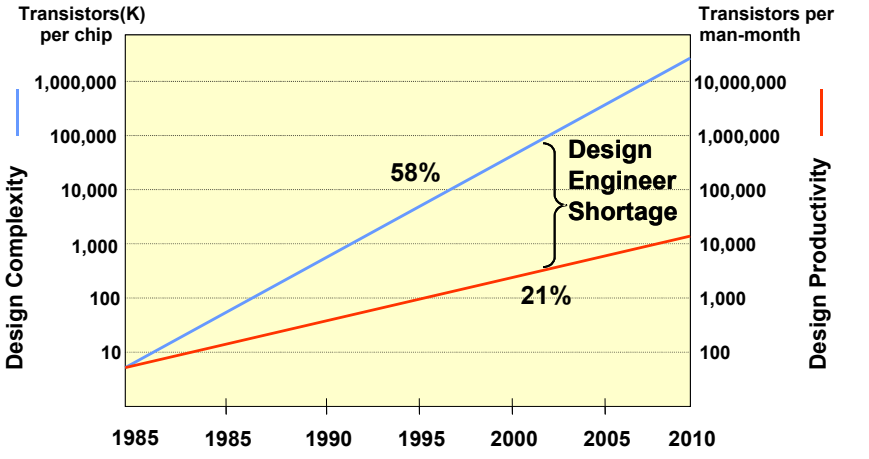
What's wrong if the next node takes longer?

- Theoretically, nothing is wrong. The technology could be more optimal for certain applications., e.g., high K/metal gate for graphics at 45nm
- Can suppliers and customers afford to wait?

Finally, Designers Are Skipping Nodes

- Designers are now skipping technology nodes due to the tremendous efforts needed for IP preparation, design verification and product qualification

Design Complexity vs. Engineering Resource Required



Source: ITRS & SRC

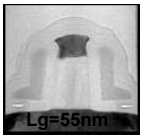
Off-shoring, Outsourcing & Global Design Centers – The World is Flat!

- It is common practice for design companies to establish global design centers to take advantage of the strengths in different geographical areas:
  - US (Silicon Valley, S. California, Texas) for product definition, advanced analog, and mixed-signal/RF designs.
  - China, Taiwan and India for IP, IC & software implementation and customer support.

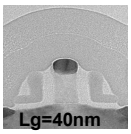
Management of global design centers is challenging, but doable!

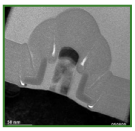
Continued Evolution of Moore's Law

CMOS Scaling Technologies

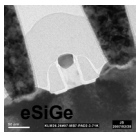


Copper/ Low-K Retrograde Twin-Well

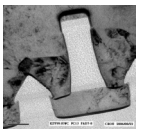


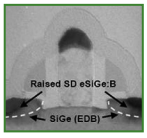


NiSi Mobility Enhancement

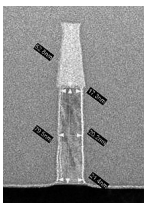


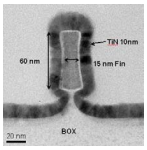
Strain/eSiGe U-Low-K Immersion Litho





High K/ Metal gate





Hi-K/Metal gate MuGFET

Challenges and Potential Solutions for 65nm and Beyond

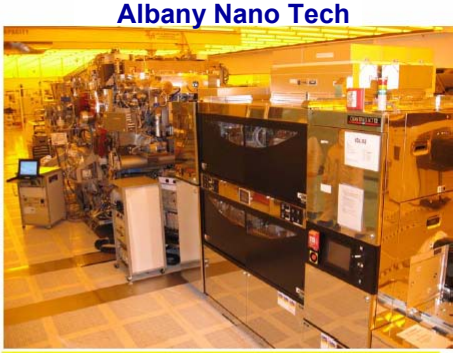
Technology Driving Force	Challenges	Process Solutions	Design Solutions
Density and Manufacturing	▪ Sub-λ Litho.	▪ Immersion Litho. ▪ High NA ▪ RET ▪ Double Patterning ▪ EUV	▪ DFM ▪ Pre/Post-tapeout ▪ SSTA, LOD, WPE (FEoL) ▪ WEE, Double Via, CMP (BEoL)
Performance	▪ Conventional FEoL scaling reaching limit (Lg, tox) ▪ BEoL scaling – inter-connect RC hitting a wall	▪ Mobility Enhancement (Strained Si, New Channel Material, Substrate Engr.) ▪ Ultra Low-k (k<2.5) ▪ Air Gap ▪ Multiple-gate FET	▪ 3D-IC a multi-disciplinary technology ▪ Optical interconnect too far away
Power	▪ Ioff and Igate growing (Band-to-Band Tunneling)	▪ High-k and metal gate ▪ Device Engineering	▪ Power Gating, Multi-Vth, Clock Gating

Two EUV Alpha Demo Tools

IMEC

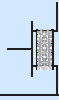
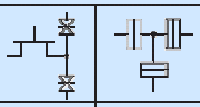
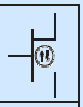
- λ 13.5 nm
- NA 0.25
- Field 26 x 33 mm^2
- Magnification 4x reduction
- Sigma 0.5
- Chief ray angle at mask is 6 degrees

Albany Nano Tech

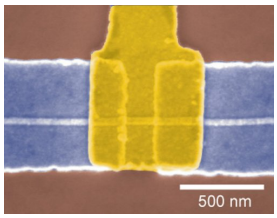


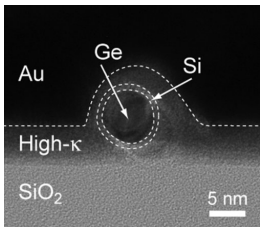
- Single stage, 300mm wafer, linked to track
- ATHENA alignment sensor
- Manual reticle load (no library)
- X REMA only; UNICOM
- Uses TWINSCAN technology (eg focus)
- Reflective optics

Emerging Research Logic Devices: 2007 ITRS

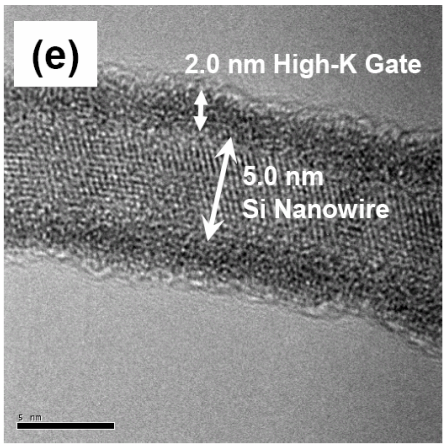
Device							
	FET [8]	1D structures	Resonant Tunneling Devices	SET	Molecular	Ferromagnetic logic	Spin transistor
Types	Si CMOS	CNT FET NW FET NW hetero-junctions Crossbar nanostructures	RTD-FET RTT	SET	Crossbar latch Molecular transistor Molecular QCA	Moving domain wall M. QCA	Spin transistor
Supported Architectures	Conventional	Conventional and Cross-bar	Conventional and CNN	CNN	Cross-Bar and QCA	CNN Reconfigure logic and QCA	Conventional

Nanowire FET as Leading Candidate for sub 22nm Technology



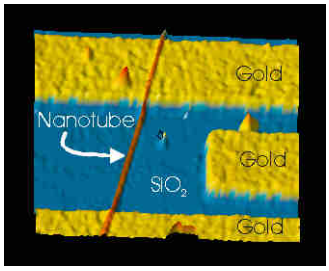


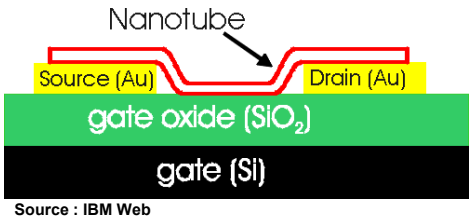
Source: Harvard Univ. 2006



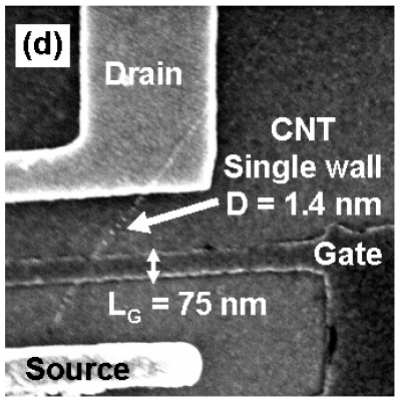
Source: Intel 2005

Carbon NanoTube (CNT) FET Technology



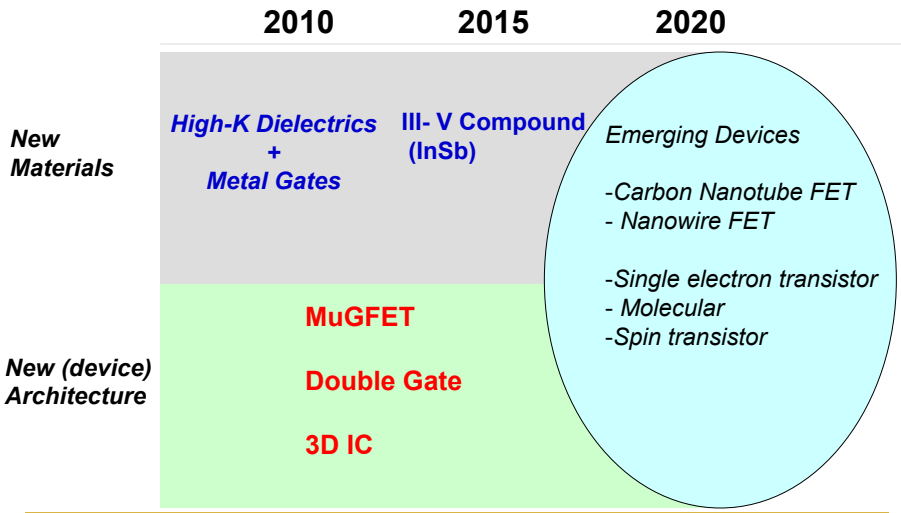


Source : IBM Web



Source: Intel 2005

Materials and Architecture Innovations Needed for beyond CMOS



Corollary of Moore's Law

Silicon Consumption Growth = $(1+CAGR)^{\text{transition time}}$ / Gross-die Gain

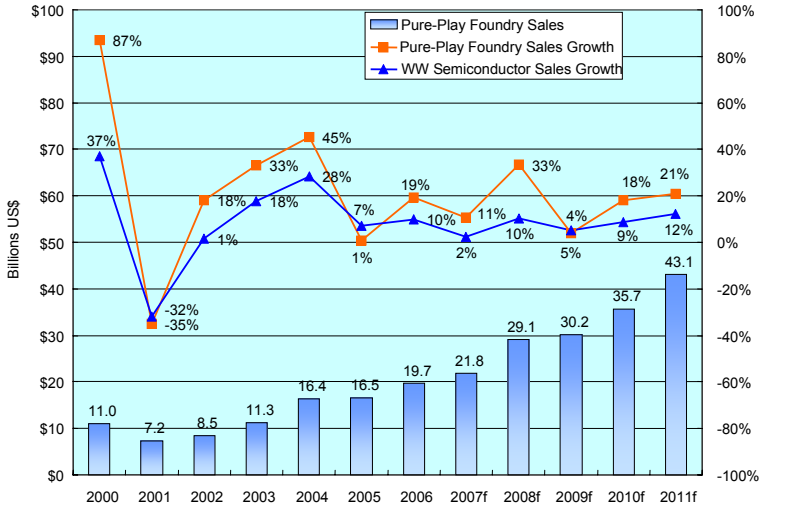
- **CAGR = Compound Annual Growth Rate for each application, customer or product.**
- **Transition Time = Time to transit into next technology node. This number is 2 if customers follow Moore's Law.**

Foundry's Position and Roles

More IDMs Have Moved To Fab-lite

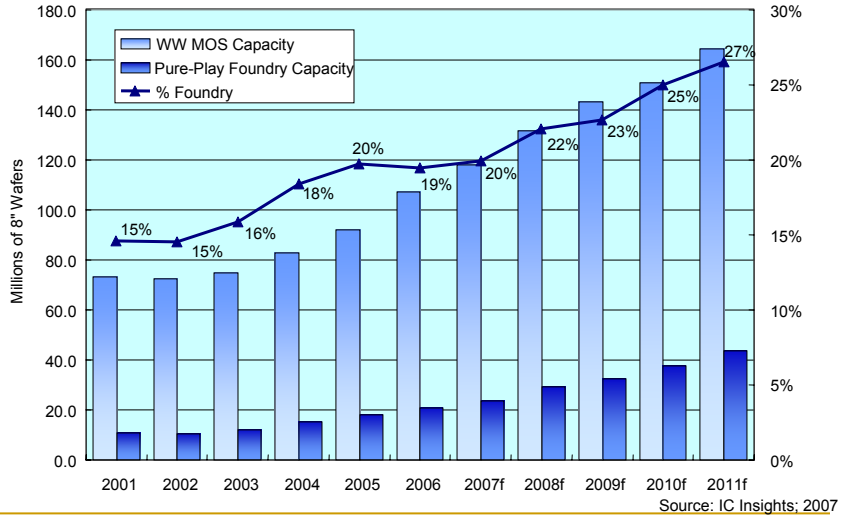
Source: UMC 2007

Foundry Sales - Maintain Higher Growth



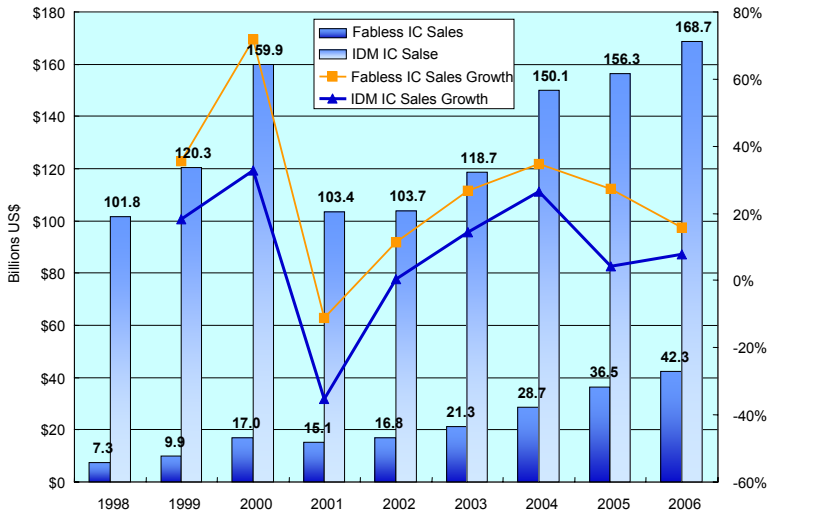
Source: IC Insights, Gartner; 5/2007

Foundry Plays Major Role in Manufacturing



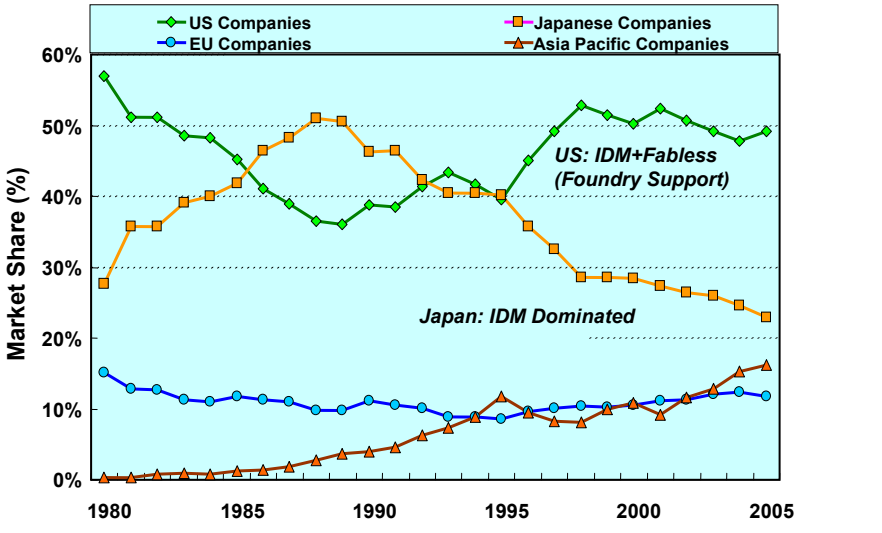
Source: IC Insights; 2007

Higher Fabless Growth



Source: IC Insights; 2007

Worldwide IC Market by Region



Source: Gartner Dataquest (April 2006) GJ06236

Worldwide Fabless Revenue (USD)

Rank	Company	2005	2006
1	Qualcomm	3,457	4,331
2	Broadcom	2,671	3,668
3	Sandisk	2,306	3,258
4	NVIDIA	2,376	3,069
5	Marvell	1,670	2,238
6	LSI Logic	1,919	1,982
7	Xilinx	1,645	1,872
8	ATI	1,810	1,750
9	MediaTek	1,430	1,629
10	Altera	1,124	1,286

In millions

Taiwan Fabless Revenue (USD)

Rank	Company	2005	2006
1	聯發 MediaTek	1,411	1,629
2	聯詠 NovaTek	789	967
3	奇景 Himax	540	758
4	威盛 VIA	581	660
5	凌陽 Sunplus	570	525
6	群聯 Phison	191	383
7	瑞昱 Realtek	323	382
8	鈺創 Etron	204	322
9	矽統 SiS	350	243
10	晨星 Mstar	170	223

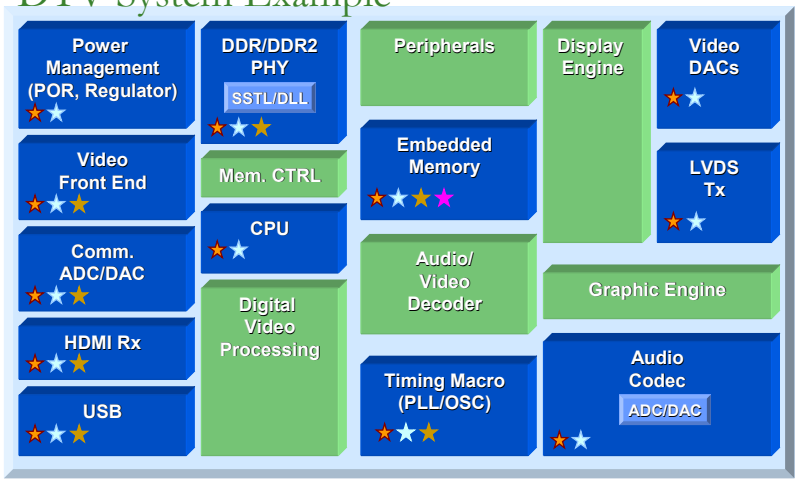
In millions

Global Fabless Market

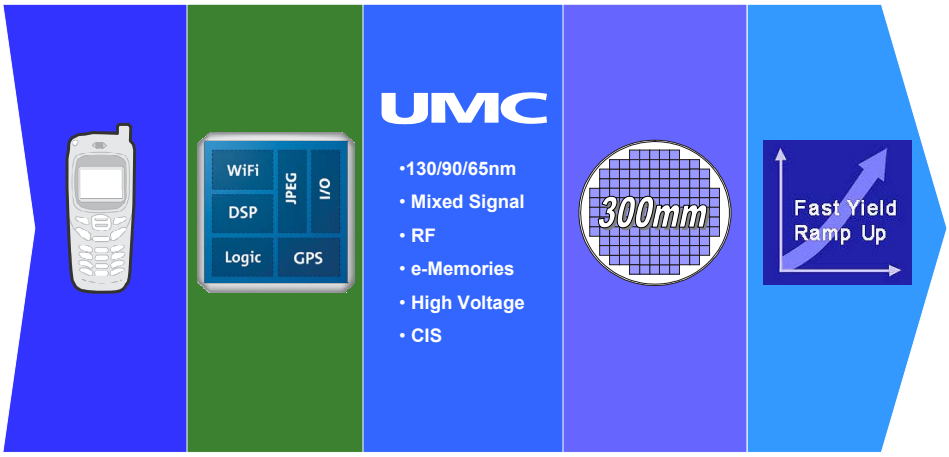
Region	2006			2005	
	Market Share	Revenue (MUS$)	yoy%	Market Share	Revenue (M US$)
North America	73%	$32,613	21%	72%	$26,958
Taiwan	18%	$8,260	16%	19%	$7,097
China	2%	$784	3%	2%	$764
Europe	4%	$1,572	17%	4%	$1,342
Korea	2%	$749	10%	2%	$681
Japan	1%	$554	24%	1%	$445
India	0%	$5	215%	0%	$2

Source: FSA; 2007

SOC design requires many IP
- DTV System Example



Foundry's Solutions for SoC Designs



System Architecture Knowledge | IP and Design Methodology | SoC Process Platform | World Class Manufacturing | Fast Yield Ramp/ Package Solution

L65SP/LL SoC Status

➢ Silicon Based DSM	❑ AC/DC Silicon-to-Model Delta <6% validated	✓	✓
➢ Qualification	❑ Process qual done ❑ Product qual done 8Mb SRAM & 5 products	✓	✓
➢ Yield Ramp	❑ 8Mb SRAM Natural Yield >90%	✓	✓
➢ Fundamental IP	❑ Standard Cell & I/O Lib. ❑ Memory Compiler	✓	✓
➢ DFM Tools	❑ CMP ❑ LSC ❑ SSTA ❑ CAA	✓	✓
➢ Low Power Solution	❑ Fundamental Lib. (cells, level shifter)	✓	✓

Summary

- New materials are needed for Moore's Law to continue. Applications that can benefit from higher density/speed, e.g., graphics, will embrace the most advanced nodes as soon as they become available.
- Other applications may skip nodes due to the increasing amount of time needed for IP preparation, design verification, process/product qualifications and software development.
- Under Moore's Law, wafer demand growth is highly dependent on the complexity of future SOC designs.
- The foundry industry is in a good position to grow due to the business released by IDMs.
- Foundry needs to carry more responsibilities in offering SOC design solutions.

Thank You!
Q & A

Keynote

"One Touch" Supply Chain

Susan Graham Johnston
Vice President, Volume System Operations,
Sun Microsystems, Inc.

9:05am
Wednesday, October 17, 2007

California Ballroom, Salon 6

ISSM 2007

Sun's "One Touch" Supply Chain

Sue Graham Johnston
VP, Volume Systems
Sun Microsystems, Inc.

Sun's Mission

To Solve Complex
Network Computing Problems
Through Innovation

The Global Power of Sun

Fortune
187
Company

Java Devices
5.5+ Billion

Java Developers
6+ Million

Worldwide Employees
34,219

Annual R&D
$1+ Billion

Annual Revenues
$13.8 Billion
Up 6.2% Y/Y

Cash
$5.94 Billion

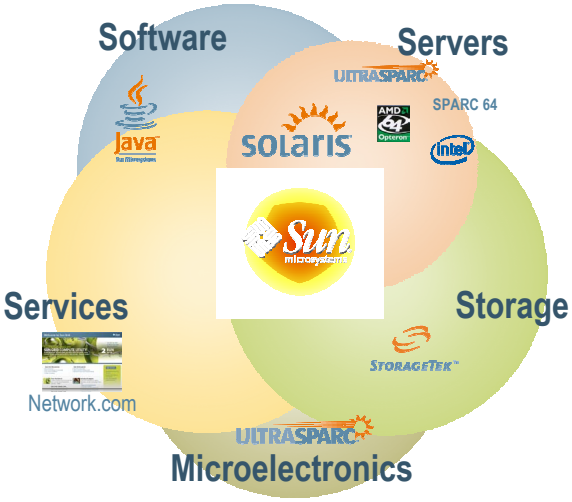
Patents
11,000+

Solaris 10
Licenses
8.9+ Million

Annual Storage
Petabytes Shipped
410

Business Presence
100 Countries

Innovation, Choice, Greater Value



Sun Worldwide Operations

GLOBAL CUSTOMERS, GLOBAL SUPPLY BASE

- Global Manufacturing Footprint
  - > 2 Sun Configuration Centers
  - > Extended reach through External Manufacturers and Third-party Logistics Providers (3PLs)

Supply Chain Conflicting Requirements

Business Metrics

- Less inventory
- Lower cost
  - Material
  - Supply chain overhead

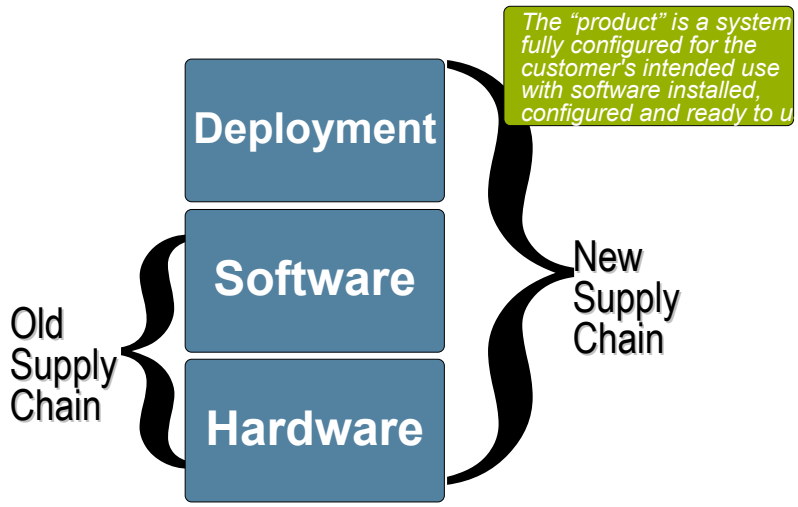
Customer Desire

- Shorter leadtimes
- More functionality
- More convenience
- Faster deployment
- Better Quality

Supply Chain Customer Requirements

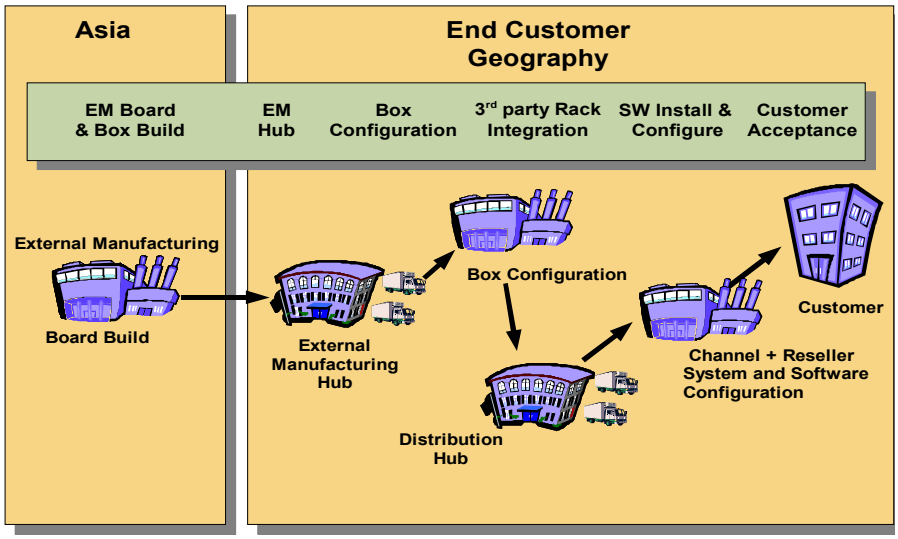
The Supply Chain is...

What Customers Buy

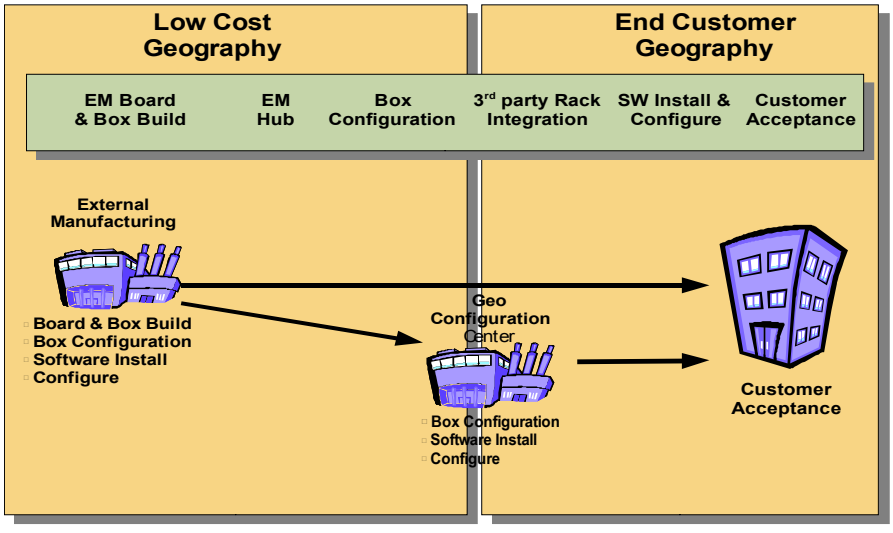


"One Touch" Supply Chain

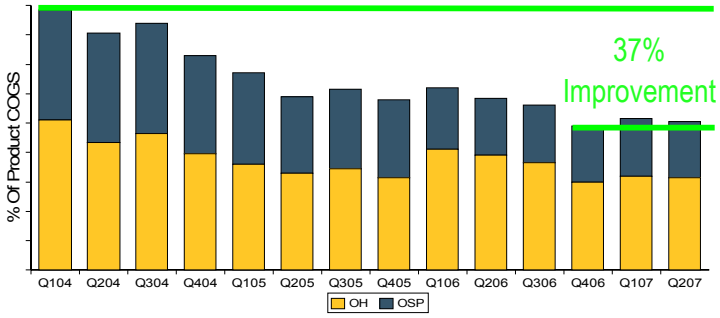
Server Supply Chain (old)



Server Supply Chain (new)



Total Overhead as % of Product COGS

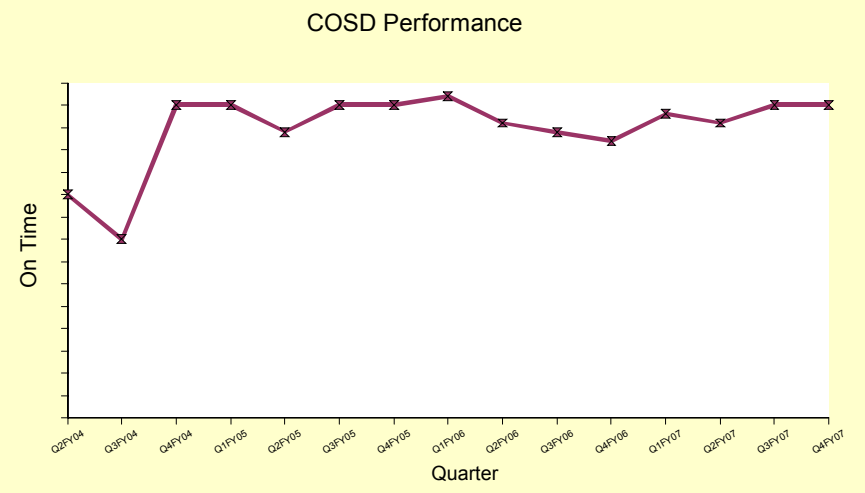


Key Points

- Total overhead reduced by outsourcing and efficiency improvements
- Did NOT just push same costs upstream
- Net result is Leaner, more efficient Supply Chain

Shipment Metric Performance

- COSD (Customer Original Ship Date) Predictability



Sun's "One Touch" Supply Chain - Results

We now ship more than 50% of orders directly to customers from suppliers

Logistics costs have been reduced by 20%

Finished goods inventory has been reduced by as much as 40%

37% reduction in over all supply chain costs

Supply Chain Foundations

Competitive Landscape

- Our competition is 10X our size
  - Economies of Scale
  - Volume Cost Advantage
  - Size Does Matter!

- Use the Supply Chain to give Customers a reason to buy from us!
- Apply Lean concepts to the entire Supply Chain

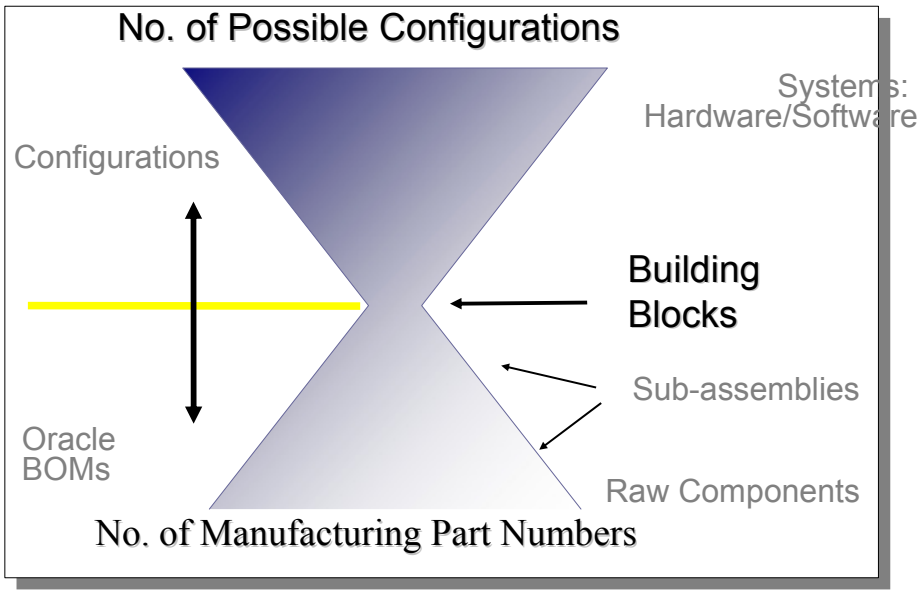
Response to the competitive pressure

- Reduce the number of parts we need to manage
- More leverage of our spend / gain economies of sale
- Faster response to demand changes
- We need less steps movements, touches

Sun's "One Touch" Supply Chain

- ✓ ***Product Structure/Simplification***
- ✓ ***Supplier Consolidation/Leverage***
- ✓ ***Supply Chain Visibility***

Product Structure Simplification



Sun's "One Touch" Supply Chain

- ✓ ***Product Structure Simplification***
- ✓ ***Supplier Consolidation/Leverage***
- ✓ ***Supply Chain Visibility***

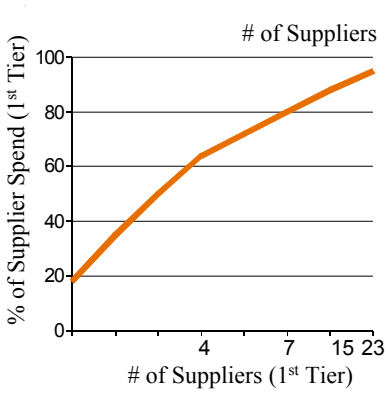
Supply Chain Leverage

90%+ manufactured outside Sun

Using Best-In-Class Manufacturing and Logistics Suppliers

- Advantages:
- Lower cost geography
- Variable cost model
- Leverage economies of scale
- Fewer Hand-offs
- Fewer Mark-ups

Focused Supplier Spend



Supply Chain as Virtual Enterprise:

- Long-term strategic relationships
- Rationalized base
- Leverage partner capabilities
- Technology and robust business processes strengthen relationships

Sun's "One Touch" Supply Chain

- ✓ ***Product Structure Simplification***
- ✓ ***Supplier Consolidation/Leverage***
- ✓ ***Supply Chain Visibility***

Supply Chain Visibility to Customer Orders

The complete supply chain has visibility to customer order impact.

Supply Chain as Virtual Enterprise:

Benefits:

- Removes links/hand off to speed communication
- React to real demand vs forecast

Sun's "One Touch" Supply Chain

Supply Chain Practices:

- ***Direct Ship and In-Transit Merge (CFIT)***
  - No material leaves the supplier without an order
- Customer Ready Systems (CRS)
  - System and software configuration done in factory
- Software Configuration at Manufacture
  - Software configuration on the web, done at source's site

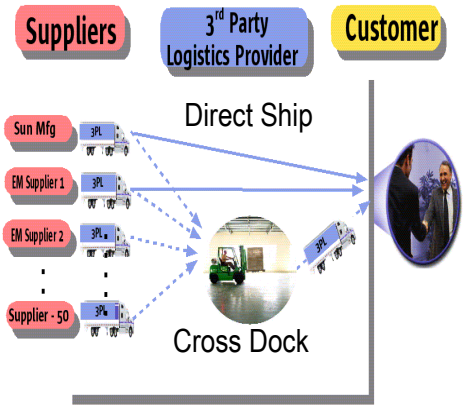
Lead Times

Rapid
Customer
Fulfillment

Speed and Predictability:

- Orders scheduled to fixed, competitive leadtimes (3-10 days)
- 80% of all Ship Sets with leadtimes of 4 days or less
- Postponement at the Building Block level

Material Movement to Customer Order In-transit merge



Benefits:

- Cut inventory
- Reduced warehousing costs
- Record supply chain velocity & predictability

Supplier Impact:

- Position inventory
- Actively commit and/or decommit goods for actual orders

Sun's "One Touch" Supply Chain

Supply Chain Practices:

- *Direct Ship and In-Transit Merge (CFIT)*
  - No material leaves the supplier without an order
- ***Customer Ready Systems (CRS)***
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CUSTOMER READY SYSTEMS

- Easy Customer Implementation
- Reliable Deployment
- Faster Time-to-Benefit
- Customized Options and Services
- "Grid on a Skid"

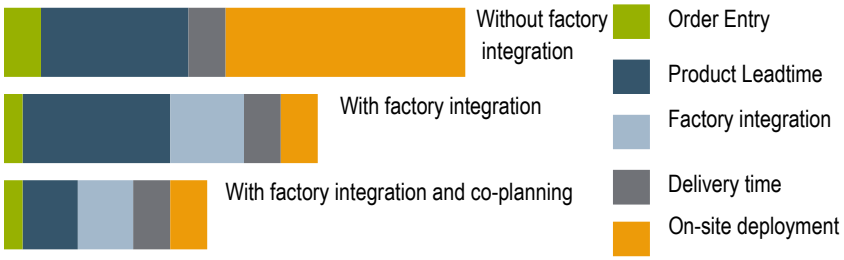
Addressing Customer Needs: Sun[SM] Customer Ready Systems Program

Quicker Deployment for the Global Enterprise

- Customized, factory-integrated and tested systems
- Reduction in system deployment time by up to 90%
- Faster Time-to-Revenue for customers

Faster Deployment

Accelerating deployment time with factory integration



- Product catalogs and building blocks simplify ordering
- Factory integration reduces on-site deployment effort
- Fewer quality issues and a single delivery from a single vendor
- Co-planning reduces product lead time and integration time

Sun's "One Touch" Supply Chain

Supply Chain Practices:

- *Direct Ship and In-Transit Merge (CFIT)*
  - No material leaves the supplier without an order
- *Customer Ready Systems (CRS)*
  - System and software configuration done in factory
- ***Software Configuration at Manufacture***
  - Software configuration on the web, done at source's site

Software Configuration at Manufacture

- Historically the product was moved to a factory or 3rd party for configuration and software load and configuration.
- We now move the software to the build point

Software Configuration at Manufacture

Mid-range Server Example:

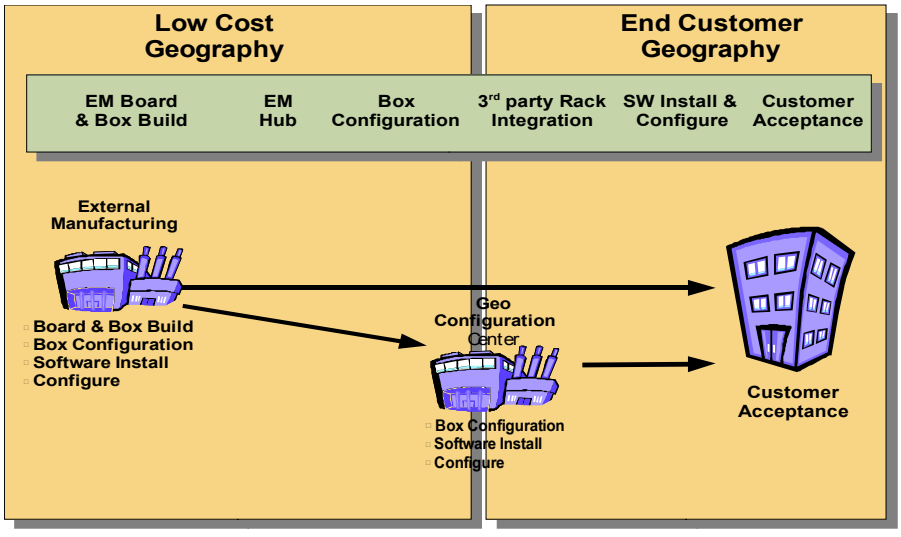
Traditional Approach

- Operating Environment installed manually in the field:
  - Includes Operating System, patches, security modifications, tunables
  - Takes ~4 hours
  - Estimated labor cost = ~$600 (for senior systems engineer)
  - Same steps required for each additional software package installed

Automated

- Installation anywhere on the Internet via Graphical User Interface:
  - > Remote control configuration, includes boot drive, patches, tunables, add-on software packages
  - > Takes <40 minutes
  - > Estimated labor cost < $50 (run by certified engineer, full configuration definition takes <10 minutes)
  - > Hands-off installation; multiple installs can be done in parallel

Server Supply Chain (new)



Faster Customer Time to Value

Project Blackbox: Sun Innovation at Work

Computer
+ Storage
+ Network
+ Power
+ Cooling
+ Software
= Project Blackbox

- Rapid, Easy Deployment: "Build once, deploy anywhere"
- Very High-density Computing: Capacity for over 500 CPUs, 2000 cores, or 8000 compute threads*!*
- Versatility and Flexibility: "What you want, where you want it, when you want it".
- Breakthrough Economics and Eco-responsibility: scalability, standard components, efficiency, cooling innovation
- All in one of the world's most universal form factors – a 20 ft shipping container!

Sun's "One Touch" Supply Chain - Results

Lower Cost -
- Logistics costs have been reduced by 20%
- Overheads reduced by 37% in supply chain

Less Inventory -
- FGI has been reduced by as much as 40%

Faster Delivery -
- Leadtime reduced by 50%
- >80% ships in 4 days or less

Improved Predictability -
- >10% improvement in predictability performance

Faster Time to Value -
- Up to 90% reduction in deployment time

Sun microsystems

Thank You.

The Network is the Computer.™

Keynote

Rising Role of Indirect Materials for Semiconductor Manufacturing

Dr. Susumu Kohyama
President and CEO,
Covalent Materials Corporation

9:05am
Monday, October 15, 2007

California Ballroom, Salon 6

Rising Role of Indirect Materials for Semiconductor Manufacturing

Susumu Kohyama
President and CEO
Covalent Materials Corporation (former Toshiba Ceramics)

In the long semiconductor history, smaller device geometry and larger wafer size have almost always resulted in effective cost reduction, better performance, more functionality and less power consumption. However, device miniaturization to sub-micron together with 300mm wafer process started to create various "Manufacturability" issues. In order to solve or ease such problems, role of indirect materials is increasing so rapidly, therefore collaborations among device manufacturers, semiconductor equipment manufacturers, and also materials and components suppliers become so critical and essential.

Semiconductor industry is experiencing different and serious manufacturability problems, revealed gradually from 130nm node with 300mm wafer process, and more so for the 90nm. Phenomena are more complex for random logics in large-scale system LSI's because of random pattern and multi-level metallization. Extreme lithography combined with variety of new materials resulted in lack of reproducibility and predictability. Process optimizations together with extensive process, device and circuit simulations supported by analysis tools and software improved the situation substantially, but without adequate satisfaction. Those challenges are getting to be more complicated for further device miniaturization down to 65, 45 and 32nm node.

Optimization is often inadequate since total engineering system for manufacturing today is not structured in hierarchical manner, therefore materials and components, equipments, and actual process modules are developed and optimized without sufficient interactions. That's why "design for manufacturing" is often inadequate from both yield and reliability point of view, caused by inaccurate modeling for lithography including all optical process, thin film deposition and etching, and the rest. 300mm prime requires more new materials for both direct and indirect, which amplify those problems even more complicated.

Among various indirect materials, inorganic materials or Ceramics in wider definition are demonstrating rapid and steady progress recently, because of their unique characteristics. In addition to traditional ceramics and their combinations, ceramics compound with rare-earth element also started to play a unique role, especially in extreme environment such with active plasma. Structured components for high precision mechanical components are also essential both inside and outside of various manufacturing equipments. Fundamental material characteristics, mechanical accuracy both body and surface, and all related physical and chemical interactions should be studied and optimized under much wider collaborations in the industry. These efforts must be very important for the 300mm prime, and inevitable for 450mm generation to come afterwards.

Keynote

Less is More

Paul Westbrook
Senior Technologist,
Texas Instruments – International Facilities

1:00pm
Monday, October 15, 2007

California Ballroom, Salon 6

ISSM 2007

Less is More

Paul Westbrook
Sustainable Development Manager
Texas Instruments International Facilities

p-westbrook@ti.com

My Conference Footprint

- Justify my resource use
  - No one actually came here to see me
  - My plane was flying here anyway
    - I only added 0.1% additional weight
  - I rented a compact car
- Easier to justify than make meaningful change

Your Conference Justification

- I love the bay area

- I had to get out of the office

- I had to get out of the house

- I enjoy airport security checks

Why Are We Here?

- Maybe we just want to learn something and do better

Man's mind, once stretched by a new idea, never regains its original dimensions. - Oliver Wendell Holmes

If so, then remember that:

LESS = MORE

waste profit

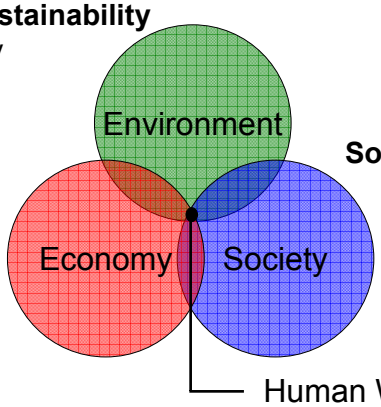
Agenda

- Sustainable Development
  - What
  - Why
- Natural Capitalism
- Buildings and really BIG buildings
- LEED
- Case Study
- Opportunity

Sustainable Development

The Balance of People, Profit, and the Planet

Environmental Sustainability
Ecosystem Integrity
Carrying Capacity
Biodiversity



Economic Sustainability
Growth
Development
Productivity

Social Sustainability
Cultural Identity
Empowerment
Accessibility
Stability
Equity

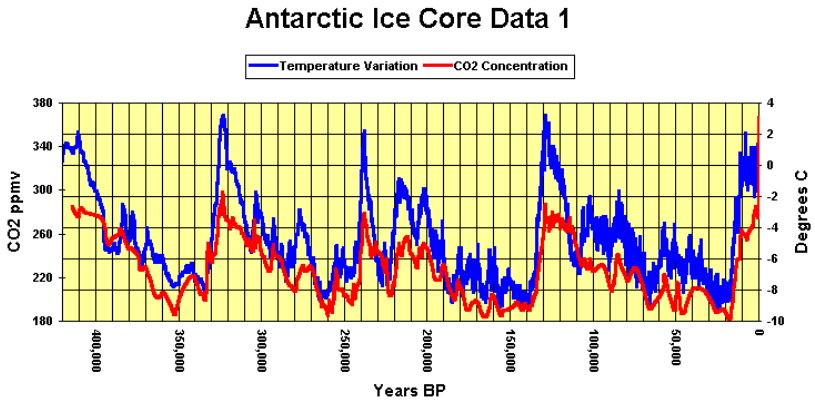
A sustainable system delivers services without exhausting resources. It uses all resources efficiently both in an environmental and economic sense.

Why Change Current Practice?

- Climate Change

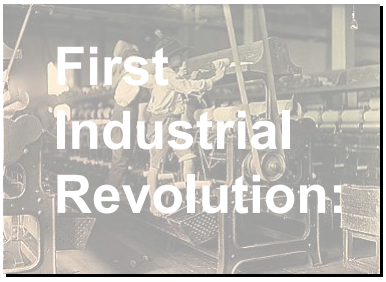
Glacier National Park, Montana

Cyclical, but Modified



Ice core data from the Vostok site in Antarctica were published by Petit et al in the British journal *Nature*.

Revolutionary Idea



People are scarce and nature is abundant – increase labor productivity

Next Industrial Revolution:

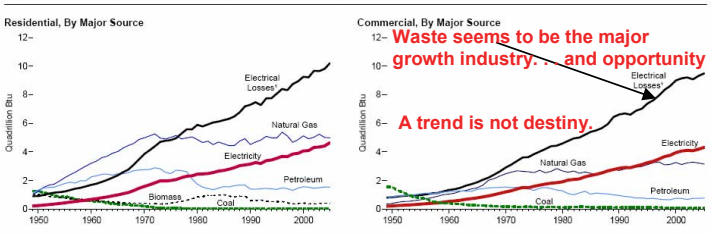
People are abundant and nature is scarce – increase **resource** productivity

REUSE
REDUCE
RECYCLE

Natural Capitalism: **Creating the Next Industrial Revolution**
by Paul Hawken, L. Hunter Lovins, Amory Lovins – 1999 www.natcap.org

Waste Not, Want Not

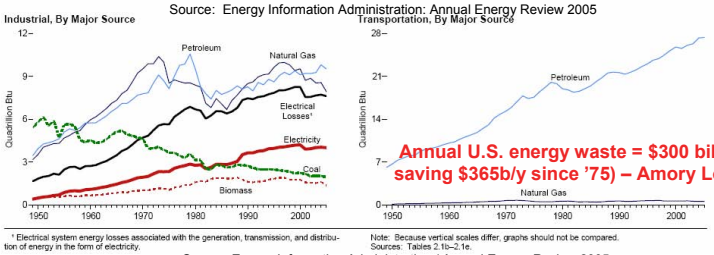
Figure 2.1b Energy Consumption by End-Use Sector, 1949-2005



Waste seems to be the major growth industry. . . and opportunity

A trend is not destiny.

Source: Energy Information Administration: Annual Energy Review 2005



Annual U.S. energy waste = $300 billion (after saving $365b/y since '75) – Amory Lovins, RMI

¹ Electrical system energy losses associated with the generation, transmission, and distribution of energy in the form of electricity.

Note: Because vertical scales differ, graphs should not be compared.
Sources: Tables 2.1b–2.1e.

Source: Energy Information Administration / Annual Energy Review 2005

Capitalism

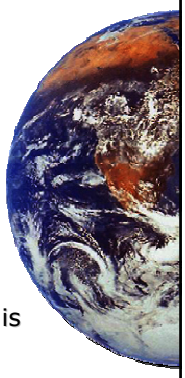
Today we have a temporary aberration called "industrial capitalism" which is inadvertently liquidating its two most important sources of capital.. the natural world and properly functioning societies. No sensible capitalist would do that. – Amory Lovins

"The significant problems we face cannot be solved at the same level of thinking we were at when we created them." - Einstein

"I don't do problems, I do solutions." – Amory Lovins

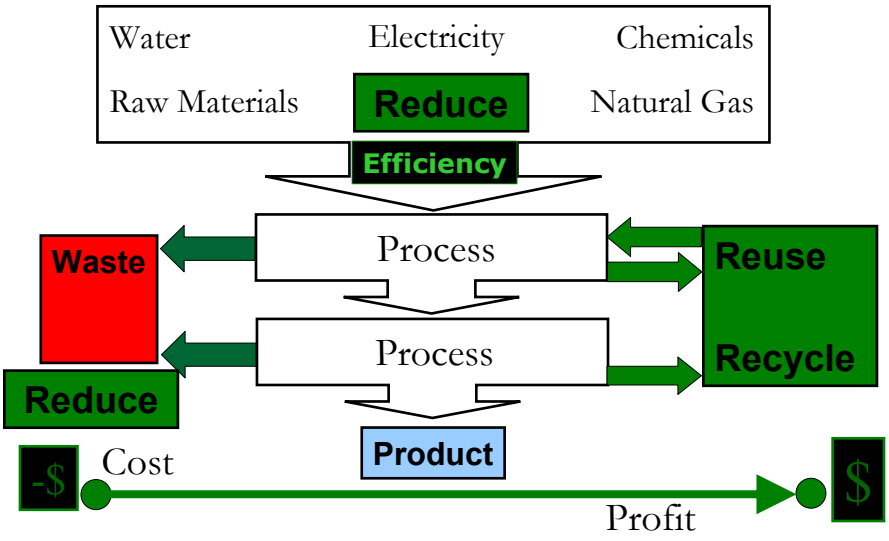
Natural Capitalism

- A way of doing business as if nature were properly valued...but without needing to know what it's worth
- Far more profitable even when natural capital, as now, is valued at zero
- Being rapidly adopted in the private sector for its benefits to people, profits, and competitive advantage

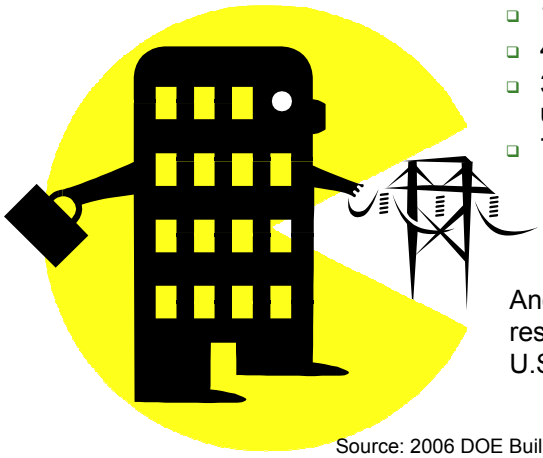


"There is a simple rule about the environment. If there is waste or pollution, someone along the line pays for it."
Lee Scott, Chief Executive, Wal-Mart

Business Model



Buildings



Buildings consume:

- 12% of the potable water
- 40% of the raw materials
- 39% of all primary energy used in the US
- 70% of all U.S. electricity

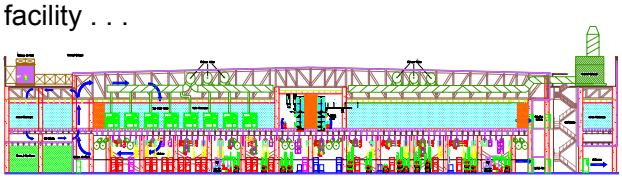
And buildings are responsible for 48% of all U.S. carbon emissions

Source: 2006 DOE Buildings Energy Data Book and USGBC

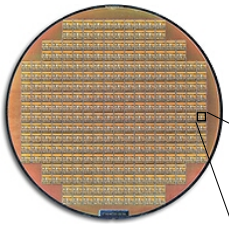
BIG Building – Wafer Fab

A very big, clean facility . . .

Total space:
1,100,000 gsf (102,000 m2)
Clean room space:
220,000 sf (20,400 m2)



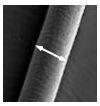
. . . that fabricates very small chips on large silicon wafers



300 mm diameter
1500-5000 chips ea
30,000 wafers/mo
1 billion chips/yr

Gate = 39 nm dia

Hair = 80,000 nm dia



DNA = 2 nm dia
Atom = 0.1 nm dia

The Opportunity

- Very tight temperature and humidity requirements . . .
  - 70F+/-2 (21C+/-1) and 45% RH +/- 3%
- Combined with a large amount of exhaust and subsequent make up air . . .
  - 650,000 cfm (307 m3/sec) = 41 Macy's Snoopy balloons a minute
- Combined with the need to recirculate a large volume of air through the filters for cleanliness . . .
  - 4,400,000 cfm (2077 m3/sec) = 22 Goodyear blimps a minute
- Combined with hundreds of process tools with vacuum pumps, RF generators, and support equipment . . .
- Combined with extensive use of deionized (DI) water to rinse the wafers during processing . . .

Could lead to annual power consumption of 170,000 mWh (10,000 homes worth) and water consumption of 3 million gallons/day (6,000 homes worth). Annual utility bills could total $20M - $25M.

TI Path to Sustainability

- Strategy Team - Fabscape
  - 4 strategy teams were formed in advance of project
  - Request made to add a 5th team - sustainability
  - Generated early white papers on a number of ideas
- Tour (Westbrook House – www.enerjazz.com/house)
  - Invited 3 VP's to tour active/passive solar home
  - Low utility bills for "normal" house spurred interest
- Design Workshop
  - Teamed up with Rocky Mountain Institute (RMI)
  - Held 3-day design charrette to brainstorm ideas
  - Generated 15 "Big Honkin' Ideas" to carry forward along with a large list of other good ideas
  - Made a first pass at LEED score sheet

What is LEED?

Leadership in **E**nergy and **E**nvironmental **D**esign

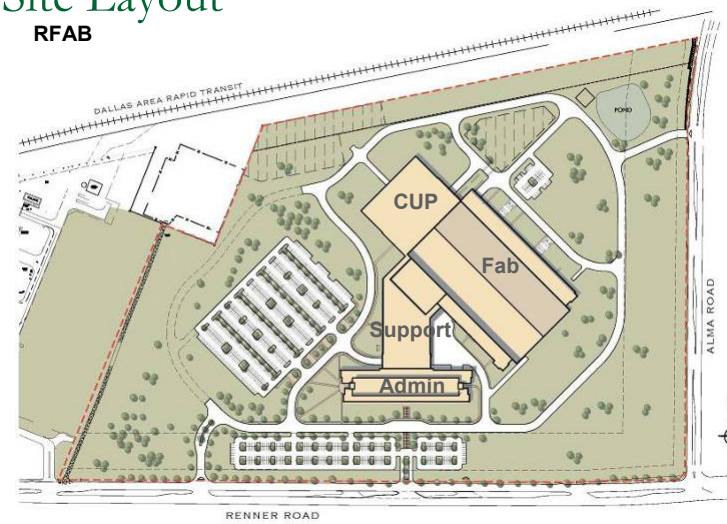
- The **LEED** Green Building Rating System™ is a voluntary, consensus-based national standard for developing high-performance, sustainable buildings. There are 5 broad categories that force an emphasis on a holistic approach to design:
  - Sustainable Sites
  - Water Efficiency
  - Energy & Atmosphere
  - Materials & Resources
  - Indoor Environmental Quality

RFAB – A Case Study

- 92 Acre Site
- 1,090,000 Gross Square Feet
- 220,000 Square Feet of Cleanroom Space
- Population of approximately 1000 Employees
- Building completed in 2006
- Main Components
  - Fab Building
  - Support Building
  - Mechanical Building
  - Administration Building

Site Layout

RFAB



PageSoutherlandPage
The Next 100

Cost Reduction – Friend or Foe?

- The design team was challenged with reducing the fab cost/sf by 30% from the previous fab!
  - Forced space efficiency (2 level vs. 3 level)
  - Forced us to question everything
  - Couldn't just copy previous design – had to innovate
  - All of this led to . . . . Engineering!
- Project was registered with **LEED**
  - Goals: **GOLD** for Admin and **SILVER** for Fab
  - Provided a focusing mechanism for team

Sustainable Sites

- ☑ SS Prerequisite 1 Erosion and Sedimentation Control

Used compost filled tubes instead of typical silt fence

Compost tubes

- ☑ SS Credit 4.1 - Alt Trans, Public Transportation Access

Free shuttle to rail station 1 mile away. Free annual public transportation pass for all TI employees.

- ☑ SS Credit 4.2 - Alt Trans, Bicycle Storage & Changing

Provided covered bicycle parking and showers / lockers

Sustainable Sites

- ☑ SS Credit 4.4 - Alt Transportation, Parking Capacity
  Preferred parking spaces for hybrid cars, vanpools, carpools.
- ☑ SS Credit 5.1 - Reduced Site Disturbance, Protect or Restore Open Space
  Site was a originally a wheat field. Restored large sections with native grasses and wildflowers.



- ☑ SS Credit 5.2 - Reduced Site Disturbance, Development Footprint

Sustainable Sites

- ☑ SS Credit 6.1 - Stormwater Management, Rate and Quantity
- ☑ SS Credit 6.2 - Stormwater Management, Treatment

Pond collects runoff from most of the 92 acres. Capacity = 2.7 million gallon base + 2 million gallon buffer. Pond meters runoff and settles sediment. Pond water is used for all site irrigation.

Windmill drives an air compressor to aerate the pond. >

Sustainable Sites

- ☑ SS Credit 7.1 - Landscape & Exterior Design to Reduce Heat Islands, Site – *reflective concrete, shade trees*
- ☑ SS Credit 7.2 - Landscape & Exterior Design to Reduce Heat Islands, Roof

Sustainable Sites

- ☑ SS Credit 8 - Light Pollution Reduction

Full cutoff down light

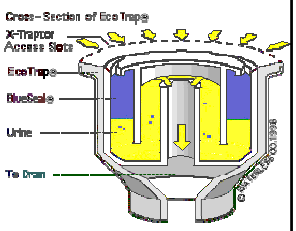
Down light for flag

Bollard – L.E.D. light, solar powered

Water Efficiency

- ☑ WE Credit 1.1 - Water Efficient Landscaping, Reduce by 50%
- ☑ WE Credit 1.2 - Water Efficient Landscaping, No Potable Use or No Irrigation – *Pond is our irrigation source*
- ☑ WE Credit 2 - Innovative Wastewater Technologies
- ☑ WE Credit 3.1 - Water Use Reduction, 20% Reduction
- ☑ WE Credit 3.2 - Water Use Reduction, additional 10% Reduction
  Admin = 39%, Fab = 41%

Water turbine powered sensor faucet



Water Efficiency (FAB)

- Though it's not counted in LEED, there are a number of process water reclaim and reuse steps incorporated:
  - RO Brine is used in the cooling towers
  - Primary Mixed Bed Water is used for CMP polishers
  - Secondary UF for additional water recovery from UF and Polish Beds
  - Secondary rinse bath DI water reclaim
  - IW water used for POU abatement and large exhaust scrubbers
  - Segregate and collect sulfuric acid waste
  - MUA condensate sent to site pond for irrigation use

Energy and Atmosphere

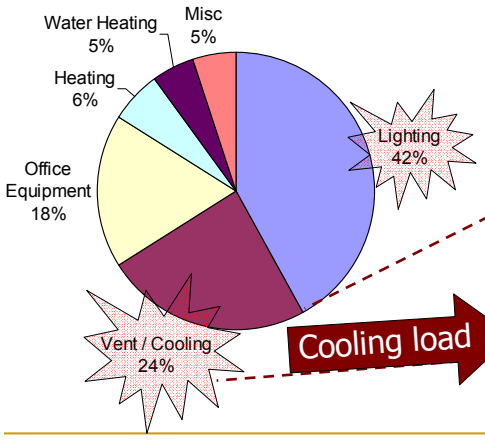
- ☑ EA Prerequisite 1 Fundamental Systems Commissioning
- ☑ EA Prerequisite 2 Minimum Energy Performance
- ☑ EA Prerequisite 3 CFC Reduction in HVAC&R Equipment
- ☑ EA Credit 1.1 - Optimize Energy Performance,
  15% New, 5% Existing (above Energy Code Std)
- ❑ You earn an additional point for every 5% improvement up to a max of 10 points in this category. 5 points (~38% better than code).

ENERGY SAVINGS APPROACH

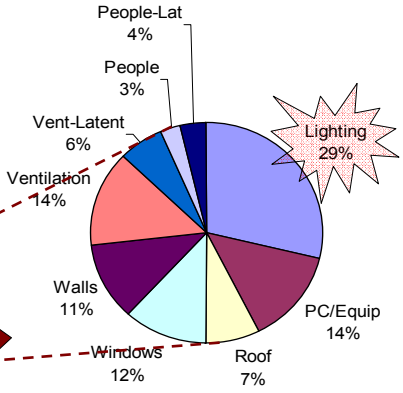
✓ Tools and Support Equipment
✓ Shell efficiency
✓ Facilities systems integration and efficiency

Typical Texas Admin Bldg Energy

Typical Texas Office Building Energy Use



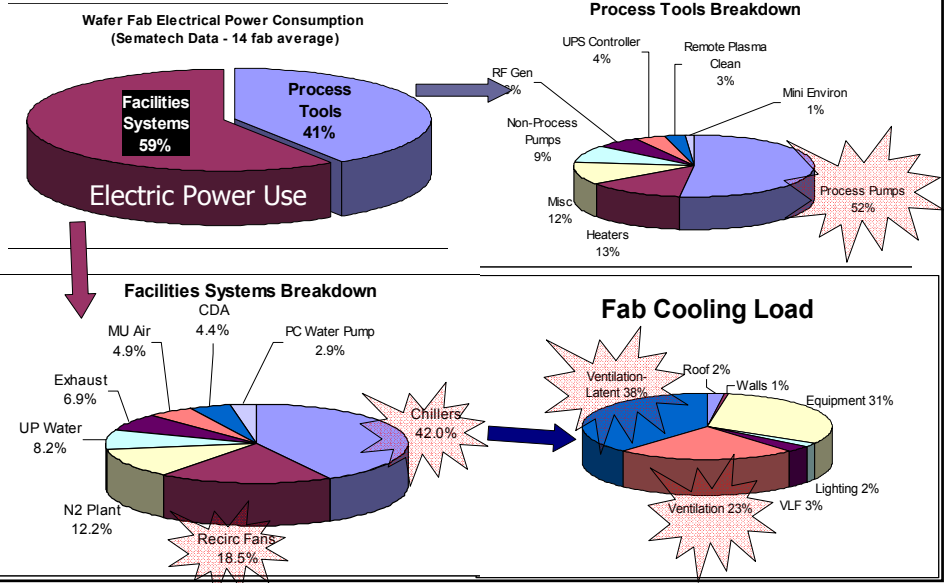
Admin Cooling Load Typical Texas Bldg



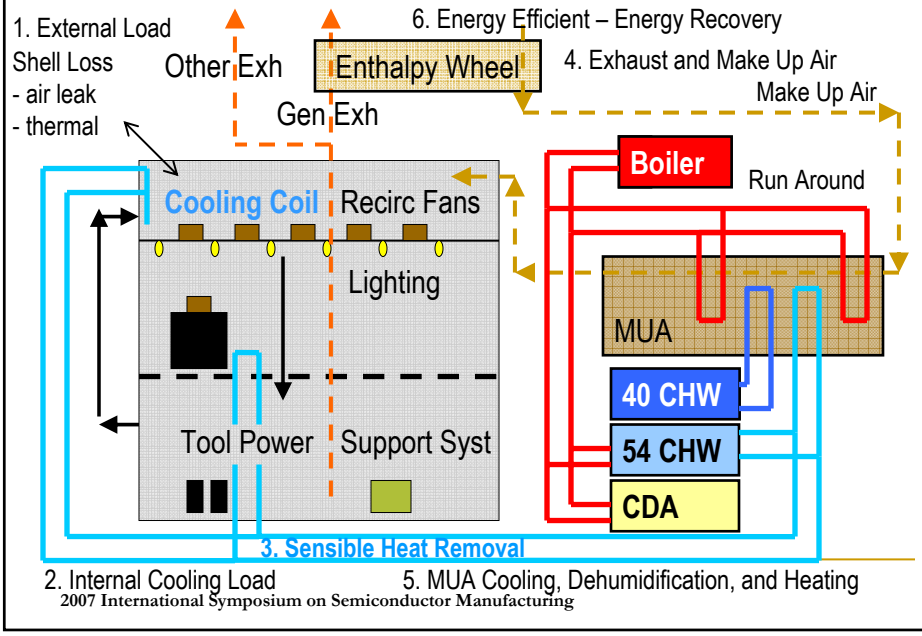
Cooling load

Typical Texas Fab Energy

Newer 300mm fabs are moving closer to a 50% / 50% ratio.



Fab Energy Flow



Energy Savings – Tool Loads

- Vacuum Pumps (*reduced cooling load by >300 tons*)
  - Met with suppliers to assess developments in pump efficiency, current OEM testing, and future plans (pumps have improved >35%)
  - Worked with Sematech and vendors to agree on an idle signal protocol
- Exhaust (*reduced exhaust load by >100,000 cfm*)
  - Return some general exhaust (heat) to space
  - Identify top tool internal constraints and work w/suppliers
- PC Water (*reduced system flow by >3,000 gpm*)
  - Reduce pressure drop and increase delta T on tool and support equipment heat exchangers

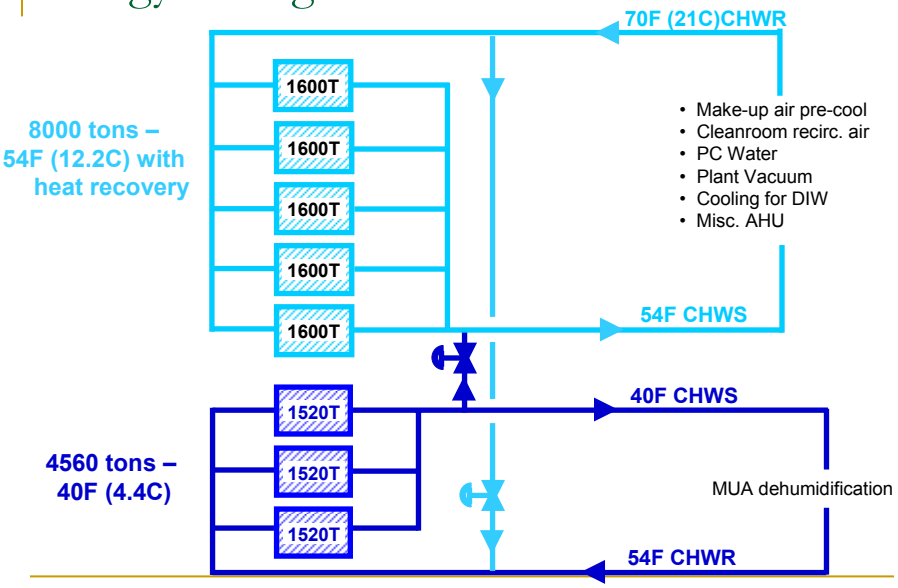
Energy Savings – Shell and Admin

- Passive solar orientation with exterior shading
- Energy and Daylight modeling
- Optimized glazing (high VLT, low SHGC, low U value)
- Reflective roof (high reflectivity, high emissivity)
- Natural daylighting with light shelves
- High efficiency lighting (motion + daylight sensors)
- Demand controlled ventilation (control on CO_2)
- Attention to detail on insulation and infiltration

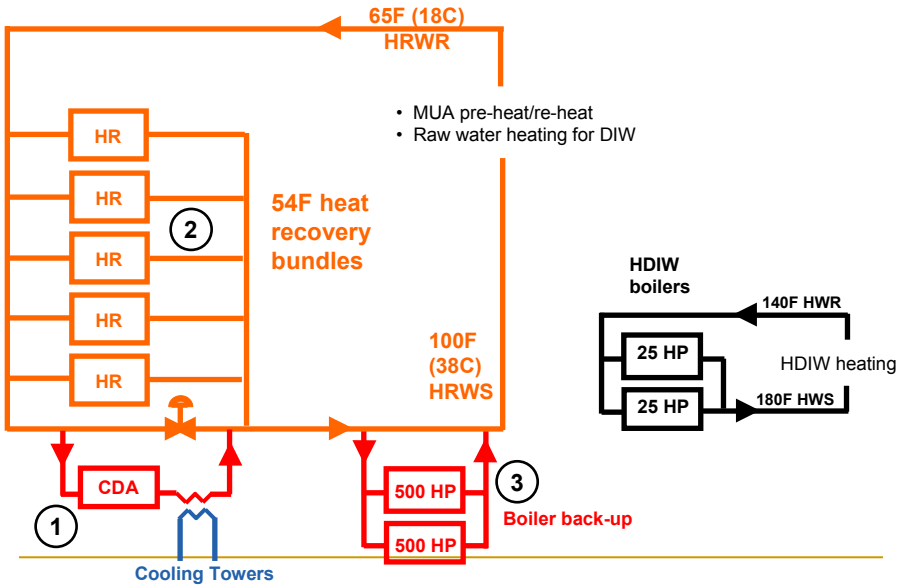
Energy Savings – Central Plant

- Chiller Plant (25% of fab load)
  - Split plant to match needs to capacity
    - 40 deg F for dehumidification (.44 - .51 kW/ton)
    - 54 deg F for all other loads (.32 - .50 kW/ton)
  - Heat Recovery on 54 degree plant (75% of CHW load)
    - More constant load year round
    - Minimal energy penalty for free hot water
    - Reduced boiler count from 6 to 2 (500HP each)
  - Utilize variable primary distribution
  - Redundancy is 1 x 40F chiller for both 40F and 54F (blending for 54F)

Energy Savings – Chiller Plant



Energy Savings – Hot Water



Energy Savings – Air Movement

- Make Up Air
  - Utilized run around coils for free reheat
  - Lowered face velocity to <400 fpm to reduce fan HP
  - Used high pressure humidification instead of steam
  - Investigating enthalpy wheel recovery
    - Recaptures >70% of the exhaust enthalpy
- Recirculating Air
  - 25% HEPA coverage (*300 ton load reduction vs. 50%*)
  - Tested FFU bidders and selected based on efficiency
    - At 90 fpm = 6100 cfm/kW (very good)
    - At 70 fpm > 8000 cfm/kW (excellent)
    - Reduce filter pressure drop, minimize velocity
      - Boosted actual operating efficiency by another 30%!

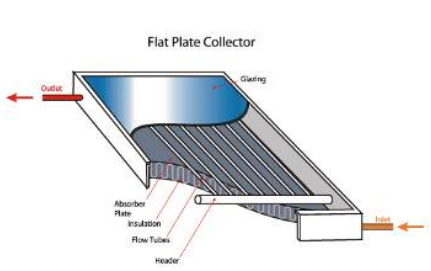
Energy Savings - Pumps, Fans, & More

- Utilize the Big Duct, Small Fan & Big Pipe, Small Pump Idea – minimize friction loss
  - Pretend that every pipeline is a drain line
  - First optimize the piping layout, then layout the equipment
- Utilize Variable Frequency Drives and minimize balancing valves (drive with accelerator, not brake)
- Continue to use premium efficiency motors

We did well. We can do even better.

Energy and Atmosphere

- ☑ EA Credit 3 Additional Commissioning
- ☑ EA Credit 4 Elimination of HCFC's and Halons
- ☑ EA Credit 5 Measurement and Verification
  - "If you don't measure it – you can't manage it"



Danger: Analysis Paralysis

- What is the payback of the following items?

Solar Water Heating

Leather Seats

Crown Molding

- Chances are no one ever asks about payback on the last two, but the first one (which actually has payback) will get analyzed to death.

Integrated Design Example #1

- An example of making the connections
  - Light Fixture Selection

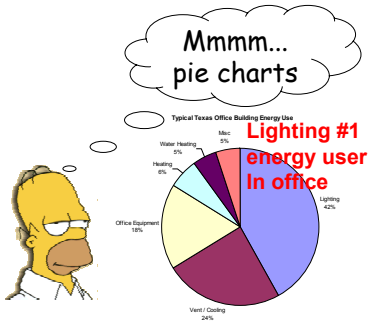
Standard cost = $125
op cost = $40/yr

Ergolight cost = $375
op cost = $25/yr

Simple payback = 16.7 years 

However, we need 30% fewer Ergolight fixtures. Simple payback down to 6.7 years.

Efficient lighting also saves cooling energy. Simple payback down to 6.0 years.



Add the contribution from dozens of similar projects (lighting, reflective roof, light shelves, sun shades, quality windows, extra insulation, vacuum pumps, ...)

Enough cooling load disappears to avoid buying a $1M chiller . . . and the cooling tower, pumps, pipes, and even the space needed to install it.

Simple payback is now 0.0 years. The total net capital cost is the same, or even less, and the operating costs are lowered forever.

Integrated Design Example #1

But wait, it gets even better . . .

Ergolights are individually controllable by each employee
Natural daylighting has been shown to increase productivity

Cost of operation over 30 years for an office building

People costs account for 92% of all costs over a 30 year period.

If natural daylighting, self-control of lighting, improved indoor air quality, and all the other green building factors improved productivity by just 1% that would save the company >$1M/year for a large office complex.

Plus, if people like the building and control over their space it can give companies a recruiting advantage for top talent.

Materials and Resources

- ☑ MR Credit 2.1 - Construction Waste Management, Divert 50%
- ☑ MR Credit 2.2 - Construction Waste Management, Divert 75%
  Almost 90% of construction waste was recycled
- ☑ MR Credit 4.1 - Recycled Content, Specify 5% p.c. or 10% p.c. + p.I.
- ☑ MR Credit 4.2 - Recycled Content, Specify 10% p.c. or 20% p.c. + p.I. Admin achieved 35%, Fab was 57%
- ☑ MR Credit 5.1 - Local/Regional Materials, 20% Manufactured Locally Admin=76%, Fab= 73%
- ☑ MR Credit 5.2 - Local/Regional Materials, of 20% Above, 50% Harvested Locally Admin=71%, Fab= 30%+
- ☑ MR Credit 7 - Certified Wood
  Admin=79%, Fab= 100%

Indoor Environmental Quality

- IEQ Prerequisite 1 - Minimum IAQ Performance
- IEQ Prerequisite 2 - Envir Tobacco Smoke (ETS) Control
- IEQ Credit 1 - Carbon Dioxide (CO2) Monitoring
- IEQ Credit 3.1 - Construction IAQ Management Plan, During Construction
- IEQ Credit 3.2 - IAQ Mgmt Plan, Before Occupancy
- IEQ Credit 4.1 - Low-Emitting Materials, Adhesives & Sealants
- IEQ Credit 4.2 - Low-Emitting Materials, Paints
- IEQ Credit 4.3 - Low-Emitting Materials, Carpet
- IEQ Credit 4.4 - Low-Emitting Materials, Composite Wood

Indoor Environmental Quality

- IEQ Credit 5 - Indoor Chemical and Pollutant Source Control
- IEQ Credit 7.1 - Thermal Comfort, Comply with ASHRAE 55-1992
- IEQ Credit 7.2 - Thermal Comfort, Permanent Temperature & Humidity Monitoring
- IEQ Credit 8.2 - Daylight and Views, Views for 90% of Spaces

Innovation

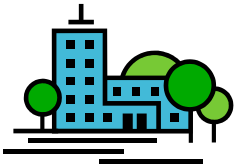
- There are also (4) additional points available for innovation and/or areas where you achieve well above and beyond the standard credit point
- There is (1) point for having a LEED Accredited Professional working on the project
- Big Benefit of LEED
  - Provided a mechanism to get people to focus on making good choices for the long term good of the building and occupants

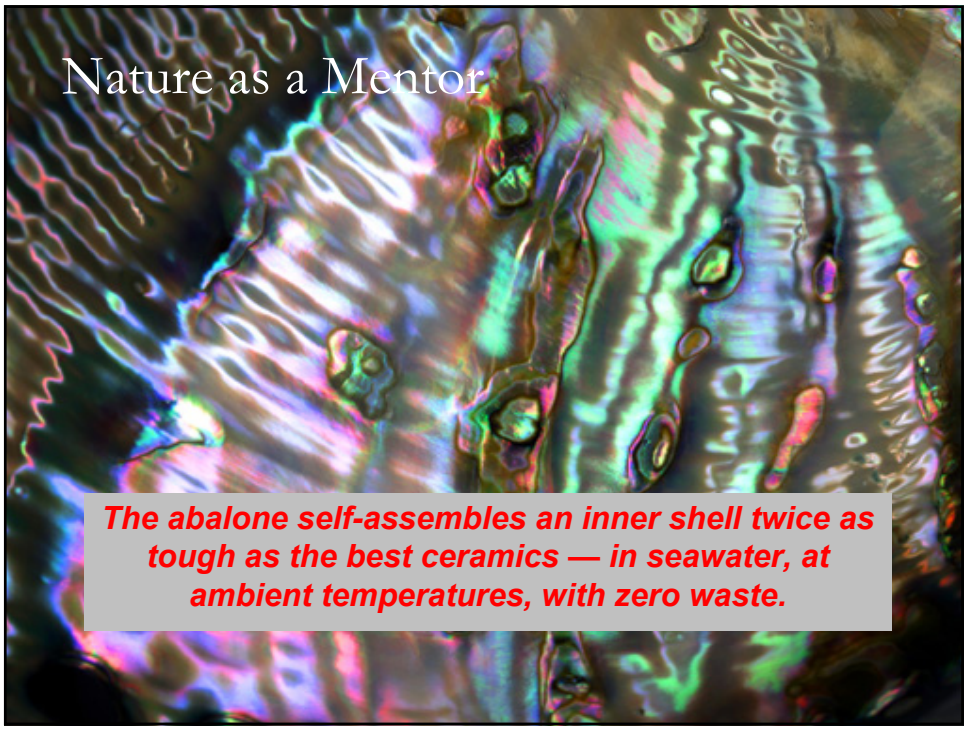
TI RFAB

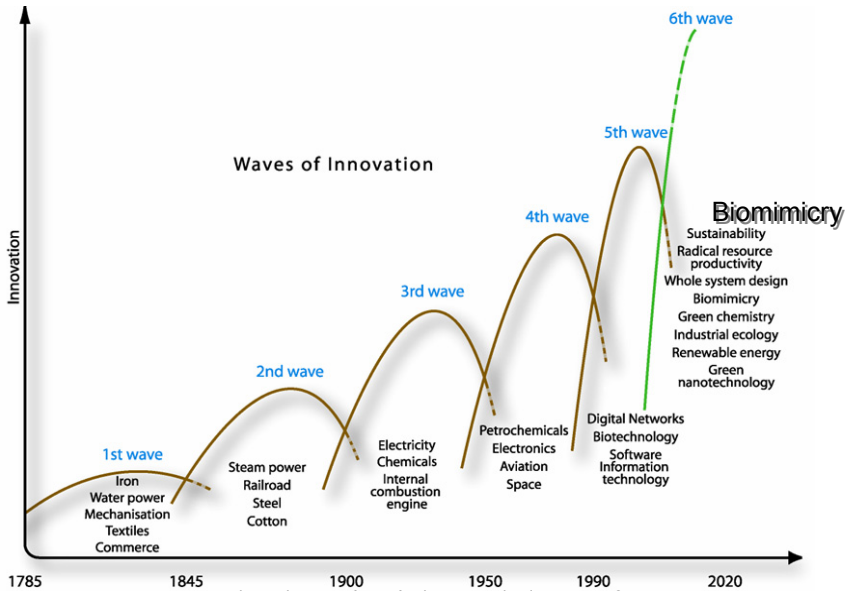
Cost / Benefit

- We will invest <1% of the project cost (<$1.5M) in LEED related items – predominately efficiency improvements that we would consider regardless of LEED
- But remember that the overall project cost 30% **LESS** than our previous 300mm fab.
- The first full year we should recover $1M in operating savings
- At full build out we will save >$4.0M per year in operating costs`
  - 20% energy reduction
  - 35% water use reduction
  - 50% emissions reduction

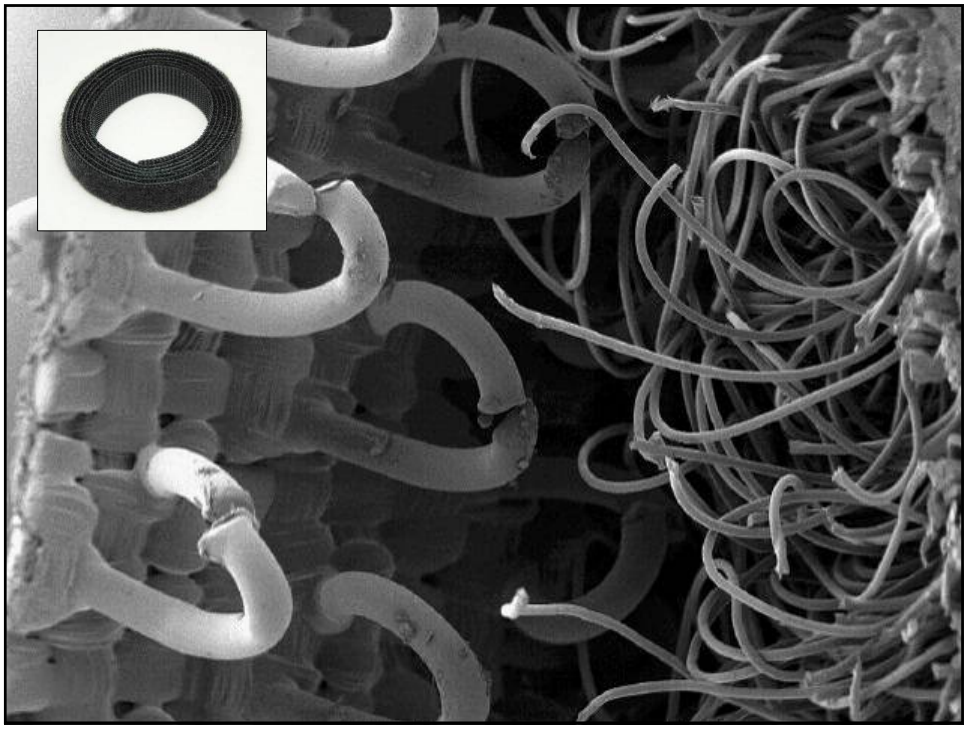
www.ti.com/rfab







Hargroves, K. and Smith, M.H. (2005) *The Natural Advantage of Nations: Business Opportunities, Innovation and Governance in the 21st Century*, Earthscan, London.



Your Turn

- You've had the power to make changes all along
- Opportunities await
- Use nature as a mentor
- Value the earth's services – they will become increasingly more valuable
- *The environment and the economy are undeniably linked – even if we have been denying it for centuries.*

ISSM 2007
Session Topics

DM: Design for Manufacturing
This area includes discussion of collaboration between design and manufacturing. Techniques for verifying resolution enhancement techniques and OPC are included.

- Optical Proximity Correction
- Design Rule Checks
- Rapid Process Qualification
- Enlarging Process and Yield Windows
- Device Simulation

ES: The Green Factory – the Role of EHS
This area focuses on reduction of energy consumption, recycling of chemical reagents, and reduction of the environment footprint of manufacturing.

- Emissions / Effluents Control
- Energy Saving
- Recycling
- Safety and Health
- Community Involvement
- Ergonomics
- Zero Emission
- Global Environment Protection

FD: Factory Design and Automated Material Handling
This area focuses on fab design and its key enablers to meet the flexibility, extendibility, and scalability needs of a cost-effective leading-edge fab.

- Fab and Cleanroom Design
- Equipment Layout
- New Fab Concepts (Extendibility, Scalability, Agility)
- Mini-environments / FOUP / Automation / Assembly
- Automation and Material Handling System
- Mini Line / Ultra Short Cycle Time Line

MC: Manufacturing Control and Execution
This area includes systems for manufacturing execution and decision support systems, factory scheduling, and control of equipment/material handling systems.

- Cycle Time Reduction
- Systems for Flexible Manufacturing
- Scheduling, Dispatching/Simulation and Forecasting Technology
- Integration of Manufacturing and Business Systems
- Factory Floor Control and Automated Exception Handling
- Productivity: Cost Improvement
- Manufacturing and Recipe Management
- Tool and Fab Monitoring
- Factory Systems for Lean Manufacturing

ISSM 2007
Session Topics

MS: Manufacturing Strategy and Operations Management
This area focuses on strategy and concepts for more efficient factories and their operation management to meet rapidly changing complex business requirements.

- Organizational Design
- Capital Productivity
- Education and Training
- Resource Management
- Total Productive Maintenance
- Quality Management
- Supply and Logistics
- Manufacturing Agility
- Ramp to Volume
- Risk Management and Mitigation
- Manufacturing Business Model

PC: Process and Equipment Control
This area focuses on tighter process control for 90nm/65nm production, systems to enabler faster ramps to volume production and higher uptime by equipment and process monitoring.

- Line Process Feedback / Feed forward Control
- Process Control Spanning Multiple Process Steps
- Equipment Embedded APC
- Equipment and Process Monitoring
- Fault Detection and Classification
- Equipment Performance Measurements
- Inline and In situ Measurements
- Statistical Approach for Equipment and Process Diagnostics
- Robust Engineering
- Design of Experiment
- Quality Engineering

PE: Advanced Process and Metrology Equipment
This area focuses on improved pattern definition and control and the metrology needed to achieve those improvements. The application of equipment engineering system will be highlighted.

- New Equipment Architecture and Design
- Equipment Performance Evaluation
- Maintenance Practices
- Design of New Unit Process and Module
- Defect Reduction in Individual Equipment
- Measurement / Metrology Process Improvement
- Equipment Engineering Capability Compatible Design
- Tool Matching
- Variation Reduction and Process Stability

ISSM 2007
Session Topics

PO : Process and Material Optimization
This area focuses on high productivity manufacturing processes for the miniaturization and cost reduction, including software applications for modeling, simulation and test.

- Process Simplification
- Low-cost Process Integration
- Material for Process Optimization
- Unit Process Modeling
- Precision Process Technique
- Defect Reduction and Process Integration
- Novel Process Techniques
- Optimization of Test Wafer
- TCAD Process Analysis
- Reliability Improvements

PT: Advanced Packaging and Test
This area focuses on the processes such as Back Grinding, Dicing, Packaging and Final Test which are applied after wafer processing. Advanced systems for packaging (including SiP), simulation, and optimization of test programs and sampling are included.

- Advanced Wafer Level Package
- Wafer thinning and Dicing Technology
- Back End Process and Property Simulation
- 3D Packaging Technology and Property Simulation
- Environmental Consideration for Back End Process
- Test Strategy Optimization

SC: Supply Chain Integration
This area focuses on coordinating the supply chain through within a factory and across factories for the entire manufacturing chain. Techniques for inventory management, scheduling, on delivery will be discussed.

- Supply Chain Management
- Inventory Management
- Just-In-Time Delivery Techniques
- Distribution Network Modeling
- Demand Planning and Forecasting

YE: Yield Enhancement and Contamination Control
This area focuses on yield enhancement technology including inspection, analysis and reduction of defects and particles. Discussion on contamination control will also be included.

- Defect Detection, Classification and Control
- Preventive Defect Monitoring and Feedback
- Advanced Inspection Methods
- Line-Yield Estimation Methodology
- Yield Modeling and Enhancement
- Failure Analysis (FA) Techniques, FMEA and FTA
- System for Quick Root Cause Analysis
- Contamination Control
- Low Cost Cleaning
- Wet/Dry Cleaning Process and Equipment
- Mini-environments / FOUP

See individual folders for ISSM papers.

Page numbers on the ISSM papers will reflect the pages in the ISSM 2007 Conference Proceedings printed book.

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