An 8-b 400-MS/s 2-b-Per-Cycle SAR ADC With Resistive DAC

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***Abstract*—An 8-b 400-MS/s 2-b-per-cycle (2 b/C) successive approximation register (SAR) analog-to-digital converter (ADC) is fabricated in 65-nm CMOS. With the implementation of a low-power and small-area resistive DAC and associated highly integrated circuit implementation, the proposed SAR ADC achieves rapid conversion rate, low power, and compact area, leading to SNDR of 44.5 dB and SFDR of 54.0 dB, at 400 MS/s with 1.9-MHz input. The measured FOM is 73 fJ/conversion-step at 400 MS/s from 1.2-V supply and 42 fJ/conversion-step at 250 MS/s from a 1-V supply. The active area with the digital calibration is 0.028 mm^2.**

***Index Terms*—Analog-to-digital converter (ADC), resistive DAC, successive approximation register (SAR), 2-b-per-cycle (2 b/C).**

I. Introduction

SUCCESSIVE approximation register (SAR) analog-to-digital converters (ADCs), which perform the conversion with only one comparator, achieve lower power with higher efficiency when compared with other types of ADCs [1]–[4]. Based on its highly digitized architecture, state-of-the-art SAR ADCs consume less and less power benefiting from CMOS technology down-scaling and provide very efficient solutions for a wide range of specifications. Typically, the SAR ADC is appropriate for low-bandwidth applications because it requires $N + 1$ or more clock cycles to obtain N-bit resolution. Achieving a moderate resolution SAR ADC for very high-speed applications, namely, over 150 MS/s, implies a tough design of the dynamic comparator. Time-interleaved implementations enhance the speed, but imperfections such as timing skew and channel mismatch limit the resolution [4]. Obviously, the power effectiveness remains the same because an increased speed entails the multiplication of hardware and power.

An effective way used to augment speed is employing more than one bit per SAR cycle [5]. Multiple comparators make a conventional SAR ADC topology a multibit/cycle (Mb/C) SAR. The number of conversion periods diminishes by a factor equal to the number of bits per SAR cycle. However, more than two-bit/cycle (2 b/C) is not recommended because multiple reference voltages required for the comparator's decision, which must be generated with a proper accuracy, increase the area and the power. In addition, the comparator offsets induce linearity errors, which degrade the ADC accuracy.

This design is a power-efficient ADC solution with up to 400-MS/s conversion rate based on a (2 b/C) SAR topology that uses a resistive-based 2-b DAC and several power/area reduction techniques [6], like interpolation [7] in the sampling network, which reduces 33% of the hardware of the sampling circuit, DAC switches, and digital decoder. Moreover, cascaded inverters in the decoder instead of the conventional AND/NAND gates saves about half the number of transistors, leading to low-power performance and faster operation. Furthermore, a cross-coupled bootstrapping network alleviates the signal-dependent clock feed-through.

In the organization of this paper, Section II presents the architecture analysis of the resistive DAC-based SAR ADC in order to obtain optimum performance. Section III introduces the implementation of the proposed ADC with different circuit techniques that comprise interpolated sampling circuits, cross-coupled bootstrapping network, resistive DAC, cascaded-inverter based decoder, and offset calibration. Section IV describes the layout considerations achieving a very compact design that allows significant power reduction. In Section V, the experimental results obtained from a 65-nm CMOS chip implementation clearly demonstrate the ADC performance. The conclusions are drawn in Section VI.

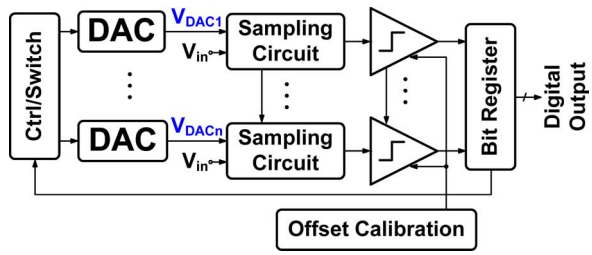

Fig. 1. Architecture of Mb/C SAR ADC.

II. ADC Architecture and Analysis

Fig. 1 shows the conceptual block diagram of an Mb/C SAR ADC where sampled input signals are successively compared to voltages (V_{DAC1} to V_{DACn}) generated by multiple DACs. The requirement of minimizing the mismatch of comparators' offset voltage is satisfied by digital offset calibration network.

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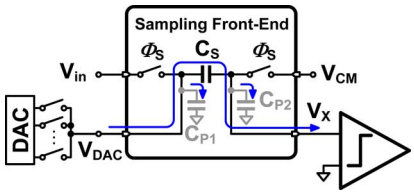

Fig. 2. Passive sampling front-end circuit.

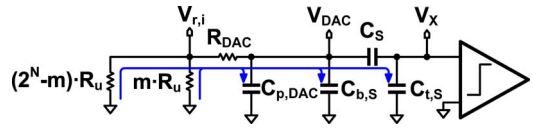

Fig. 3. *R-C* model of the DAC settling path.

TABLE I
ESTIMATED 6-B ADC PERFORMANCE VERSUS SAR CYCLE PRECISION

6-bit ADC	1b/C	2b/C	3b/C
$f_{S,max}$	358MS/s	836MS/s	1.04GS/s
Power @ $f_{S,max}$	3.27mW	3.03mW	4.02mW
FOM @ $f_{S,max}$	143fJ	56.4fJ	60.3fJ

TABLE II
ESTIMATED 8-B ADC PERFORMANCE VERSUS SAR CYCLE PRECISION

8-bit ADC	1b/C	2b/C	3b/C *
$f_{S,max}$	109MS/s	396MS/s	591MS/s
Power @ $f_{S,max}$	4.02mW	4.29mW	8.7mW
FOM @ $f_{S,max}$	143fJ	42.3fJ	57.3fJ

*: Determine 3, 3 and 2 bits in three subsequent SAR cycles.

Following the comparator array, a bit register and a switching network performs the SAR algorithm to determine the digital input of the DACs. The Mb/C structure effectively increases the speed of the ADC, allowing a SAR ADC structure to operate in high-bandwidth applications [8], [9].

There are two possible solutions for the DAC: capacitive or resistive schemes. The capacitive DAC uses a circuit like the one proposed in [5], where a suitable capacitor array, which consumes dynamic power, generates the reference voltages. However, even with two bits, the voltages needed by a differential implementation lead to a six-capacitances scheme, which means large area and capacitive load.

Early implementations [10] used resistive DACs, but the static power imposed by the required fast settling makes them unsuitable for low power (or occupying large area), especially for N bits resolution that requires 2^N switches and control logic associated with heavy parasitic capacitance (in old technology), thus dominating the chip area and power consumption. However, the use of nano CMOS technology naturally moderates the limits because shrinking diminishes parasitic capacitances and reduces the silicon area required for the digital control. Recent results show optimum figures-of-merit (FOM) [1]–[3], [11]–[13] with high digitization of the ADC. Therefore, resistive-based DACs become valid solutions even for high-conversion rate. In addition, the use of a resistive DAC provides 2^N reference voltages which can be reused in the various steps of the conversion cycle. Thus, only one DAC is necessary for the Mb/C needs, including the generation of differential references.

Fig. 2 shows the detail of the passive front-end circuit. It uses the DAC voltage in series to the sampled input, stored on C_S, for minimizing the capacitive load and speeding up the settling. The circuit gives rise at the input of the comparator to the difference between input voltage and DAC output [14] because C_S behaves as a voltage shifter. The only capacitive load of the DAC consists of the parasitic along the charging path. It includes the parasitic capacitances of C_S, the switch parasitic, and the input capacitance of the comparator. Such a small capacitive load gives rise to a fast settling, enabling a low-power and small-area resistive DAC design with satisfying settling speed.

A. Precision of SAR Cycle

The goal of this design is to optimize ADC speed, power, and linearity in order to find the optimal performance, namely, the lower FOM. The sampling rate is the inverse of the sampling duration plus the SAR cycles, controlled by the analog settling and the digital latency. The *R-C* constant of the DAC (and that of the sampler) determines the settling times; the addition of all of the gate delay in the digital blocks, including comparator, bit register, and decoder, makes the digital latency. In order to estimate the settling, Fig. 3 represents the *R-C* model of the DAC and sampling circuit. $\mathrm{V_{r,i}}$ is the reference voltage generated by an N-bit Kelvin ladder with m unit resistor R_u connected between $\mathrm{V_{r,i}}$ and the ground. R_{DAC} is the resistance of the enabled DAC switch and $C_{\mathrm{p,DAC}}$ models the additional parasitic capacitances of the DAC's switches. $C_{\mathrm{p},S}$ is the plates parasitic capacitance of C_S, including bottom-plate parasitic $C_{\mathrm{b},S}$ and top-plate parasitic $C_{\mathrm{t},S}$. If neglecting the effect of multiple switching on the ladder, the time constant of the DAC settling is

$$\tau = [m \cdot R_u // (2^N - m) \cdot R_u + R_{\mathrm{DAC}}] \cdot (C_{\mathrm{p,DAC}} + C_{\mathrm{p},S}). \quad (1)$$

Since the DAC must settle within half $\mathrm{V_{LSB}}$ to guarantee the linearity, the sampling rate of an N-bit resistive DAC-based SAR ADC [15] with n-bit per step is

$$f_{\mathrm{S}}^{-1} = T_{\mathrm{S}} = \left(\frac{N}{n} + U\right)[\tau\,(N+1)\ln 2 + t_D] \quad (2)$$

where U is the ratio between the duration of the sampling phase and the SAR cycle, and t_D is the overall digital latency. Although the time constant is not the same in different SAR cycles, the SAR phases have to be uniform without implementing the asynchronous SAR logics. Therefore, in the calculation, the worst time constant is introduced to estimate the maximum clock frequency. The value of the sampling frequency f_S predicts the speed limitation of the ADC with different resolutions N, and it helps to estimate its FOM as well.

The power consumed by the resistive DAC, comparators, and digital circuits determines the total ADC consumption. The power of the resistive DAC connected between V_{REF} and ground is given by

$$P_{\mathrm{REF}} = \frac{V_{\mathrm{REF}}^2}{2^{\mathrm{N}} R_u}. \quad (3)$$

TABLE III
ESTIMATED PERFORMANCE OF RESISTIVE DAC-BASED 2 B/C SAR ADC

Resolution (bits)	4	6	8	10
$f_{S,max}$	1.3GS/s	836MS/s	396MS/s	111MS/s
Power @ $f_{S,max}$	2.38mW	3.03mW	4.29mW	6.33mW
FOM @ $f_{S,max}$	115fJ	56.4fJ	42.3fJ	55.5fJ

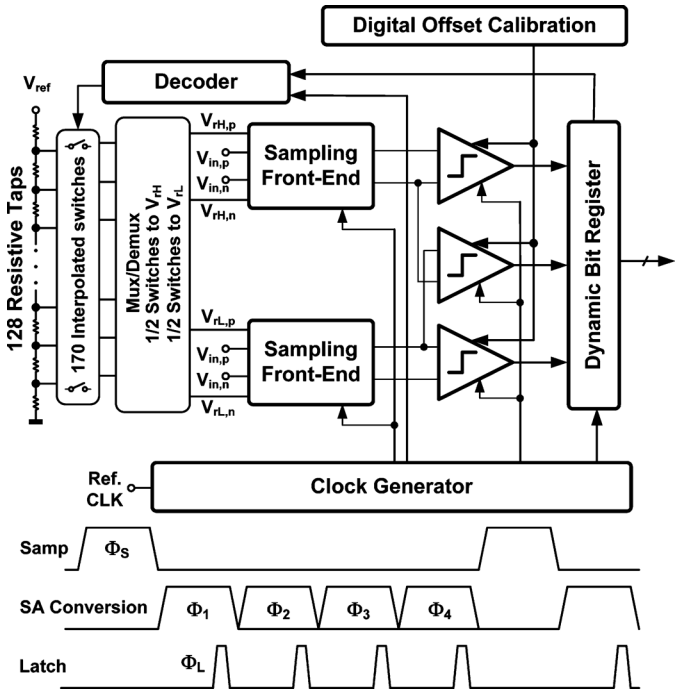

Fig. 4. Proposed ADC architecture and timing diagram.

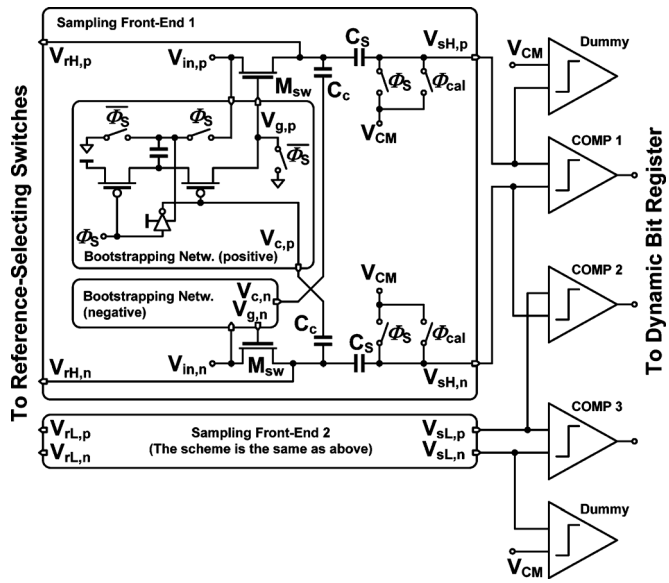

Fig. 5. Implementation of the interpolated sampling front-ends with cross-coupled bootstrapping network.

Also, the power of the digital circuits and comparator are calculated as

$$P_{\mathrm{Digital/Comp}} = f_{\mathrm{CLK}} C_{\mathrm{L}} V_{\mathrm{DD}}^2 \tag{4}$$

where f_{CLK} is the operation frequency of the circuit and C_L indicates the overall switched capacitance. In particular, the C_L of the comparator (including the comparator's load and comparator's intrinsic capacitance) has to be scaled with the ADC resolution, allowing a good noise performance.

The overall DAC resistance is estimated to be 1 kΩ and R_{DAC} is 500 Ω. Each switch's drain or source parasitic capacitance is approximately 0.5 fF, including the proper routing parasitics. Since tens of switches may connect to V_{DAC} at the same time, the overall capacitance $C_{\mathrm{p,DAC}}$ should be 0.5 fF multiplied by the number of connecting switches. The value of $C_{\mathrm{p},S}$ should be around 50% of C_S which can be estimated from the kT/C noise. On the other hand, t_D is close to 250 ps, including the latency in the comparator, bit register, decoder, and intermediate buffers. To estimate the digital power, each gate capacitance is considered to be 5 fF, including the routing capacitance. The total capacitance of the comparator is 80 fF, comprising the extracted capacitance and its MOS-capacitor load for offset calibration as well.

Finally, the above equations estimate the maximum sampling rate and the corresponding power consumption with MATLAB. Accordingly we obtain the maximum achievable FOM, in the case that the ADC achieves its nominal accuracy. Tables I and II summarize the ADC performances for a 6-b and an 8-b ADC with different SAR cycle precision. The ADC speed increases significantly from 1 to 2 b/C, because of two reasons. First, the number of SAR cycles diminishes by 50%. Second, in the 1-b/C structure, 2^N DAC switches connect to a common node of a single sampling circuit, giving rise to a large parasitic capacitance load that slows down the DAC settling. In the 2-b/C structure, the common node of switches is separated by multiple sampling circuits. The capacitive load at each node can be greatly reduced, thus allowing the DAC to settle much faster. Moreover, an interpolation technique (presented later) can be implemented to further reduce the number of switches. The 3-b/C structure still improves the ADC speed, but the enhancement is smaller. Thus, it implies a further doubling of the number of comparators, whose additional side effects are an increase of the comparator's offset calibration hardware, large timing error due to the mismatch of latch phases, and longer latency in the bit register.

The multibit solution benefits the figure of merit and achieves the minimum for 2 bit per cycle. Therefore, the 2-b/C topology exhibits the optimum tradeoff between power and speed.

Moreover, comparing with the 2-b/C SAR structure, another effective way to increase the ADC speed is to use a time-interleaved (T-I) topology. A T-I ADC foresees the multiplication of hardware (and power) and a corresponding increase of speed. However, the FOM of the ADC does not improve or even deteriorates because more power is required by the complex calibra-

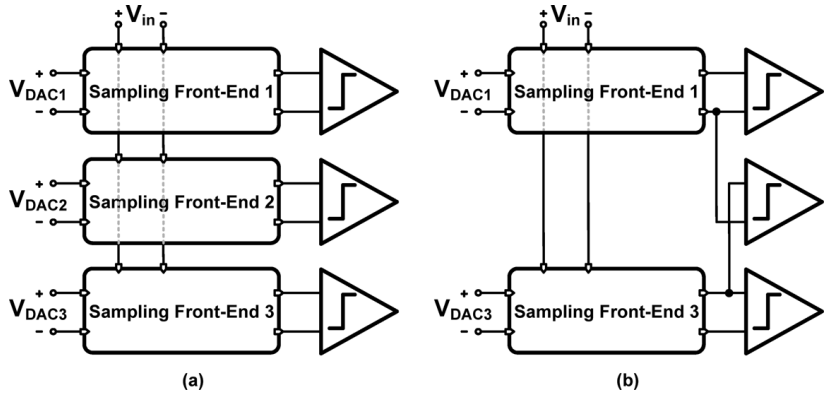

Fig. 6. (a) Conventional and (b) proposed interpolated sampling circuits topology in 2-b/cycle SAR structure.

tion circuits that become necessary to reduce the error between channels. On the other hand, a 2-b/C structure not only improves the ADC speed, but also allows DAC reference sharing, thus improving power effectiveness.

B. ADC Resolution

The performance of the resistive DAC-based 2-b/C SAR ADC also varies with the ADC resolution. With low resolution, the power is low, while the achievable speed is higher. On the other hand, with high resolution, the speed is lower and larger power is required. In particular, for an ADC resolution of 10 b, which exceeds the dynamic comparator's accuracy [16], a preamplifier has to be inserted before the comparator to guarantee the ADC precision, with the power of a single-stage preamplifier estimated in [15]. However, a high-speed preamplifier is quite power-thirsty and it may greatly degrade the ADC efficiency. Therefore, it is necessary to examine the ADC's performance in terms of power and speed, for different ADC resolutions, in order to determine the optimum efficiency point. Finally, (1)–(4) are supposed to achieve full resolution, leading to the results summarized in Table III, obtained with the same capacitor/resistor setting of Section II-A. Thus, a conclusion can be drawn; with a resistive DAC-based 2-b/C SAR structure, a moderate specification of 8 b achieves the best FOM.

III. Circuit Implementation

Fig. 4 shows the architecture and timing diagram of the implemented 8-b 400-MS/s resistive DAC-based 2-b/C SAR ADC. The digital decoder controls 170 switches to provide two differential reference voltages, $\mathrm{V_{rH}}$ and $\mathrm{V_{rL}}$. Two sampling front-ends generate the difference between the input and the references. The differential signals serve a three-level interpolation network with three fast comparators [17], [18]. An on-chip foreground offset calibration circuit [19] minimizes the offset of the comparators. The scheme adjusts the comparators offset with a digital controlled MOS capacitance located at the comparators' outputs. The use of interpolation reduces the number of switches and decoders, thus diminishing consumed power and area. An on-chip clock generator provides the timing phases for the sampling circuit, comparator, bit register, and decoder, with a master input clock equal to the sampling rate.

A. Interpolated Sampling Circuits With Cross-Coupled Bootstrapping Network

Fig. 5 shows the interpolated sampling circuits, where capacitors C_S sample the input signal during the sampling phase Φ_S and hold it for the entire conversion period. The use of a resistive DAC enables a very fast settling with a relatively small dynamic and affordable power, since it is required to charge only the parasitic capacitances. The input range is defined as 1.2 V, peak-to-peak, differential, with a common-mode voltage of 0.3 V equal to the common mode of the reference voltage. V_{CM} is 0.6 V and defines the input common mode of the comparator.

Comparing with the conventional sampling approach in Fig. 6(a), interpolation is able to reduce the number of sampling circuits as shown in Fig. 6(b), implying a saving of the sampling power. An important feature of this structure is the reduction of the number of reference-selecting switches by 1/3, as well as the switches' control logics. Moreover, because the difference of the two provided DAC reference voltages ($\mathrm{V_{rH,p}}$ and $\mathrm{V_{rL,p}}$) in the last SAR cycle has been doubled to be $2\mathrm{V_{LSB}}$, the number of taps in the resistive ladder can be consequently halved (from 256 to 128). As shown in Fig. 6(b), the middle comparator takes the output voltages from the upper and lower sampling networks, which effectively interpolate the extra reference such that a 128-tap DAC is used in this 8-b ADC. In addition, the resolution of the implemented resistive DAC is still 8 b, although it includes only 128 taps. The benefit of tap reduction derives directly from the reduction of the physical length of the resistive DAC, because the minimum length of the unit resistor is limited. Further details will be shown in the reference DAC implementation.

Kickback noise is also an important issue of comparator design. In order to balance this dynamic error, as well as the load of the sampling circuit, two extra dummy comparators are utilized. With identical clock phase and supply voltage, the dummy comparators inject the same amount of charge back to the sampling circuit, as the three functional comparators. When comparators start latching, the two differential outputs of the sampling circuit drop the same amount of voltage because of the equalized kickback. At the end of each latch phase, the sampling circuit will wait for the recovery of kickback before starting the next SAR cycle.

Bootstrapping of the sampling switch makes almost constant the clock feedthrough [21], and the voltage driving the switch,

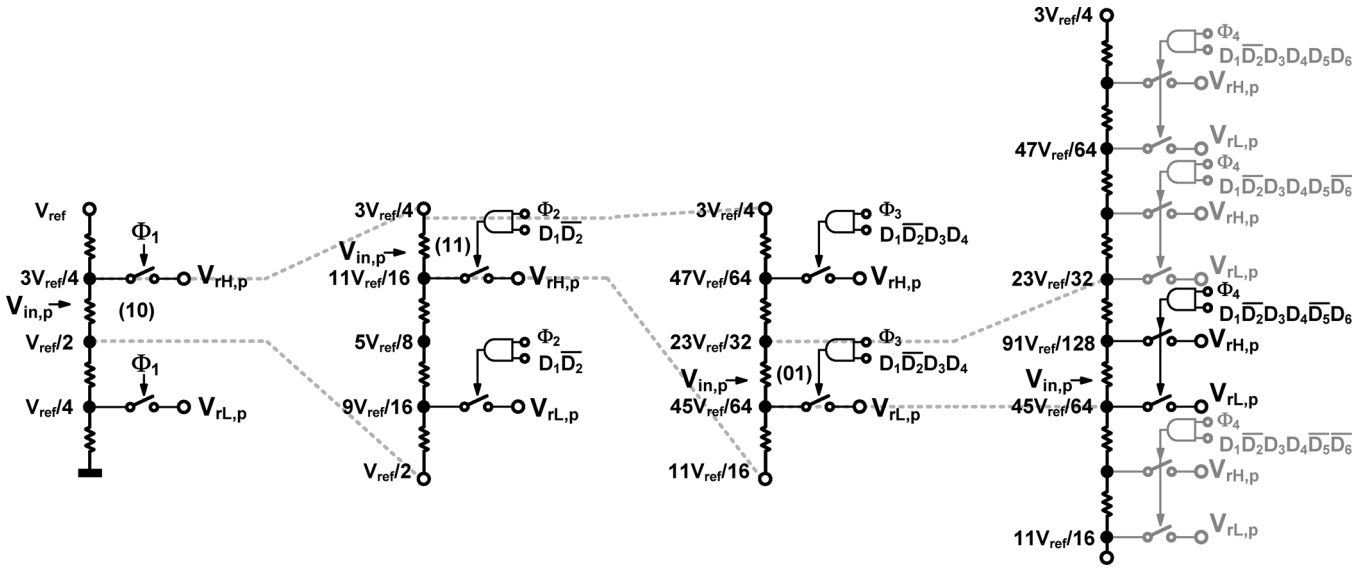

Fig. 7. Switching operation of the reference DAC.

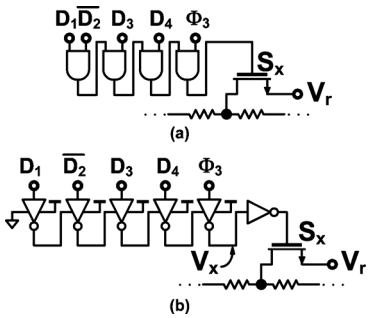

Fig. 8. Different implementations of the decoder unit in the third conversion cycle by (a) AND/NAND gates and (b) cascaded inverters.

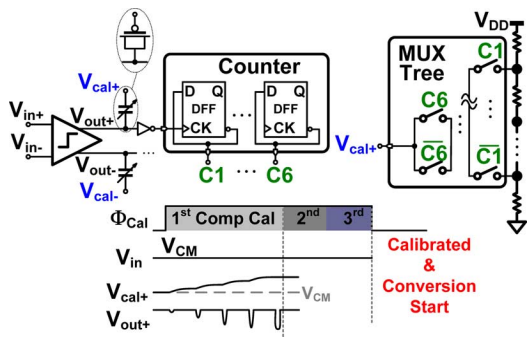

Fig. 9. Implementation of comparator offset calibration.

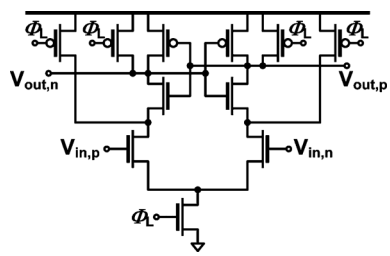

Fig. 10. Circuit implementation of dynamic comparator.

$V_{\rm GS}$, is almost constant. However, since the rising edge of the bootstrapped clock phase depends on $V_{\rm in}$, there is a second-order signal-dependent clock feedthrough term. In this design, it is alleviated by the cross-connected capacitance C_C. The value of those capacitances matches the parasitic $C_{\rm gd}$ of $M_{\rm SW}$.

Comparator offset is a key error term which is attenuated by a foreground digital calibration in this design. When the offset calibration is enabled the differential input of the comparator is shorted to $V_{\rm CM}$ by nMOS switches controlled by $\Phi_{\rm cal}$, as shown in Fig. 5. Subsequently, the calibration logics (presented in offset calibration section), will detect the comparator's output and will unbalance the load of the comparator to neutralize its offset. Once the calibration is over, $\Phi_{\rm cal}$ will be low and the comparators will sense the output of the sampling circuit to initialize normal A/D conversion.

B. Reference DAC

The 128 taps resistive DAC with a total resistance of 750 Ω is connected between $\rm V_{ref}$ and ground. $\rm V_{ref}$ is at midsupply to allow the use of single nMOS as DAC switches. Because of the lower threshold voltage of nMOS transistors, the choice enables rapid settling having minimum parasitic capacitances. Fig. 7 highlights, as an example of a switching operation, the selection of the positive reference voltage of the resistive DAC. The selection to obtain the complementary reference is similar, where $\rm V_{rH,n}$ (or $\rm V_{rL,n}$) $= \rm V_{ref} - V_{rH,p}$ (or $\rm V_{rL,p}$). Each side of the reference generation includes 170 switches (340 switches for overall differential DAC implementation) which have been reduced by 1/3 from the original number of 255, due to the interpolation. The 106 decoder units with the AND function are laid out together with the related switch. The inputs of the decoders are the corresponding approximation phases and the determined digital bits. The ADC approximates the input in four steps. The first step activates the switches that provide $\rm 3V_{ref}/4$ and $\rm V_{ref}/4$ to $\rm V_{rH,p}$ and $\rm V_{rL,p}$. The following steps are similar but the control exploits the determined digital bits. Since the difference of $\rm V_{rH,p}$ and $\rm V_{rL,p}$ of the last step is twice the value of $\rm V_{LSB}$ ($\rm V_{ref}/2^8$), only 128 resistive taps of the DAC

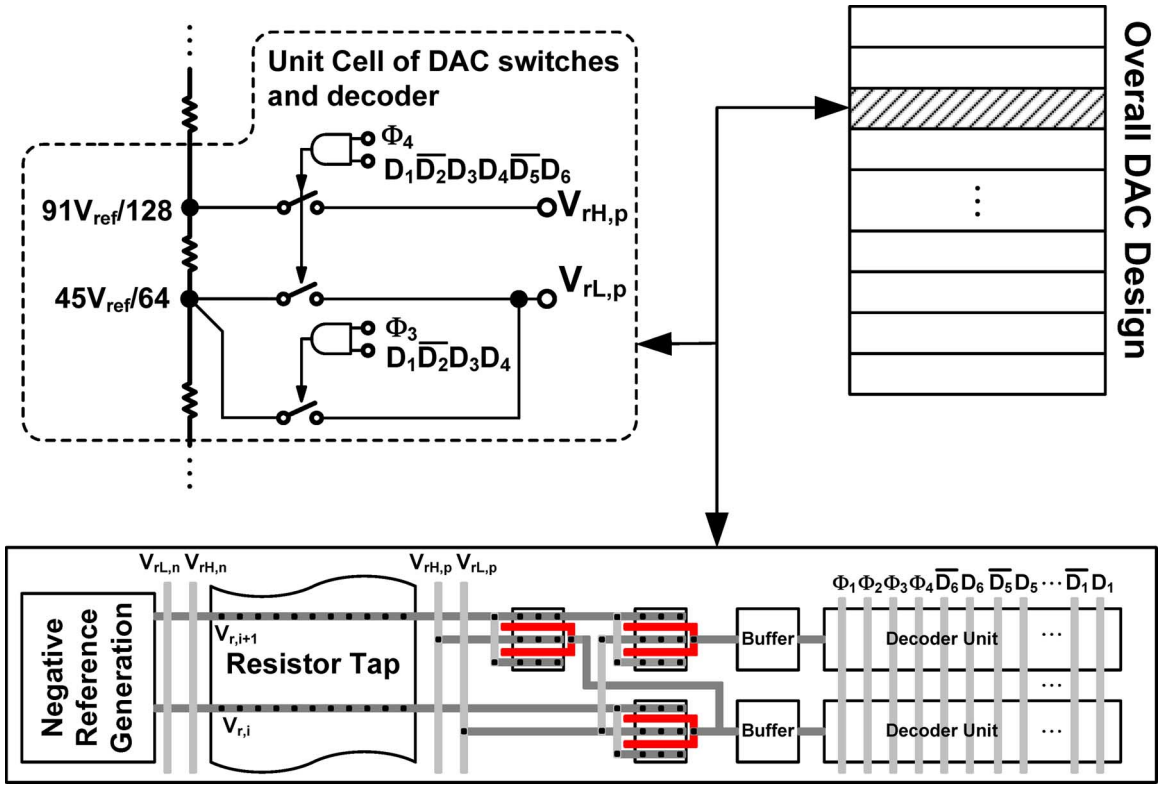

Fig. 11. Layout implementation of DAC unit cell.

are required. Reducing the taps by half saves significant area and alleviates the gradient effect in the DAC. In addition, the two active switches in the last step are physically close to each other in order to share one decoder, thus achieving power and area optimization.

C. Digital Decoder

Fig. 8(a) shows an AND gates structure suitable for decoding the already determined bits and driving one of the selection switches. This design uses the more effective method of Fig. 8(b) made by a special configuration of inverters. The figure shows the 1011 selection control, possibly used at the third step of conversion. The cascade uses the output of an inverter as ground connection of the subsequent one. The decoder design realizes the same function but reduces by approximately half the number of the transistors, saving a considerable amount of power. The operation, similar to pass transistor logic, requires all zeros at the beginning of the conversion cycle for setting the outputs V_X at V_{DD}. The operation is quite fast because the speed only depends on the transition time of the last inverter, while the controls of others are already set.

D. Offset Calibration

Fig. 9 shows the topology [19] of the offset calibration, which is realized by a variable capacitor added to the output of the comparator [20], as shown in Fig. 10. Similar to the previous calibration scheme [18], the comparator offset is compensated by unbalancing the dynamic response of the comparator. The variable capacitor is implemented by a pMOS capacitor, where the gate voltage is controlled by a multiplexer selecting the reference voltage from a resistive ladder. The multiplexer, which is a tree of switches, gives rise to a calibration ramp. The counter changes the calibration capacitor until the crossing of the threshold. Though the ladder exhibits static current, it has been demonstrated to be low because calibration speed is not necessary as fast as in the normal A/D conversion. The additional calibration slightly attenuates the comparator operation speed but to a much lesser extent than the calibration method used in [18] that needs 2^N capacitors for N-bit calibration resolution. Fig. 9 also illustrates the timing diagram of the offset calibration, which is enabled off-chip. Once the calibration is triggered, $\Phi_{\rm cal}$ goes high to calibrate the three comparators sequentially. Once calibration is over, $\Phi_{\rm cal}$ returns to low and the ADC starts conversion.

IV. Layout Considerations

The SAR ADC prototype is laid out in a 65-nm single-poly, seven-metal CMOS with low-threshold option (the value of V_{TH} is approximately 280 mV). One of the most important issues of this SAR ADC is that its approximation loop operates at an extremely high speed: 2 GHz. A compact layout is therefore vital to limit the propagation delay on the metal routings. Special attention is paid to the layout of the resistive DAC, together with its switches and digital decoder, which constitutes the most complex block in the ADC design, since it includes 212 decoder units and 340 controlled DAC switches (for differential reference voltage generation). Indeed, the ADC area is good for more than a general assessment of the ADC performance; a small area design with less parasitic and less gradient enables better performance in both power and speed [22].

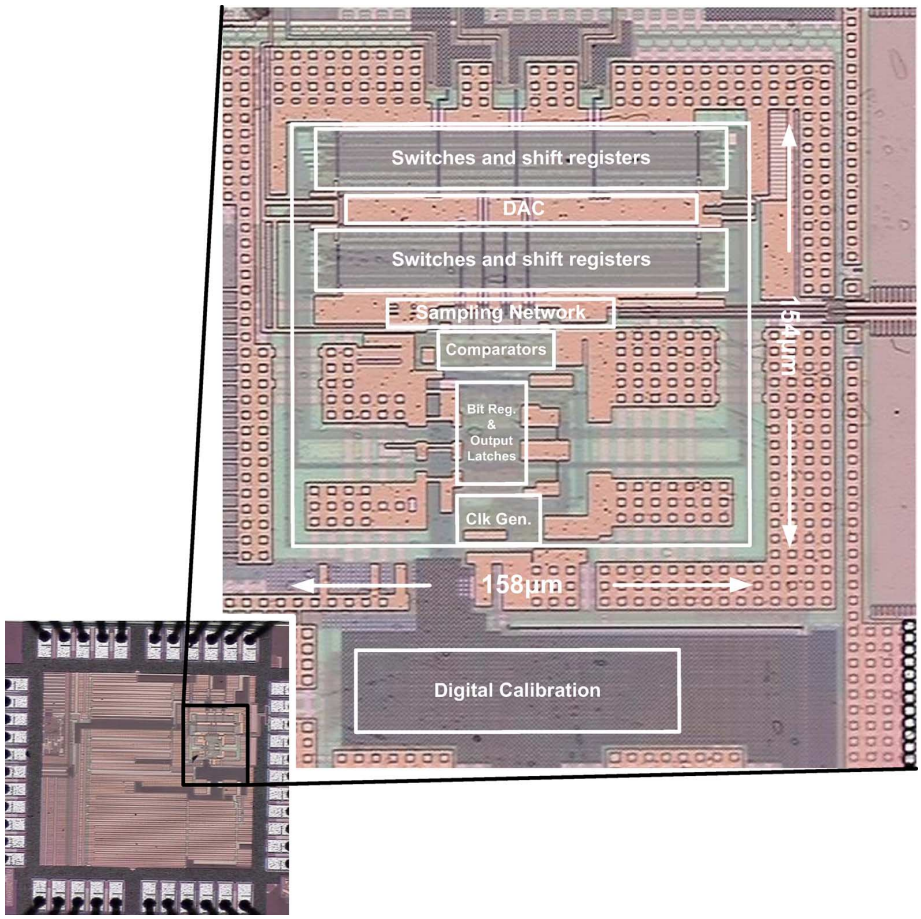

Fig. 12. Chip micrograph.

Tens of unit cells make the DAC and decoder, each of them consisting of two resistor taps and switches. The small width of the rectangular cells minimizes the gradient error of the resistive unity elements. Fig. 11 refers to positive reference generation. The layout for negative reference generation is similar and symmetrical. The switches are implemented with two-finger configuration for minimizing the drain parasitic, load of $V_{rH,p}$ and $V_{rL,p}$. The area of the overall DAC layout is 60 μm$\times$ 140 μm.

V. Measurement Results

Fig. 12 shows the micrograph of the fabricated prototype design. The ADC core occupies 154×158 μm^2, in which the on-chip digital calibration is 35×117 μm^2. The differential nonlinearity (DNL) and integral nonlinearity (INL) measured with either a voltage ramp or a low-frequency sinusoidal wave at the input [23] give rise to the static performance. Fig. 13(a) shows that, before calibration the measured DNL and INL are $-1/+10.2$ LSB and $-8.6/+5.9$ LSB at 400-MS/s conversion rate. With calibration and the same sampling frequency, the nonlinearities are greatly reduced. The DNL and INL become $-0.9/+1.6$ LSB and $-1.5/+1.4$ LSB, as illustrated in Fig. 13(b).

A single tone to the inputs and the recorded code stream measures the dynamic performance of the prototype ADC, with output decimated by 25 times. Fig. 14(a) shows the FFT spectrum for a 1.2 V_{p-p} 1.9 MHz input signal. The SNDR and SFDR are 44.4 dB and 56.4 dB, respectively. Fig. 14(b) presents

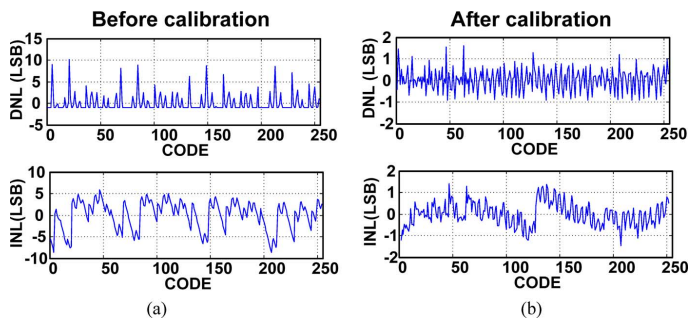

Fig. 13. Measured DNL and INL (a) without and (b) with comparator offset calibration at 400 MS/s.

the output FFT spectrum with input near Nyquist; the SNDR and SFDR are 40.1 and 52.4 dB, respectively. Fig. 14(c) illustrates the measured peak at different sampling rates. The SNDR versus input frequency is plotted in Fig. 14(d) with two different sampling rates. With 400-MS/s sampling frequency and 1.2-V supply, the SNDR is above 40 dB; with 250-MS/s sampling frequency and 1-V supply, the SNDR is higher and above 44 dB. The total dissipated power of the prototype ADC at 400 MS/s is 4 mW from a 1.2-V supply; 0.49 mW (12% of the total) is used for the resistive DAC. Operating at 250 MS/s from 1-V supply, the ADC requires only 1.8-mW power and the DAC uses 0.43 mW (24%) of the total. Table IV summarizes the performance of the proposed ADC. It achieves a very high power

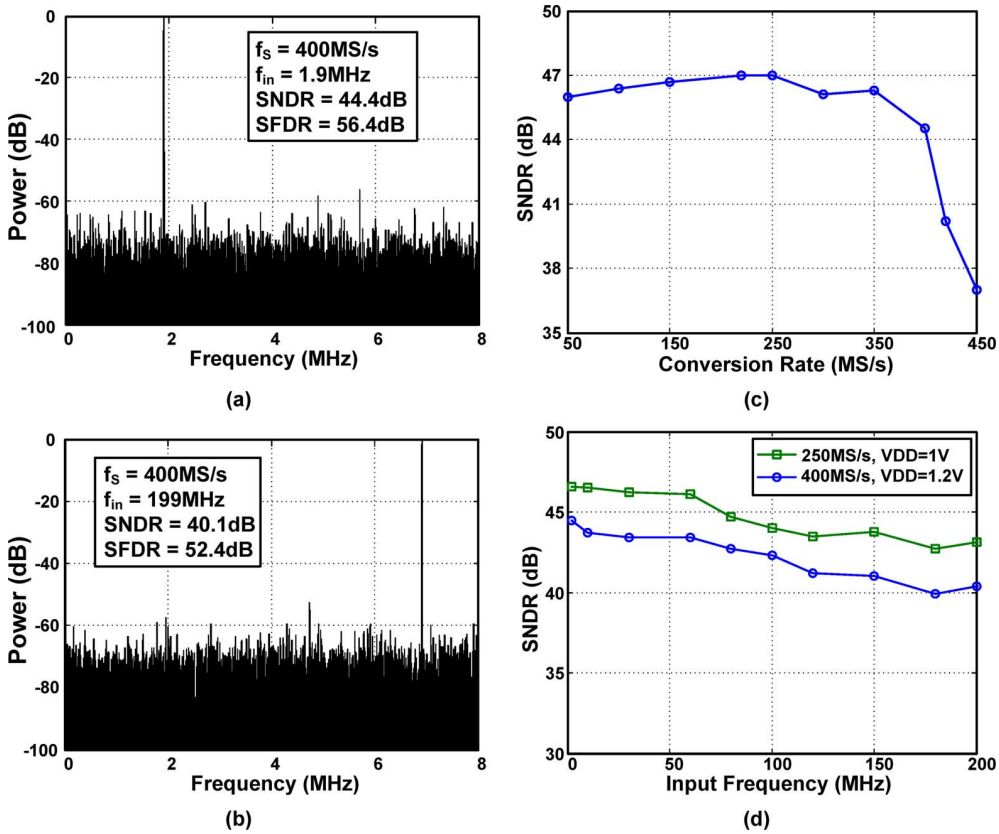

Fig. 14. Measured dynamic performance. (a) FFT spectrum at 2-MHz input (output decimated by 25). (b) FFT spectrum at Nyquist input (output decimated by 25). (c) SNDR versus conversion rate. (d) SNDR versus input frequency.

TABLE IV
PERFORMANCE BENCHMARK WITH STATE-OF-THE-ART DESIGNS

Specifications	This Work		ISSCC'09 [24]	ISSCC'08 [25]	ISSCC'07 [26]	VLSI'11 [27]	CICC'10 [28]
Architecture	SAR		TI-SAR	2-Step	Pipelined	TI-Counter	TI-SAR
Technology (nm)	65		130	90	180	130	65
Resolution (bits)	8		8	8	8	8	10
Sampling Rate (MS/s)	400	250	600	300	200	500	204
Supply Voltage (V)	1.2	1	1.2	1.2	1.8	1.2	1
SNDR (dB)	44.5	46.7	47	46.1	40.3	44.6	55.2
Power (mW)	4	1.8	30	34	8.5	26	9.15
FOM1 @ Low f_{in} (fJ/Conv.-step)	73	42	208	680	-	350	95.4
FOM2 @ Nyquist f_{in} (fJ/Conv.-step)	117	60	340	780	510	380	130
Active Area (mm^2)	0.028		1.1	0.29	0.05	0.55	0.22

efficiency and compact area when compared with the state of the art with similar specifications. It is also faster than the previous single-channel SAR ADC with SNDR $>$ 40 dB [29].

VI. CONCLUSION

This paper presents an 8-b 400-MS/s ADC with resistive DAC-based 2-b/C SAR structure, which has been demonstrated to achieve good efficiency at high conversion speed. Several effective solutions at the circuit and layout level, like the interpolated sampling circuits and cascaded-inverter based decoder, optimize the power/area cost of the ADC. A cross-coupled bootstrapping network and offset calibration enhance the accuracy. The proposed ADC is a valuable solution to solve the stringent tradeoff among power, speed, and resolution and achieves a FOM of 73 fJ/conversion-step at a 400-MS/s conversion rate. Comparing with capacitive SAR ADC, this ADC topology my lose effectiveness at high resolution level, but it extends the application range of SAR ADCs in speed. It is also believed to be a good approach that might scale well into future technologies.

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