Comments and Corrections

Correction to "A 40 GS/s Time Interleaved ADC Using SiGe BiCMOS Technology"

Michael Chu, Philip Jacob, Jin-Woo Kim, Mitch LeRoy, Russell Kraft, and John F. McDonald

In the above paper [1], a mistake in the value of V_t used in the calculation of the third harmonic (HD_3) in equation (1) was discovered by Dr. Kilic of www.um-ic.com. A value of 0.65 V was used in the paper, which is incorrect. The correct value is 25.8 mV. With this proper value, HD_3 is calculated to be -62.9 dB instead of -34.9 dB. The authors would like to thank Dr. Kilic for pointing out this mistake. They apologize for the error.

References

[1] M. Chu *et al.*, "A 40 GS/s time interleaved ADC using SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 380–390, Feb. 2010.

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Correction to "A Sub-μW Embedded CMOS Temperature Sensor for RFID Food Monitoring Application"

Man Kay Law, Amine Bermak, and Howard C. Luong

In the above paper [1], the sampling rate of the proposed temperature sensor, which appears in various locations including the abstract, main text, and Table II, should be 33 samples/s instead of 333 samples/s.

The authors would like to thank K. A. A. Makinwa of Delft University of Technology, The Netherlands, for spotting this error.

References

[1] M. K. Law, A. Bermak, and H. C. Luong, "A sub-μW embedded CMOS temperature sensor for RFID food monitoring application," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1246–1255, Jun. 2010.

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Correction to "Distributed Parametric Resonator: A Passive CMOS Frequency Divider"

Wooram Lee and Ehsan Afshari

In the above paper [1, p. 1834], at the end of the abstract, the following sentences were printed incorrectly:

The output phase noise is almost 6 dB lower than that of the input signal for all offset frequencies up to 1 MHz. There is a good agreement among analysis, simulation, and 10-MHz measurement results.

This is corrected to:

The output phase noise is almost 6 dB lower than that of the input signal for all offset frequencies up to 10 MHz. There is a good agreement among analysis, simulation, and measurement results.

References

[1] W. Lee and E. Afshari, "Distributed parametric resonator: A passive CMOS frequency divider," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1834–1844, Sep. 2010.

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