Correspondence

Addition to "A Wideband 2.4-GHz Delta-Sigma Fractional-N PLL With 1-Mb/s In-Loop Modulation"

Sudhakar Pamarti, *Member, IEEE*, Lars Jansson, *Member, IEEE*, and Ian Galton, *Member, IEEE*

A technique was presented in [1] that is similar to that presented in the above paper [2]. It was published shortly before the above paper went to press, and therefore should have been included as a reference in the above paper.

References

[1] I. Bietti, E. Ternporitil, G. Albasini, and R. Castello, "An UMTS sigma delta fractional synthesizer with 200 kHz bandwidth and -128 dBc/Hz at 1 MHz using spurs compensation and linearization techniques," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2003, pp. 463–466.

[2] S. Pamarti, L. Jansson, and I. Galton, "A wideband 2.4-GHz delta-sigma fractional-N PLL with 1-Mb/s in-loop modulation," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 49–62, Jan. 2004.

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S. Pamarti is with the Department of Electrical Engineering, University of California, Los Angeles, CA 90095 USA (e-mail: spamarti@gmail.com).

L. Jansson is with Silicon Wave, Inc., San Diego, CA 92122 USA.

I. Galton is with the Department of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA 92092 USA (e-mail: galton@ece.ucsd.edu).

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Correction to "A 40-Gb/s Clock and Data Recovery Circuit in 0.18-μm CMOS Technology"

Jri Lee, *Member, IEEE,* and Behzad Razavi, *Fellow, IEEE*

The first author of [1] has indicated that the topologies shown in Fig. 4 of the above paper [2] are the same as those described in [1], [3], and [4]. He has also stated that the means of detection of the direction of the wave described on page 2184 of [2] is the same as that in [4]. We regret the unintentional omission of these references.

References

[1] J. Wood, T. C. Edwards, and S. Lipa, "Rotary traveling-wave oscillator arrays: A new clock technology," *IEEE J. Solid-State Circuits*, vol. 36, no. 11, pp. 1654–1665, Nov. 2001.

[2] J. Lee and B. Razavi, "A 40-Gb/s clock and data recovery circuit in 0.18-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2181–2190, Dec. 2003.

[3] J. Wood, " Electronic circuitry," U.S. Patent 6,556,089 B2, Apr. 29, 2003.

[4] ——, International Patent Application Number PCT/GB01/02069, May 11, 2001.

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J. Lee is with the National Taiwan University, Taipei, Taiwan 106, R.O.C.

B. Razavi is with the Electrical Engineering Department, University of California, Los Angeles, CA 90095 USA (e-mail: razavi@ee.ucla.edu).

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