Correspondence

Addition to "Evaluation of Three 32-Bit CMOS Adders in DCVS Logic for Self-Timed Circuits"

G. A. Ruiz

A reader has correctly pointed out that prior publications should have been referenced in the above paper.[1] The author was not aware of previous publications that define the complementary carry signal, N_i [1], [2].

References

[1] B. Gilchrist, J. H. Pomerene, and S. Y. Wong, "Fast carry logic for digital computers," *IRE Trans. Electronic Computers*, vol. EC-4, pp. 133–136, Dec. 1955.

[2] K. Hwang, *Computer Arithmetic Principles, Architecture, and Design*. New York, NY: Wiley, 1979, pp. 77–78.

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[1]*IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 604–613, Apr. 1998.

Correction to "High-Q HF Microelectromechanical Filters"

Frank D. Bannon III, John R. Clark, and Clark T.-C. Nguyen

In the above paper,[1] (21) on page 516 should read

$$\eta_c = \sqrt{\frac{k_r(y = l_c)}{k_{re}}}.$$

In addition, (39) on page 523 should read

$$P_{i,\,fltr} = \left(\frac{2\,(R_{Qi} + R_x)}{(R_x + R_p)}\right) P_{i,\,res}.$$

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[1]*IEEE J. Solid-State Circuits*, vol. 35, pp. 512–526, Apr. 2000.