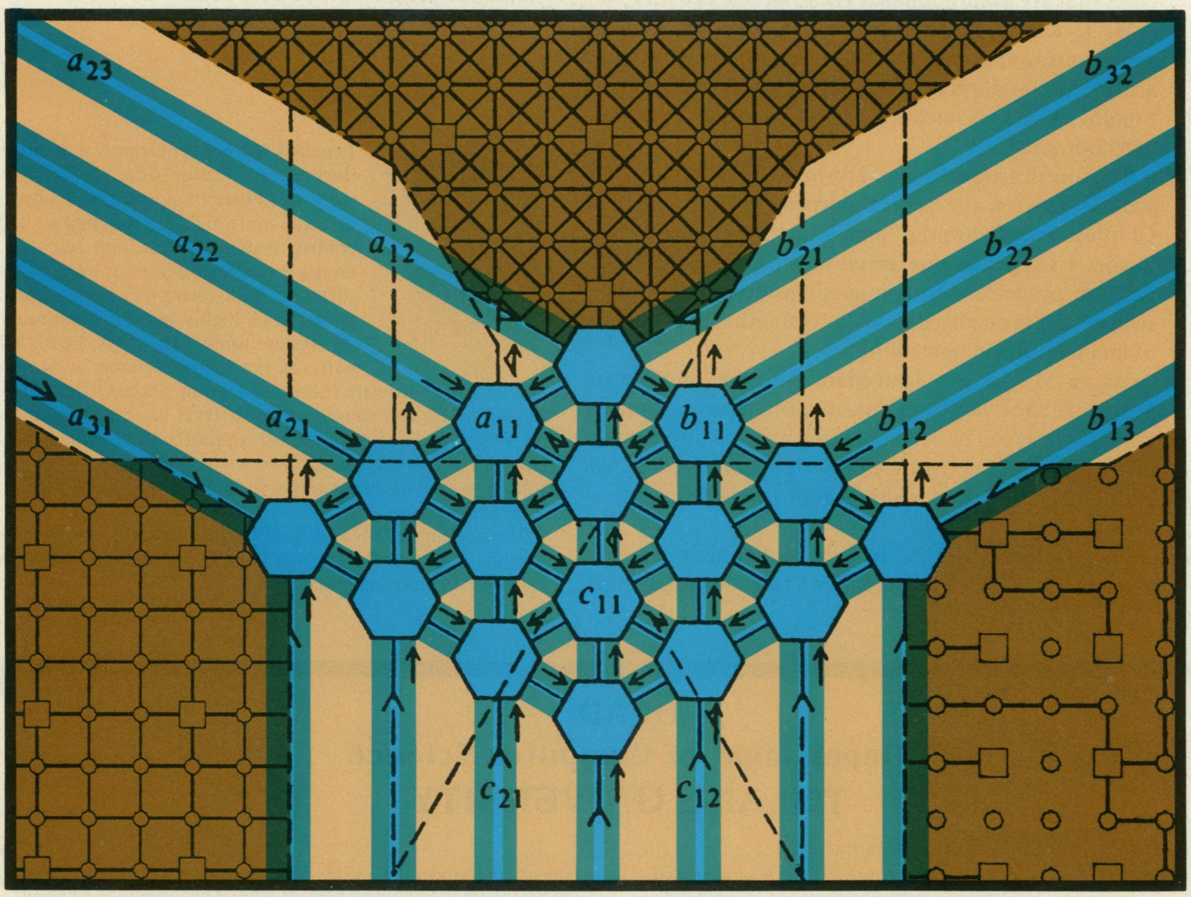
Highly Parallel Computing



Guest Editor's Introduction

Leonard S. Haynes
Federal Aviation Administration

This issue of *Computer* presents promising new techniques for using very large numbers of computing elements to solve important problems. In many areas of computer application, such as meteorology, cryptography, image processing, and sonar and radar surveillance, the quality of the answer the computer returns is proportional to the amount of computation performed. Despite the impressive speed of many recent computers, their architecture limits them to a mostly serial approach to computation, and therefore limits their usefulness for these computationally intensive problems.

Advances in the design and fabrication of VLSI circuits will soon make it feasible to implement computers consisting of tens or even hundreds of thousands of computing elements. Synergistic advances in numerical analysis and software engineering have made it possible for these highly parallel computing elements to work *cooperatively* on the solution of a single problem. Highly parallel structures can be either general or special purpose. Either way, they promise tremendous speed improvements over the fastest conventional machines. Solutions to problems that were computationally intractable only a few years ago now fall within the bounds of this new technology.

The six articles in this special issue of *Computer* examine some of the important recent developments in

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highly parallel computing. The first, by Richard Lau, Daniel Siewiorek, David Mizell, and myself, presents a survey of the field. In it, we describe classes of highly parallel machines, interconnection structures, software development, and several application examples.

The second article, by Allan Gottlieb and Jack Schwartz, describes the ultracomputer—a computer constructed from large numbers of standard microprocessor chips that are tightly coupled via a suitable network.

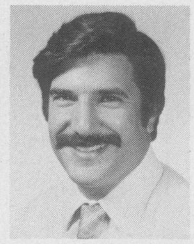
H. T. Kung's article discusses the advantages of the systolic array approach to parallel computing. In systolic arrays, special-purpose processors are connected in fixed topologies such as linear, mesh, and hexagonal nearest-neighbor arrays.

The fourth article, by Larry Snyder, looks at the middle ground between the general-purpose ultracomputer of Gottlieb and Schwartz, and Kung's systolic arrays. Snyder's Chip machine employs an array of general-purpose processors with interconnections that can be switched from one fixed topology to another by the action of an independent control function.

Hasan M. Ahmed, Jean-Marc Delosme, and Martin Morf then show how superior solutions to several important problems can be achieved using highly parallel arrays of elements that compute Cordic functions rather than addition, subtraction, multiplication, and division functions.

Finally, the sixth article, by Douglas Fairbairn, presents a summary of those advances in VLSI technology that make highly parallel computation feasible, both for general-purpose and for special-purpose applications.

These articles describe the infancy of a new technology that goes far beyond a new architecture or a new algorithm. It is, in fact, a new science, born of the creative union of numerical analysis, VLSI designers, software engineers, and application area specialists. Maturity will provide valuable solutions to today's problems, and help realize our dreams for tomorrow. ■



Leonard Haynes is currently a member of the Federal Aviation Administration team working toward implementing a more reliable and more highly automated air traffic control system. His current research interests include the design of hardware and software fault-tolerant systems, and application of highly parallel computing to AI. Before joining the FAA, he managed parts of the software research program, and later the hardware research program, at the Office of Naval Research. He has taught graduate-level courses on computer hardware- and software-related topics for the Evening College Division of Johns Hopkins University, and has served as a consultant to several companies in these areas. He is also the holder of seven patents.

Haynes earned BS and PhD degrees from the University of Maryland, and an MS degree from the University of Pennsylvania, all in electrical engineering.