A Tunnel Diode Body Contact Structure for High-Performance SOI MOSFETs

Jiexin Luo, Jing Chen, *Member, IEEE*, Qingqing Wu, Zhan Chai, Jianhua Zhou, Tao Yu, Yaojun Dong, Le Li, Wei Liu, Chao Qiu, and Xi Wang

***Abstract*—A tunnel diode body contact (TDBC) silicon-on-insulator (SOI) MOSFET structure without floating-body effects (FBEs) is proposed and successfully demonstrated. The key idea of the proposed structure is that a tunnel diode is embedded in the source region, so that the accumulated carriers can be released through tunneling. In an n-MOSFET, a heavily doped p$^+$ layer is introduced beneath the n$^+$ source region. The simulated and measured results show the suppressed FBE, as expected. Other phenomena that originate from the FBEs, such as the kink, linear kink effect, abnormal subthreshold swing, and small drain-to-source breakdown voltage in the properties, were also sufficiently suppressed. In addition, it should be noted that the proposed SOI MOSFETs are fully laid out and process compatible with SOI CMOS. Hysteresis effects disappear in TDBC SOI MOSFETs, which makes them attractive for digital applications. On the other hand, in analog applications, TDBC SOI MOSFETs are shown to hold the advantage over floating-body SOI MOSFETs due to their higher G_m/I_D ratio. TDBC SOI MOSFETs can be considered as one of the promising candidates for digital and analog devices.**

***Index Terms*—Body contact, floating-body effects (FBEs), kink effect, linear kink effect (LKE), partially depleted (PD) silicon-on-insulator (SOI), SOI MOSFETs, tunnel diode, tunnel diode body contact (TDBC).**

Manuscript received July 25, 2011; revised September 7, 2011 and October 12, 2011; accepted October 14, 2011. Date of publication November 18, 2011; date of current version December 23, 2011. The review of this paper was arranged by Editor Y. Momiyama.

J. Luo and Q. Wu are with the State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China, and also with the Graduate University of Chinese Academy of Sciences, Beijing 100049, China (e-mail: jxluo@mail.sim.ac.cn).

J. Chen, Z. Chai, and X. Wang are with the State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China (e-mail: jchen@mail.sim.ac.cn).

J. Zhou and C. Qiu are with the State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China, and with the Graduate University of Chinese Academy of Sciences, Beijing 100049, China, and also with Grace Semiconductor Manufacturing Corporation, Shanghai 201203, China.

T. Yu and Y. Dong are with the State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China, and also with the Department of Physics, The Key Laboratory of Thin Films of Jiangsu, Soochow University, Suzhou 215006, China.

L. Li and W. Liu are with Grace Semiconductor Manufacturing Corporation, Shanghai 201203, China.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2011.2173201

I. Introduction

IMPROVED frequency performance through reduced capacitance, higher drive current, and a reduction in interconnect length are significant advantages of using a silicon-on-insulator (SOI) for analog applications. Noise and latch-up are minimized through reduced substrate coupling [1]. However, the main concern is the floating-body effects (FBEs) in partially depleted (PD) SOI MOSFETs caused by impact ionization, which is known as the kink effect [2]. With the shrinking of the gate oxide, the linear kink effect (LKE) due to the direct tunneling mechanism appears in PD SOI MOSFETs [3]. Correspondingly, the body potential instability, an abnormal subthreshold swing, and a small drain-to-source breakdown voltage (BVdss) caused by FBEs are the most serious problems that are required to be solved [4].

Kink-free operation of SOI MOSFETs with a floating-body (FB) is generally desirable for analog circuits. Several approaches have been proposed to suppress the FBE, but each method has some limitations. The most commonly used method is the body contact (such as the T-gate [5], I-gate [6], and body-contacted SOI [7], [8]) scheme, which suffers from the area penalty. Moreover, its efficiency of hole absorption rapidly decreases as the channel width increases in the T-gate SOI MOSFET. Body-tied-to-source structures supply the path for the generated holes to escape to the contact, and it is subject to the lowering of effective device width [9]. The other approach is based on source engineering, including using implantation to introduce recombination centers for the holes [10], SiGe source structures [11], SiGe-inserted SOI structures [12], and BESS (bipolar embedded source structure) structures [13]. These methods increase the fabrication process complexity and are not fully compatible with SOI CMOS technology. In addition, there is a tradeoff between improving the FBEs and increasing the junction leakage current in Ar-ion implantation. Because Ge doping is inactive to alter the conduction band energy [14], the SiGe source structure is not applicable to the p-channel MOSFET.

This paper proposes a possible solution that can suppress the FBEs in PD SOI MOSFET by means of a new type of source engineering, which is referred to as the tunnel diode body contact (TDBC) SOI MOSFET. The experimental results show that this structure efficiently suppresses the FBEs. The TDBC SOI MOSFET takes up the same area as the conventional FB SOI MOSFET and less area than a transistor using other body contact schemes. The layout pattern and the process steps are completely compatible with SOI CMOS technology.

0018-9383/$26.00 © 2011 IEEE

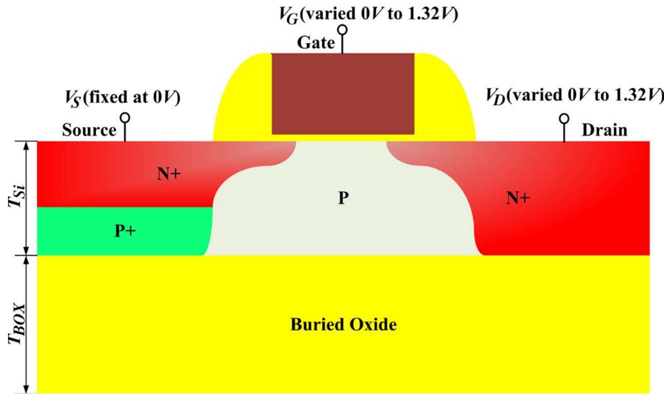

Fig. 1. Device structure of the novel TDBC SOI n-MOSFET.

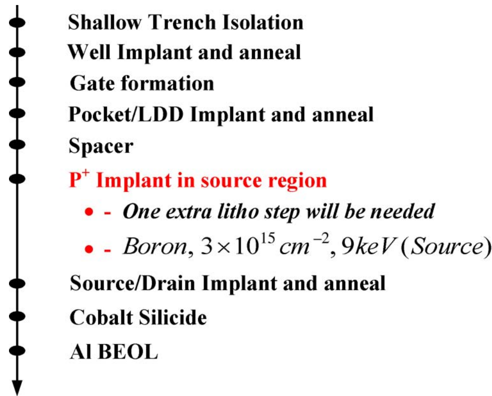

Fig. 2. Process flow of the novel TDBC SOI n-MOSFET.

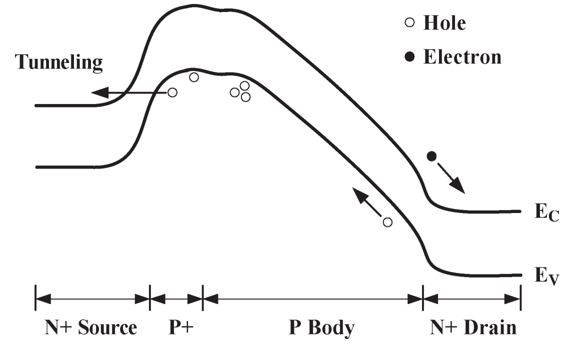

Fig. 3. Band diagram for the n^+ source/p^+/p-body/n^+ drain structure.

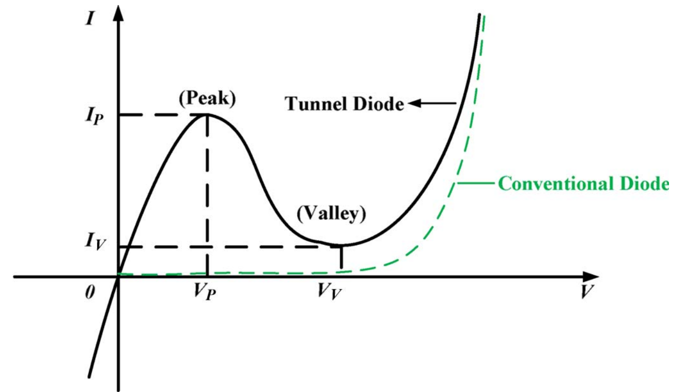

Fig. 4. Static current–voltage characteristics of a typical tunnel diode.

II. Device Concept

A. Device Structure and Fabrication

Fig. 1 shows the device structure of the novel TDBC SOI n-MOSFET. Instead of an n^+ source as in a conventional FB SOI MOSFET, an Esaki tunnel diode [15] is embedded in the source region, adjacent to the SOI/buried oxide interface. The TDBC SOI MOSFETs with a partially depleted substrate are fabricated in 0.13-μm SOI CMOS technology using shallow trench isolation (STI) and $CoSi_2$ silicide. The layer thickness is 0.1 μm for the top silicon film ($T_{\rm Si}$) and 0.145 μm for the buried oxide ($T_{\rm BOX}$). The gate oxide has a thickness of 1.8 nm ($T_{\rm OX}$). After gate patterning, the source/drain was formed by As/P ion implantation and activation. Then, the p^+ region was formed by B^+ implantation only into the source region with a protection of the drain and the gate. The process flow of the TDBC SOI n-MOSFET fabrication is shown in Fig. 2.

B. Principle of Device Operation

In TDBC SOI n-MOSFETs, a tunnel diode is formed in the source region to enhance hole flow to the source. Fig. 3 shows the band diagram for the n^+ source/p^+/p-body/n^+ drain structure. The recombination current dominates the total current of conventional diodes at low forward bias. However, the recombination current is small at low forward bias (see Fig. 4). As shown in Fig. 4, the current first increases to a maximum value (peak current or I_P) at a peak voltage V_P in the forward direction of the tunnel diode [16]. The total current of the tunnel diode is dominated by the band-to-band tunneling current at low forward bias, which is much larger than the recombination current in conventional diodes. Therefore, the holes caused by the FBE flow to the p^+ region are efficiently released by Esaki tunneling. Both p^+ and n^+ sides in the tunnel diode were degenerate, where the Fermi levels were set inside the valence band of the p^+ region or the conduction band of the n^+ source [17]. To obtain a heavily doped p-n junction in the source region, one extra mask for the p^+-type diffusion region in the TDBC SOI n-MOSFET is required. The extra process step is a p^+-type implantation with the doping peak at 1×10^{20} cm^{-3}, which can be carried out after the spacer and before the source/drain implantation (see Fig. 2).

III. Simulation Results

A. Process Simulation

Process simulations are performed using the Sentaurus process simulator Sprocess [18]. In process simulation, we use Advanced Calibration of the Sentaurus process. Many model equations and model parameters are taken from reliable publications. In addition, a rigorous calibration has been performed by Synopsys based on a SIMS database.

The dose of 3×10^{15} cm^{-2} at energy of 9 keV is selected for boron implantation in the source region. In the process flow, the source/drain implantation is realized by a two-step phosphorus implantation. To embed the p^+ layer in the n-source region adjacent to the SOI/buried oxide interface, the low dose of

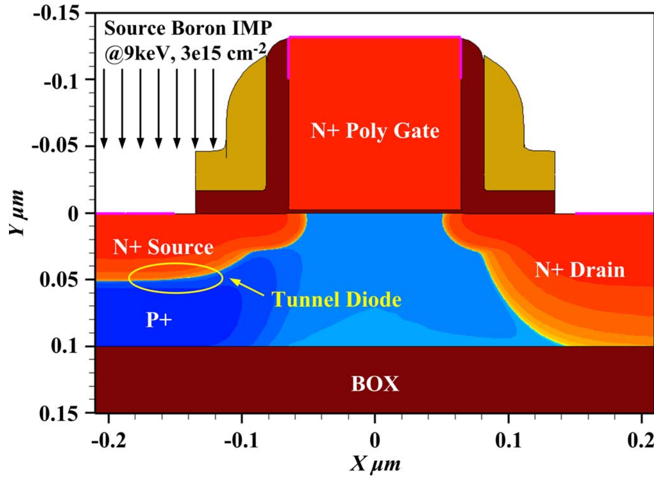

Fig. 5. Two-dimensional simulated doping profile of the TDBC SOI n-MOSFET.

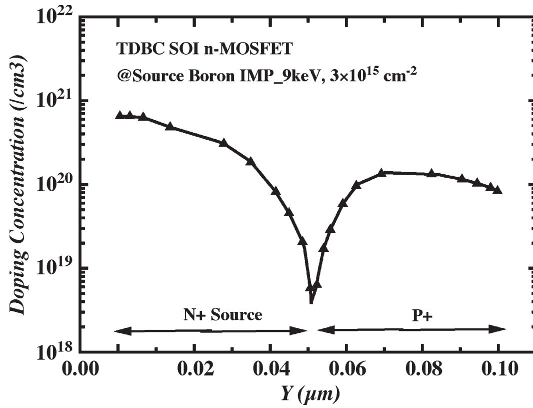

Fig. 6. Two-dimensional simulated doping profile of the TDBC SOI n-MOSFET ($X = -0.2\ \mu$m).

7×10^{13} cm^{-2} at energy of 30 keV is selected for the deep phosphorus implantation in the source/drain region. To form the sharp n$^+$/p$^+$ junction, the high dose of 3×10^{15} cm^{-2} at energy of 4 keV is selected for the shallow phosphorus implantation in the source/drain region. Then, rapid thermal process annealing at 1030 °C for 5 s was performed. The 2-D process simulations with a gate length of 0.13 μm are shown in Fig. 5.

The vertical profile of $X = -0.2\ \mu$m is shown in Fig. 6. The doping peak of 1×10^{20} cm^{-3} is obtained in the p$^+$ region. The Fermi levels are set inside the valence band or the conduction band, which is predicted by technology computer-aided design (TCAD) simulation in Fig. 7. TCAD predicted that the tunnel diode is successfully embedded in the source region.

B. Device Simulation

A 2-D device simulator based on the drift–diffusion model, which is the physical device model in Sentaurus [18], includes effects such as mobility (doping dependence and high-field saturation effects), Shockley–Hall–Read and Auger recombination, as well as avalanche generation. With continued scaling into the deep submicrometer regime, neither internal nor external characteristics of state-of-the-art semiconductor devices

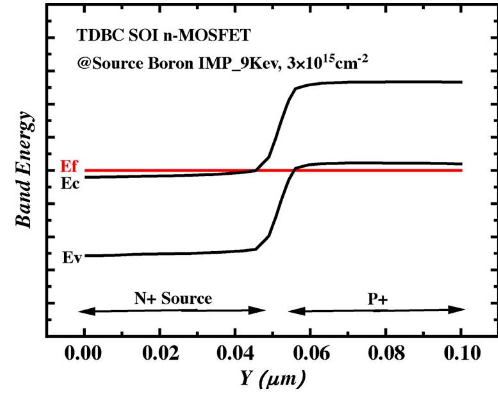

Fig. 7. TCAD predicted the band energy of the TDBC SOI n-MOSFET in the condition of thermal equilibrium. The Fermi levels were set inside the valence band of the p$^+$ region and the conduction band of the n$^+$ source.

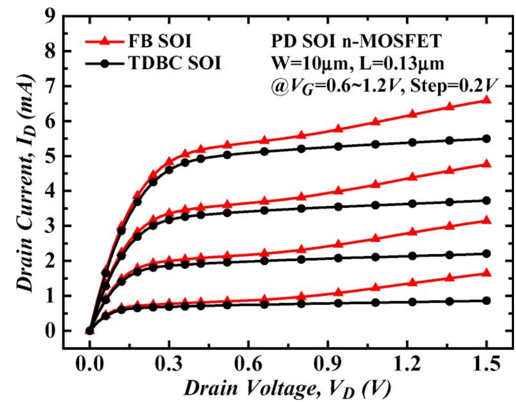

Fig. 8. TCAD predicted the output characteristics of the proposed TDBC and conventional FB SOI n-MOSFETs with a gate length of 0.13 μm. Kinks are observed in the conventional FB SOI n-MOSFET and suppressed in the proposed TDBC device.

can be properly described using the conventional drift–diffusion transport model; therefore, the hydrodynamic (or energy balance) model is used. The operation of the TDBC SOI MOSFET is based on the principle of band-to-band tunneling. It is important to point out that the Hurkx model is selected to simulate the band-to-band tunneling current [19]. As shown in Fig. 8, kink effects are observed in the conventional FB SOI n-MOSFET and suppressed in the TDBC SOI n-MOSFET. As shown in Fig. 9, the simulation results predicted that the TDBC technique is applicable for the p-channel MOSFET.

IV. Experimental Results and Discussion

The TDBC SOI MOSFETs with a partially depleted substrate are fabricated in 0.13-μm SOI CMOS technology using STI and $CoSi_2$ silicide. FB devices and T-gate body contact (TB) MOSFETs were fabricated as references. Fig. 10 shows a cross-sectional transmission electron microscopy (TEM) image of the fabricated TDBC SOI n-MOSFET structure with a gate length of 0.13 μm. All devices were measured using an Agilent B1500A semiconductor parameter analyzer, keeping the source of the transistor grounded.

Fig. 11 shows the measured transfer characteristics of the TDBC and conventional FB SOI n-MOSFETs with a gate

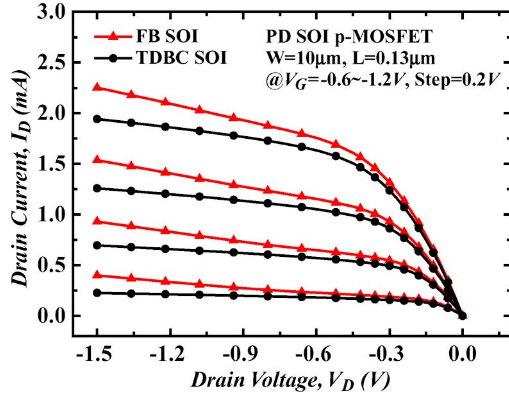

Fig. 9. TCAD predicted the output characteristics of the proposed TDBC and conventional FB SOI p-MOSFETs with a gate length of 0.13 μm. Kinks are observed in the conventional FB SOI p-MOSFET and suppressed in the proposed TDBC device.

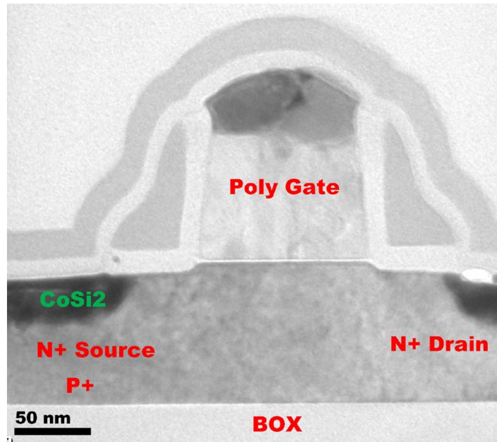

Fig. 10. Cross-sectional TEM image of a fabricated TDBC SOI n-MOSFET structure with a 0.13-μm gate length.

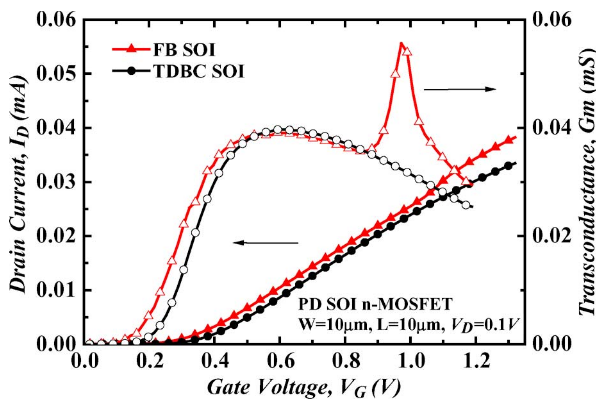

Fig. 11. Measured transfer characteristics and transconductance of the TDBC and FB SOI n-MOSFETs. The LKE is observed in the FB SOI n-MOSFET and suppressed in the TDBC SOI n-MOSFET.

length of 10 μm at $V_D = 0.1$ V. The LKE, which is indicated by the sharp transconductance peak, is observed in the conventional FB SOI n-MOSFET, whereas it is completely suppressed in the TDBC device. As shown in Fig. 11, there is no mobility degradation in the TDBC SOI MOSFET, as compared with the introduction of lifetime killers such as neutron irradiation in [20].

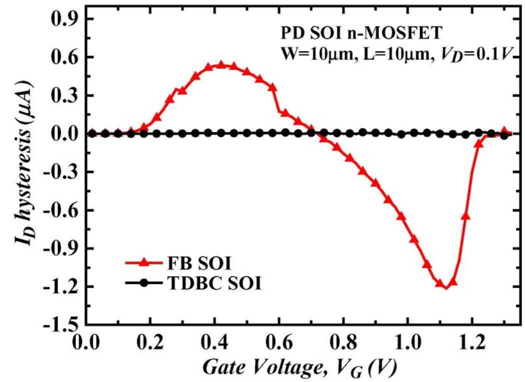

Fig. 12. Measured hysteresis on input characteristics of the TDBC and conventional FB SOI n-MOSFETs. The hysteresis effect is observed in the FB SOI n-MOSFET and suppressed in the TDBC SOI n-MOSFET.

The hysteresis effect was observed in the FB PD SOI n-MOSFET, which is related to the FBE. To investigate the hysteresis characteristics of the drain current in greater detail, the following definition is adopted for I_D hysteresis:

$$I_D \text{ hysteresis} = I_D + (V_D \text{ forward sweep}) \\ - I_D - (V_D \text{ reverse sweep})$$

Fig. 12 shows the I_D hysteresis on the input characteristics of the TDBC and conventional FB PD SOI n-MOSFETs. A positive peak at low V_G and a negative peak at high V_G can be clearly observed in the conventional FB SOI n-MOSFET. The body potential varies due to the surplus or the shortage of holes in the body region arising from the expulsion and the restoration of holes due to the growth and the contraction of the channel depletion layer [21], which results in the positive peak. The negative results from the body potential variation are related to the LKE. The hysteresis phenomenon disappears in the TDBC SOI n-MOSFET owing to the suppression of the FBE.

The subthreshold characteristics are compared in Fig. 13 for the TDBC and conventional FB SOI n-MOSFETs with a gate length of 0.13 μm. An abnormal subthreshold swing, which typically appears in the conventional FB SOI n-MOSFET, is suppressed by the TDBC SOI n-MOSFET. The drain-induced barrier-lowering (DIBL) properties, which are drastically affected by the FBE [22], are remarkably improved in the TDBC SOI MOSFET. The DIBL value, which is measured at a constant drain current of 0.1 $\mu\text{A} \times W/L$, amounts to 49 mV/V for the TDBC SOI n-MOSFET and 92 mV/V for the conventional FB SOI MOSFET. The $I_{\text{ON}}/I_{\text{OFF}}$ ratio is compared in Fig. 14 for the TDBC and conventional FB n-MOSFETs. The $I_{\text{ON}}/I_{\text{OFF}}$ ratio of 10^7 is realized in the TDBC n-MOSFET with a 0.13-μm gate length, and it has improved by two orders of magnitude compared with the FB n-MOSFET.

The measured output characteristics for the TDBC and conventional FB SOI n-MOSFETs are shown in Fig. 15. Kink phenomena appear in the conventional FB SOI n-MOSFET at drain voltages of ≥ 0.6 V due to the hole accumulation in the p-body. These holes are caused by the impact ionization at high drain fields. The hole accumulation raises the body potential and further reduces the threshold voltage, resulting in the increase in the drain current. No kink phenomena in

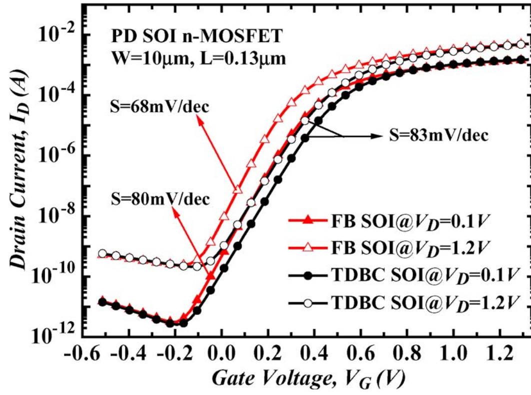

Fig. 13. Measured subthreshold characteristics in the TDBC and conventional FB SOI n-MOSFETs with a 0.13-μm gate length.

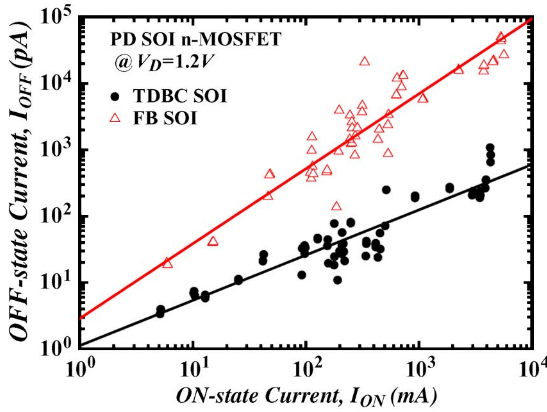

Fig. 14. Measured $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ characteristics of the TDBC and conventional FB SOI n-MOSFETs. The $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio of 10^7 is realized in the TDBC n-MOSFET with a 0.13-μm gate length, and it has improved by two orders of magnitude compared with the FB n-MOSFET.

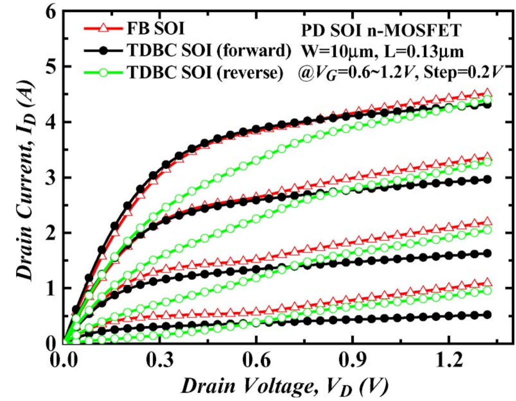

Fig. 15. Measured output characteristics of the TDBC and conventional FB SOI n-MOSFETs with a gate length of 0.13 μm. Kinks are observed in the conventional FB SOI n-MOSFET and suppressed in the TDBC device.

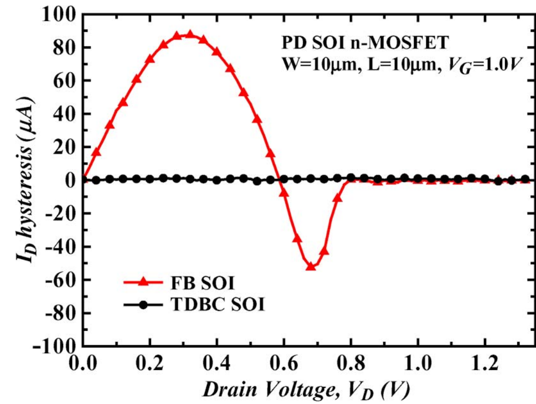

Fig. 16. Measured hysteresis on output characteristics of the TDBC and conventional FB SOI n-MOSFETs. The hysteresis effect is observed in the FB SOI n-MOSFET and suppressed in the TDBC SOI n-MOSFET.

the TDBC SOI n-MOSFET were observed. We can conclude that TDBC SOI technology can fully suppress the FBE. The suppression of the FBE makes the TDBC device suitable for analog applications. In addition, the hysteresis effect on output characteristics is suppressed by the TDBC SOI n-MOSFET (see Fig. 16). It is critical for digital applications. Because the TDBC SOI n-MOSFET is an asymmetrical FET, as shown in Fig. 15, the kink effect appears in the reversed I_d–V_d characteristics (reverse source and drain).

In practical analog applications of the PD SOI MOSFET, noise and mismatching increase in the kink regime [23]. The kink effect makes PD SOI devices unsuitable for analog applications. TDBC MOSFETs provide an obvious solution owing to the suppression of the FBE. The transistor is in strong inversion with G_m/I_D around 10 V^{-1} at the gate voltage overdrive $(\mathrm{VGO} = V_G - V_{\mathrm{TH}})$ of 0.2 V, which results in a good compromise between speed and power consumption [24], [25]. Thus, we perform the comparison for device bias at VGO $=$ 0.2 V. To assess the analog performance, transconductance G_m is plotted in Fig. 17 versus normalized drain current on a linear scale. As shown in Fig. 17, the G_m/I_D ratio of the TDBC SOI n-MOSFET is $\sim$10% higher than that of the FB SOI n-MOSFET at VGO $=$ 0.2 V. It is shown that the conventional FB SOI MOSFET G_m deviates from the TDBC SOI MOSFET

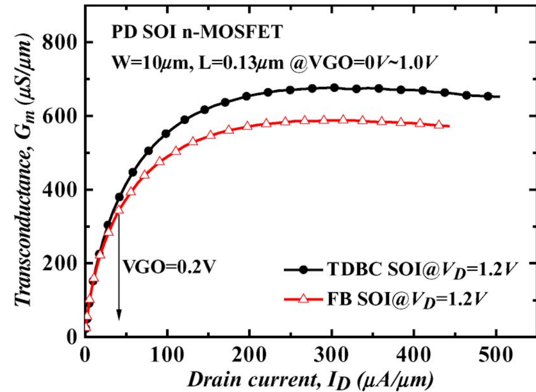

Fig. 17. Measured normalized transconductance (G_m/W) versus normalized drain current (I_D/W) for $V_{DS} = 1.2$ V and increasing gate voltage overdrive, VGO. The G_m of the conventional FB SOI MOSFET degrades at high gate overdrive compared with that of the TDBC SOI MOSFET.

at VGO $>$ 0.2 V. This increase in the G_m/I_D ratio provides improvement of the voltage gain (G_m/G_{DS}) in the TDBC SOI MOSFET. This represents a big advantage over the FB device for analog circuit performance.

In the high-speed digital applications, cutoff frequency f_T is an interesting criterion, which corresponds to the transit frequency of the current gain. Using a conventional MOSFET

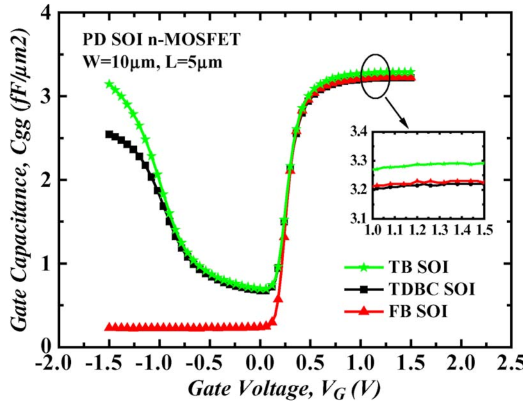

Fig. 18. Measured gate capacitance characteristics of the TDBC, conventional TB, and FB SOI n-MOSFETs.

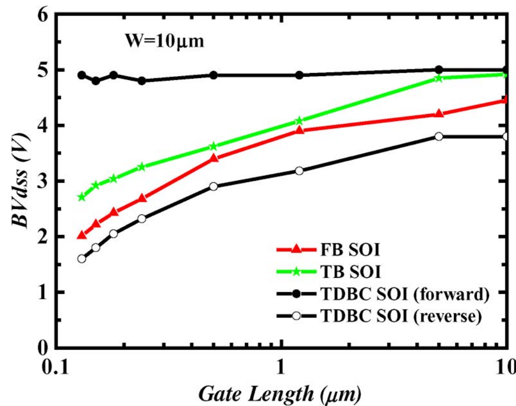

Fig. 19. Measured drain-to-source breakdown voltages BVdss of the TDBC, conventional TB, and FB SOI n-MOSFETs at $V_G = 0$ V.

equivalent circuit and taking into account some simplifications, we can express f_T as follows [24]:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

where C_{gs} is the gate-to-source capacitance, and C_{gd} is the gate-to-drain capacitance. The gate capacitance measurement is carried out on the TDBC and conventional FB/TB SOI n-MOSFETs. The results are shown in Fig. 18. When $V_G =$ 1.2 V, the gate capacitance of the TDBC SOI n-MOSFET is equal to that of the FB SOI n-MOSFET. The results indicated that the n^+/p^+ junction does not increase the capacitance. Moreover, it is clearly shown that the TDBC SOI n-MOSFET is more attractive than the TB SOI n-MOSFET for high-frequency applications.

Fig. 19 shows the measured BVdss as a function of the gate length for the TDBC and conventional FB/TB SOI n-MOSFETs, where BVdss is defined as the drain voltage at a drain current of 1 μA/μm without gate bias, $V_G = 0$ V. The reduction of BVdss for the conventional FB SOI n-MOSFET could be subjected to the parasitic bipolar junction transistor effect [26]. The BVdss of the TB SOI n-MOSFET decreases with decreasing gate length. It is verified that the efficiency of hole absorption rapidly decreases due to the body resistance in the TB SOI n-MOSFET. However, the TDBC SOI n-MOSFET dramatically improved the BVdss characteristics in forward mode, showing no gate length dependence. The reverse current of the tunnel diode rapidly increases with reverse voltage, which results in the lowering of the source-to-drain breakdown voltage.

V. Conclusion

We have proposed a novel structure with a tunnel diode embedded at the source to suppress FBEs in the PD SOI, which we refer to as the TDBC SOI. It is successfully fabricated by 0.13-μm SOI CMOS technology. The LKE is well suppressed, and the abnormal subthreshold swing disappeared in the TDBC SOI MOSFET. In addition, it has a remarkably improved DIBL feature. The accumulated carriers due to impact ionization are successfully released in the TDBC SOI MOSFET. Correspondingly, kink-free operation of the TDBC SOI MOSFET is obtained. Moreover, it shows a dramatically increased drain breakdown voltage. A significant advantage is that the fabrication process is fully compatible with SOI CMOS technology.

The hysteresis effect disappears in TDBC SOI MOSFETs owing to the suppression of FBEs. The I_{ON}/I_{OFF} ratio of 10^7 is realized in TDBC SOI MOSFETs with a 0.13-μm gate length, and it has improved by two orders of magnitude compared with FB SOI MOSFETs. All this makes TDBC SOI MOSFETs attractive for digital applications. TDBC SOI MOSFETs are shown to exhibit outstanding properties for analog applications, well superior to comparable conventional FB SOI MOSFETs. An increase of G_m/I_D ratio by at least of 10% was found for a wide range of gate voltage overdrive. In all, our work provides a possible way for using SOI technology in digital and analog applications.

Acknowledgment

The authors would like to thank the Process Engineers at Grace Semiconductor Manufacture Corporation for their help and Dr. Q. T. Zhao at PGI 9 of Forschungszentrum Jülich for the valuable discussions.

References

[1] S. N. Andrew Marshall, *SOI Design: Analog, Memory and Digital Techniques*. Boston, MA: Kluwer, 2003.

[2] J. P. Colinge, *Silicon-on-Insulator: Materials to VLSI*, 3rd ed. Boston, MA: Kluwer, 2004.

[3] A. Mercha, J. M. Rafi, E. Simoen, E. Augendre, and C. Claeys, "“Linear kink effect” induced by electron valence band tunneling in ultrathin gate oxide bulk and SOI MOSFETS," *IEEE Trans. Electron Devices*, vol. 50, no. 7, pp. 1675–1682, Jul. 2003.

[4] S. Dongwook and J. G. Fossum, "A physical charge-based model for non-fully depleted SOI MOSFETs and its use in assessing floating-body effects in SOI CMOS circuits," *IEEE Trans. Electron Devices*, vol. 42, no. 4, pp. 728–737, Apr. 1995.

[5] B. W. Min, L. Kang, D. Wu, D. Caffo, J. Hayden, and M. A. Mendicino, "Reduction of hysteretic propagation delay with less performance degradation by novel body contact in PD SOI application," in *Proc. IEEE Int. SOI Conf.*, 2002, pp. 169–170.

[6] C.-H. Wu, C. Yu, H. Shichijo, and K. O. Kenneth, "I-gate body-tied silicon-on-insulator MOSFETs with improved high-frequency performance," *IEEE Electron Device Lett*, vol. 32, no. 4, pp. 443–445, Apr. 2011.

[7] Y.-H. Koh, J.-H. Choi, M.-H. Nam, and J.-W. Yang, "Body-contacted SOI MOSFET structure with fully bulk CMOS compatible layout and process," *IEEE Electron Device Lett*, vol. 18, no. 3, pp. 102–104, Mar. 1997.

[8] Y.-H. Koh, M.-R. Oh, J.-W. Lee, J.-W. Yang, W.-C. Lee, and H.-K. Kim, "Body-contacted SOI MOSFET structure and its application to DRAM," *IEEE Trans. Electron Devices*, vol. 45, no. 5, pp. 1063–1070, May 1998.

[9] A. Daghighi, M. Osman, and M. Imam, "An area efficient body contact for low and high voltage SOI MOSFET devices," *Solid State Electron.*, vol. 52, no. 2, pp. 196–204, Feb. 2008.

[10] T. Ohno, M. Takahashi, A. Ohtaka, Y. Sakakibara, and T. Tsuchiya, "Suppression of the parasitic bipolar effect in ultra-thin-film nMOSFETs/SIMOX by Ar ion implantation into source/drain regions," in *IEDM Tech. Dig*, 1995, pp. 627–630.

[11] M. Yoshimi, M. Terauchi, A. Nishiyama, O. Arisumi, A. Murakoshi, K. Matsuzawa, N. Shigyo, S. Takeno, M. Tomita, K. Suzuki, Y. Ushiku, and H. Tango, "Suppression of the floating-body effect in SOI MOSFETs by the bandgap engineering method using a $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ source structure," *IEEE Trans. Electron Devices*, vol. 44, no. 3, pp. 423–430, Mar. 1997.

[12] G. J. Bae, T. H. Choe, S. S. Kim, H. S. Rhee, K. W. Lee, N. I. Lee, K. D. Kim, Y. K. Park, H. S. Kang, Y. W. Kim, K. Fujihara, H. K. Kang, and J. T. Moon, "A novel SiGe-inserted SOI structure for high performance PDSOI CMOSFETs," in *IEDM Tech. Dig*, 2000, pp. 667–670.

[13] M. Horiuchi and M. Tamura, "BESS: A source structure that fully suppresses the floating body effects in SOI CMOSFETs," *IEEE Trans. Electron Devices*, vol. 45, no. 5, pp. 1077–1083, May 1998.

[14] R. People, "Physics and applications of $\mathrm{Ge}_x\mathrm{Si}_{1-x}/\mathrm{Si}$ strained-layer heterostructures," *IEEE J. Quantum Electron.*, vol. QE-22, no. 9, pp. 1696–1710, Sep. 1986.

[15] L. Esaki, "New phenomenon in narrow germanium p-n junctions," *Phys Rev*, vol. 109, no. 2, pp. 603–604, Jan. 1958.

[16] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. New York: Wiley, 2007.

[17] L. Esaki, "Discovery of the tunnel diode," *IEEE Trans. Electron Devices*, vol. ED-23, no. 7, pp. 644–647, Jul. 1976.

[18] *Sentaurus Device User Guide*, Mountain View, CA: Synopsys, Inc., 2010.

[19] G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuvers, "A new recombination model for device simulation including tunneling," *IEEE Trans. Electron Devices*, vol. 39, no. 2, pp. 331–338, Feb. 1992.

[20] A. C. Ipri, G. M. Dolny, D. P. Vu, and M. W. Batty, "Suppression of parasitic bipolar effects in SOI MOSFETS by neutron irradiation," in *Proc. IEEE Int. SOI Conf.*, 1992, pp. 34–35.

[21] T. Sakurai, A. Matsuzawa, and T. Douseki, *Fully-Depleted SOI CMOS Circuits and Technology for Ultralow-Power Applications*. Berlin, Germany: Springer-Verlag, 2006.

[22] M. Horiuchi and M. Tamura, "BESS: A source structure that fully suppresses the floating body effects in SOI CMOSFETs," in *IEDM Tech. Dig*, 1996, pp. 121–124.

[23] O. Rozeau, J. Jomaah, S. Haendler, J. Boussey, and F. Balestra, "SOI technologies overview for low-power low-voltage radio-frequency applications," *Analog Integr. Circuits Signal Process.*, vol. 25, no. 2, pp. 93–114, Nov. 2000.

[24] V. Kilchytska, A. Neve, L. Vancaillie, D. Levacq, S. Adriaensen, H. van Meer, K. De Meyer, C. Raynaud, M. Dehan, J. P. Raskin, and D. Flandre, "Influence of device engineering on the analog and RF performances of SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 577–588, Mar. 2003.

[25] V. Subramanian, B. Parvais, J. Borremans, A. Mercha, D. Linten, P. Wambacq, J. Loo, M. Dehan, C. Gustin, N. Collaert, S. Kubicek, R. Lander, J. Hooker, F. Cubaynes, S. Donnay, M. Jurczak, G. Groeseneken, W. Sansen, and S. Decoutere, "Planar bulk MOSFETs versus FinFETs: An analog/RF perspective," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 3071–3079, Dec. 2006.

[26] J. Y. Choi and J. G. Fossum, "Analysis and control of floating-body bipolar effects in fully depleted submicrometer SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 38, no. 6, pp. 1384–1391, Jun. 1991.

Jiexin Luo, photograph and biography not available at the time of publication.

Jing Chen (M'03) photograph and biography not available at the time of publication.

Qingqing Wu, photograph and biography not available at the time of publication.

Zhan Chai, photograph and biography not available at the time of publication.

Jianhua Zhou, photograph and biography not available at the time of publication.

Tao Yu, photograph and biography not available at the time of publication.

Yaojun Dong, photograph and biography not available at the time of publication.

Le Li, photograph and biography not available at the time of publication.

Wei Liu, photograph and biography not available at the time of publication.

Chao Qiu, photograph and biography not available at the time of publication.

Xi Wang, photograph and biography not available at the time of publication.