Foreword
Special Issue on Characterization of Nano CMOS Variability by Simulation and Measurements

THIS Special Issue presents significant results from recent research studies on the "Characterization of Nano CMOS Variability by Simulation and Measurements." Due to the continuous scaling of the transistor dimensions and the rapid introduction of the 32-nm and 22-nm technology nodes, the variability of transistor characteristics has become a major concern associated with the further scaling and integration of CMOS. Variability already critically affects SRAM scaling and introduces leakage and timing issues in digital logic circuits. Variability is the main factor restricting scaling of the supply voltage, which for the last four technology generations has remained virtually constant and thereby has added to the power crisis. In addition to this increasing variability, the looming challenges that arise from the statistical aspects of reliability threaten to dramatically reduce the life span of integrated circuits and systems in the near future. The physical and compact modeling of variability and the statistical aspects of reliability, together with their requirements for comprehensive characterization, have been highlighted in the 2008 and 2010 updates of the International Technology Roadmap for Semiconductors and in the 2008 European Nanoelectronics Initiative Advisory Council (ENIAC) Joint Technology Initiative (JTI) Multi-annual Strategic Plan. These topics have also received particular attention in the recent European FP7 Cooperation Project named "Silicon-based nanostructures and nanodevices for long-term nanoelectronics applications" (NANOSIL FP7 IST-216171) that is cited by several papers in this Special Issue.

The simulation and characterization of variability have become extremely important in terms of understanding the current variability mechanisms and sources. They are also used for predicting the levels of variability in future technology generations involving conventional and novel nanoscale CMOS devices such as biosensors and other devices used in more than Moore applications of nanoelectronics. Many semiconductor industry stakeholders now accept that variability and statistical reliability requirements will transform the way circuits and systems are designed in the future. In addition, reliable statistical compact models based on predictive physical simulations will be critical for designing these systems.

In view of the increasing importance of this area that involves new materials, devices, circuits, modeling tools, characterization techniques, and associated international standards, the aim of this Special Issue is to bring together recent advances in the "Characterization of Nano CMOS Variability by Simulation and Measurements" and present them to the device- and design-oriented academic and industrial communities, as represented by the readers of the IEEE TRANSACTIONS ON ELECTRON DEVICES.

This Special Issue consists of 16 carefully selected papers, i.e., 5 invited papers (one of which has two parts) and 11 contributed papers, that discuss topics such as process variation, device variability, hierarchical modeling tools, and address challenges such as device mismatch and SRAM noise margin variability. The Special Issue starts with the five invited papers.

Highlights from the 5 invited papers:

1) In "Process Technology Variation," Kuhn *et al.* discuss the importance of process variation in modern CMOS transistor technology, review front-end variation sources, present device and circuit variation measurement techniques, and compare recent intrinsic transistor variation performance reported in the literature.
2) In "Quantum transport study on the Impact of Channel Length and Cross-section on Variability Induced by Random Discrete Dopants in Narrow Gate-all-around Silicon Nanowire Transistors," Martinez *et al.* review and extend recent work on the effect of random discrete dopants on the statistical variability in gate-all-around silicon nanowire transistors. The authors use the nonequilibrium Green's function formalism and full 3-D real-space and coupled-mode-space representations.
3) In "Hierarchical Simulation of Process Variations and their Impact on Circuits and Systems: Methodology (Part I) and Results (Part II)," Lorenz *et al.* discuss in Part I the sources of process variations and the state-of-the-art related simulation tools with their hierarchical structure. In Part II, they present examples of hierarchical simulation results obtained with the methodology described in Part I.
4) In "Characterization and Modeling of Transistor Variability in Advanced CMOS Technologies," Mezzomo *et al.* review their results on the characterization and modeling of transistor mismatch in advanced CMOS technologies. They begin with a review of the theoretical background and modeling approaches for analyzing and interpreting the mismatch results. Next, they discuss the experimental procedures and methodologies for characterizing transistor matching. Finally, they present typical matching results obtained on modern CMOS technologies with the main variability (mismatch) sources.
5) In "Direct Measurement of Correlation between SRAM Noise Margin and Individual Cell Transistors Variability by Using Device-Matrix-Array," Hiramoto *et al.* present direct measurements of noise margin, characteristics of

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six individual cell transistors, and their variability in SRAM cells using a special device-matrix-array test element group of 16-Kbit SRAM cells. Their results indicate that the circuit simulation with only the threshold variability taken into account will not predict SRAM stability precisely at low supply voltage.

We arranged the 11 contributed papers into two groups as follows: 1) New Model Developments and 2) Characterization and Reliability Aspects of Variability.

Group 1: New Model Developments

This group of six papers covers new model developments, including process, device, and compact models, devoted to variability.

1) In "Statistical Enhancement of the Evaluation of Combined RDD and LER-Induced V_T Variability: Lessons from 10^5 Sample Simulations," Reid *et al.*, report on the statistical threshold voltage variability in a state-of-the-art n-Channel MOSFET. They are the first to include the combined effect of random discrete dopants and line-edge roughness and demonstrate that the resulting distribution is nonnormal. They are able to analyze up to 100 000 devices by deploying computationally efficient statistical enhancement techniques.
2) In "An approach based on sensitivity analysis for the evaluation of process variability in nanoscale MOSFETs," Bonfiglio *et al.* propose an interesting approach to evaluate the effects of line-edge roughness, surface roughness, and random dopant distribution on the threshold voltage dispersion in nanoscale MOSFETs. They use parameter sensitivity analyses performed by means of a limited number of technology computer-aided design simulations or analytical modeling.
3) In "A comparative study of surface-roughness-induced variability in silicon nanowire and double-gate FETs," Pala *et al.*, present a full quantum analysis based on the 3-D self-consistent solution of the Poisson–Schrödinger equation within the nonequilibrium Green's function formalism and solved with a coupled-mode-space approach. They use this approach to calculate the effect of surface roughness at the Si/SiO2 interfaces on transport properties of quasi-1-D- and quasi-2-D-silicon nanodevices by comparing the electrical performances of nanowire and double-gate FETs.
4) In "Grain-Orientation Induced Quantum Confinement Variation in Multi-Gate Ultra-Thin Body CMOS Devices and Implications for Digital Circuit Design," Rasouli *et al.* identify a new source of random threshold voltage variation, i.e., "grain-orientation induced quantum confinement" in emerging ultrathin body metal-gate CMOS devices. These effects arise from the dependence of the work function of the metal gates on the grain orientations and cause different parts of the gate in multigate CMOS devices to feature different work-function values.
5) In "Statistical Threshold-Voltage Variability in Scaled Deca-Nanometer Bulk HKMG MOSFETs: a Fully Scaled 3D Simulation Scaling Study," Wang *et al.* present a comprehensive fully scaled 3-D simulation scaling study of the statistical threshold voltage variability in bulk high-κ/metal-gate (HKMG) MOSFETs with gate lengths down to 13 nm. They include metal-gate granularity and the corresponding work-function-induced threshold voltage variability, which have become important sources of statistical variability in bulk HKMG MOSFETs.
6) In "Compact Modeling of Variability Effects in Nanoscale NAND Flash Memories, " Spessot *et al.* present a thorough investigation of the main variability effects in nanoscale NAND Flash memory devices and consider their impact on device operation by means of a statistical compact model for the memory array.

Group 2: Characterization and Reliability Aspects of Variability

The final five papers cover several characterization and reliability aspects of variability.

1) In "Low Frequency Noise Investigation and Noise Variability Analysis in High-κ Metal Gate 32nm CMOS Transistors," Lopez *et al.* report on the low-frequency noise (LFN) of high-κ/metal stack n- and p-MOS transistors. Their results obtained on the 32-nm CMOS technology, including LFN spectra, indicate that carrier number fluctuation is the main noise source for both n- and p-MOS devices.
2) In "Investigation on Variability in Metal-Gate Si Nanowire MOSFETs: Analysis of Variation Sources and Experimental Characterization," Wang *et al.* study the characteristic variability in gate-all-around Si nanowire (NW) MOSFETs and include detailed discussions on specific sources of NW cross-sectional shape variation, random dopant fluctuation in NW source/drain extension regions, and NW line-edge roughness.
3) In "On the Variability in Planar FDSOI Technology: From MOSFETs to SRAMs," Mazurier *et al.* report a variability analysis of MOSFET threshold voltage (Vth) on static random access memory devices noise margin in fully depleted silicon-on-insulator technology and demonstrate a very low Vth variability.
4) In "A 3-D Physical Model for Vth Variations Considering the Combined Effect of NBTI and RDF," Panagopoulos *et al.* use the stochastic differential equation to investigate the combined effects of random dopant fluctuation and negative bias temperature instability due to hot carriers on Vth.
5) In "Impact of Hot Carriers on n-MOSFET variability in 45 nm and 65 nm CMOS Technologies," Magnone *et al.* examine the impact of hot carriers (HCs) on n-channel metal–oxide–semiconductor (MOS) field-effect transistor mismatch across the 45-nm and 65-nm complementary MOS technology generations. Their reported statistical analysis is based on a large overall sample population of about 1000 transistors. They find that HC stress becomes a source of variability in device electrical parameters due to the randomly generated charge traps in the gate dielectric or at the substrate/dielectric interface.

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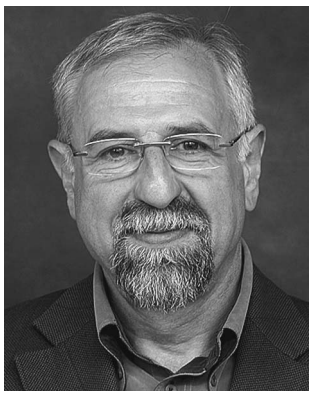
Mr. Sangiorgi is a Fellow of the IEEE, Distinguished Lecturer of the Electron Device Society, Chairman of the Electron Device Society Technology Computer-Aided Design Technical Committee. From 1994 to 2009, he was an Editor of IEEE ELECTRON DEVICE LETTERS. He has been a Guest Editor of several special issues on major scientific journals such as IEEE TRANSACTIONS ON ELECTRON DEVICES and SOLID-STATE ELECTRONICS. He has been a member of the Technical Committees of several International Conferences on Electron Devices: International Electron Devices Meeting ('91–96; '04–'06), European Solid-State Device Research Conference ('99-present), INFOS ('95-03), ULIS ('00–'08), etc. He has been involved in several European Projects of the 5, 6, and now 7 FP with management responsibilities, and he has acted as a Project Reviewer for the European Commission.



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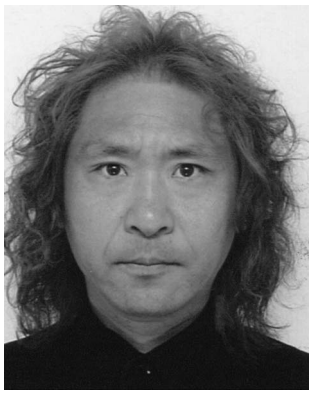

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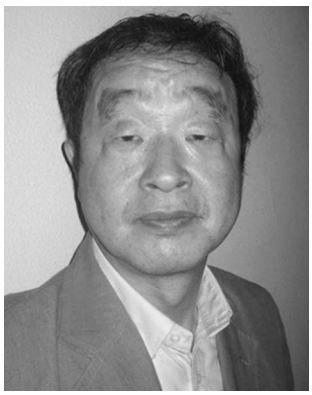

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