Guest Editorial
Special Issue on Nanowire Transistors: Modeling, Device Design, and Technology

THE RAPID development of integrated circuit technology is primarily due to MOSFET downscaling trends that have continued to the present day. However, silicon-based MOS technology is expected to face fundamental limits in the near future, and therefore, new types of nanoscale devices are being investigated aggressively. Recently, various semiconductor nanowire devices have drawn much attention because of their possible use in future electronics and optoelectronics applications. Continued MOSFET scaling has led to the study of nonplanar FET geometries that can provide better short channel control than conventional planar FETs. In particular, gate-all-around or surround gate FETs with a thin nanowire channel can provide superior electrostatic characteristics that will allow continued scaling beyond what is possible with planar technology.

Variability in these devices is also a topic of aggressive investigation. For smaller nanowire diameters, the inversion charge changes from surface inversion to bulk inversion due to quantum confinement. Variations in nanowire dimensions due to fabrication imperfections can lead to perturbations in the carrier potential and scattering that degrade the charge transport characteristics. Additionally, variations in nanowire diameters may lead to a variation in FET threshold voltage. Reducing variability is therefore a key challenge in making nanowire FETs a viable technology.

Among the different materials considered for growing nanowires, silicon has been studied extensively due to its compatibility with conventional Si CMOS technology. Si nanowires with diameters as small as one nanometer have been grown successfully. Ge nanowires are also of particular interest due to their higher carrier mobility. Nanowire-based transistors have also been demonstrated using a number of other materials, chief among these are ZnO, SnO, SiC, InP, GaN, other III–V compounds, and conducting polymers. Not only can nanowires be prepared from a diverse range of materials but also they can be integrated with very dissimilar materials. For example, Ge nanowires and even III–V nanowires have been grown on silicon substrates. Nanowires with a lattice constant different from that of the substrate can elastically accommodate the lattice mismatch and can be grown defect free. This is an opportunity that was not previously available to crystal growers. Similarly, nanowires with heterostructures along the main axis of the nanowire as well as in the radial direction have been demonstrated. Because of the diversity of materials available for fabricating nanowire transistors, the breadth of potential applications is significant and includes chemical and biological sensing, high-performance electronic circuits on glass or plastic substrates, a variety of memory types, flexible electronics, displays, nanocomputers, and atomic-scale light-emitting diodes.

Quantum confinement effects make modeling of nanowire transistors a complex problem. While there are many studies in the literature on the modeling of nanowire transistors based on nonequilibrium Green function or Monte Carlo approaches, the physics related to the operation of nanowire transistors needs to be well articulated so that simple compact models, including ballistic transport and realistic subband parameters, can be developed for circuit design using SPICE-like simulators.

Devices based on nanowires can be fabricated using a "bottom-up" approach (such as CVD or liquid-vapor-phase growth and self-assembly) or a "top-down" approach (using photolithography and etching). Most bottom-up approaches are statistical by nature and are lacking the fidelity of top-down fabrication. Yet, their integration with traditional top-down fabrication is already taking place in applications such as nonvolatile memories and in the realization of ultralow-κ dielectrics for back end of line applications. Bottom-up approaches for making nanoscale devices circumvent some of the fabrication challenges and the high cost of equipment that are associated with established top-down CMOS processing. Acquiring and maintaining such big-ticket infrastructure which is prone to becoming obsolete at a rapid rate is out of bounds to most universities and even to many corporations. Therefore, there is a great need to focus on bottom-up fabrication methods for nanowire devices since they enable a wider range of academic institutions, laboratories, and corporations to participate and contribute to the growth of nanowire electronics.

Due to the rapid development taking place in the area of nanowires, there is an immediate need to bring the potential of nanowire devices to the notice of device designers and technologists working within the confines of Si CMOS technology. The primary goal of this special issue is, therefore, to compile advances in different aspects of nanowire-based devices including device physics and modeling, device design, characterization techniques, technology, and applications so that this special issue will not only be of great archival value but also attract new researchers into this area for further accelerating the application of nanowires in building cheaper and higher performance electronic systems.

This special issue of the IEEE TRANSACTIONS ON ELECTRON DEVICES and the IEEE TRANSACTIONS ON NANOTECHNOLOGY contains both invited papers surveying

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recent developments and contributed papers reporting original results. The papers are divided between these two journals to reflect the scope of each of these journals. Many internationally renowned experts from across the world have contributed to this special issue, making it perhaps the first ever effort in putting together an invaluable collection of knowledge in the field of nanowire electronics.

The following papers will appear in the IEEE TRANSACTIONS ON NANOTECHNOLOGY:

1) *Real Time, Label Free Detection of Biological Entities Using Nanowire Based Field Effect Transistors*
2) *Chemical Sensors and Electronic Noses Based on One-Dimensional Metal Oxide Nanostructures*
3) *Characteristic Features of One-Dimensional Ballistic Transport in Nanowire MOSFETs*
4) *Highly Sensitive ZnO Nanowire Acetone Vapor Sensor with Au Adsorption*
5) *SPICE Modeling of Silicon Nanowire Field Effect Transistors for High-Speed Analog Integrated Circuits*
6) *Dual Nanowire Silicon MOSFET with Silicon Bridge and TaN Gate*
7) *Nanorods of LiF:Mg, Cu, P as Detectors for Mixed Field Radiations*
8) *Temperature Dependence of Carrier Transport of Silicon Nanowire Schottky Barrier Field Effect Transistor*
9) *Self Assembled Nanowire Arrays of Metal–Insulator–Semiconductor Diodes Exhibiting S-Type NonLinearity*
10) *Palladium Nanowires Assembly by Dielectrophoresis Investigated as Hydrogen Sensors*
11) *Enhanced Electrical Conductance of ZnO Nanowire FET by Non-destructive Surface Cleaning*
12) *Metal–Semiconductor Field Effect Transistors (MESFETs) Made From Individual GaN Nanowires*
13) *Band Effects on the Transport Characteristics of Ultra-Scaled SNW-FETs*
14) *Electrical Characteristics of Back-Gated Bottom-up Silicon Nanowire Field Effect Transistors*
15) *Hydrogen Ion Sensing Using Schottky Contacted Silicon Nanowire FETs*
16) *Bandstructure Effects in Silicon Nanowire Hole Transport*
17) *Single Palladium Nanowire Via Electrophoresis Deposition Used as Ultra Sensitive Hydrogen Sensor*
18) *Electrical Failure Analysis of Au Nanowires.*

Publishing a special issue is not an easy task due to the strict deadlines and the need for an efficient coordination among the guest editors, authors, and the reviewers. However, the Editor-in-Chief of the IEEE TRANSACTIONS ON ELECTRON DEVICES, Dr. Doug Verret played a pivotal role in bringing coherence to the diverging views and provided effective leadership in making sure this special issue became a reality. The initiative taken by the Editor-in-Chief of the IEEE TRANSACTIONS ON NANOTECHNOLOGY, Prof. Aristides Requicha in joining with the Electron Devices Society to bring out this special issue is deeply appreciated. Ms. Jo Ann Marsh of the Electron Devices Society Office received all the manuscripts and acted as an effective bridge between the guest editors, reviewers, and the authors. She was always prompt and was a pleasure to work with. We would like to thank the reviewers who have worked hard to provide prompt reviews and to make sure that the accepted papers met the high standards that our readers are used to. Finally, this special issue would not have been possible without the dedicated effort of all the guest editors. We hope that the contents will be of great interest to not only beginners in this area but also to those who are active contributors to the growth and application of nanowire electronics.

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Dr. Kumar is a Fellow of the Indian National Academy of Engineering and the Institution of Electronics and Telecommunication Engineers (IETE) India. He is an IEEE Distinguished Lecturer of the IEEE Electron Devices Society (EDS). He is also a member of the EDS Publications Committee and EDS Educational Activities Committee. He is an Editor for the IEEE TRANSACTIONS ON ELECTRON DEVICES. He has extensively reviewed for different international journals. He was the recipient of the 29th IETE Ram Lal Wadhwa Gold Medal for his distinguished contribution in the field of semiconductor device design and modeling and the 2008 IBM Faculty Award. He was the first recipient of ISA-VSI TechnoMentor Award given by the India Semiconductor Association in recognition of a distinguished Indian academician or researcher for playing a significant role as a mentor and researcher.

Mark A. Reed (SM'97) received the B.S. degree (with honors) in physics, the M.S. degree in physics, and the Ph.D. degree in solid-state physics from Syracuse University, Syracuse, NY, in 1977, 1979, and 1983, respectively.

He joined Texas Instruments Incorporated as a Member of Technical Staff in the Ultrasmall Electronics Branch, where he cofounded the Nanoelectronics Research Program. In 1988, he was elected to Senior Member of Technical Staff. In 1990, he joined the faculty of Yale University, New Haven, CT, where he holds a joint appointment as Professor with the Departments of Electrical Engineering and Applied Physics, Harold Hodgkinson Chair of Engineering and Applied Science, and Associate Director of the Yale Institute for Nanoscience and Quantum Engineering. He has given 20 plenary and more than 280 invited talks. He is the author of more than 175 professional publications and six books. He is the holder of 25 U.S. and foreign patents. His research interests include the investigation of electronic transport in nanoscale and mesoscopic systems, heterojunction materials and devices, molecular-scale electronic transport, plasmonic transport in nanostructures, and chem/bio nanosensors.

Prof. Reed is a Fellow of the American Physical Society and a member of the Connecticut Academy of Science and Engineering. He is an Editor for the IEEE TRANSACTIONS ON ELECTRON DEVICES. He was the recipient of the Kilby Young Innovator Award (1994), the Fujitsu ISCS Quantum Device Award (2001), the Yale Science and Engineering Association Award for Advancement of Basic and Applied Science (2002), and the IEEE Pioneer Award in Nanotechnology (2007).

Gehan A. J. Amaratunga received the B.Sc. degree in electrical/electronic engineering from Cardiff University, Wales, U.K., in 1979 and the Ph.D. degree in electrical/electronic engineering from the University of Cambridge, Cambridge, U.K., in 1983.

He has held the 1966 Professorship in engineering with the University of Cambridge since 1998. He currently heads the Electronics, Power and Energy Conversion Group, one of four major research groups within the Electrical Engineering Division of the Cambridge Engineering Faculty. He has worked for 25 years on integrated and discrete electronic devices for power conversion, and on the science and technology of carbon-based electronics for 22 years. He has an active research program on the synthesis and electronic applications of carbon nanotubes and other nanoscale materials. His group has many "firsts" emanating from his research in carbon, including field emission from n-doped thin-film amorphous carbon and diamond, laboratory synthesis of carbon nanonions, tetrahedral amorphous carbon ("amorphous diamond")-Si heterojunctions, deterministic growth of single isolated carbon nanotubes in devices, high-current nanotube field emitters, and the polymer-nanotube composite solar cells. He is also has research interest in nanomagnetic materials for spin transport devices. He currently sits on the steering committee of the Nokia-Cambridge University Strategic Collaboration on Nanoscience and Nanotechnology and is the head of the Nokia-CU Nanotechnology for Energy Programme. His group was among the first to demonstrate integration of logic-level electronics for signal processing and high-voltage power transistors in a single IC (chip). His current research is focused on integrated power conversion circuits. He is a Cofounder of CamSemi—which is commercializing a new generation of power and mixed-signal ICs for power management with venture capital investment. He is also a founder of Enecsys, a company formed with his research students to develop and market integrated electronics for grid connection of small-scale solar, wind, and fuel cell generators. Nanoinstruments, a company he founded with his colleagues to commercialize CNT synthesis equipment, was recently sold to Aixtron. He has previously held faculty positions at the Universities of Liverpool (Chair in Electrical Engineering), Cambridge, and Southampton. He has held the U.K. Royal Academy of Engineering Overseas Research Award at Stanford University, Stanford, CA, and been a Royal Society visitor at the School of Physics, University of Sydney, Sydney, N.S.W., Australia. He has published over 450 journal and conference papers.

Dr. Amaratunga was elected a Fellow of the Royal Academy of Engineering, in 2004. In 2007, he was awarded the Royal Academy of Engineering Silver Medal "for outstanding personal contributions to British engineering."

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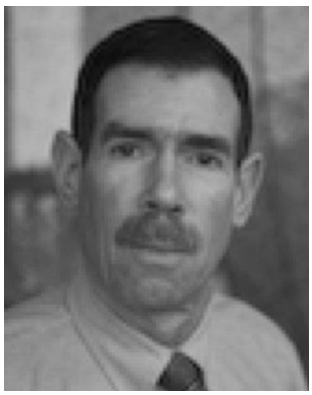
Dr. Chau was a recipient of six Intel Achievement Awards and 13 Intel Logic Technology Development Division Recognition Awards. He was also recognized by IndustryWeek in 2003 as 1 of the 16 "R&D Stars" in the U.S. who "continue to push the boundaries of technical and scientific achievement."



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Dr. Lundstrom currently serves as an IEEE Electron Devices Society Distinguished Lecturer. He is a Fellow of the American Physical Society and of the American Association for the Advancement of Science. In 1992, he received the Frederick Emmons Terman Award from the American Society for Engineering Education. With his colleague, S. Datta, he was awarded the 2002 IEEE Cledo Brunetti Award for their work on nanoscale electronic devices. In the same year, they shared the Semiconductor Research Corporation's Technical Excellence Award. In 2005, he received the Semiconductor Industry Association's University Researcher Award for his career contributions to the physics and simulation of semiconductor devices. Most recently, in 2006, he was the inaugural recipient of the IEEE Electron Devices Society's Education Award.

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Dr. Zhou is currently an Associate Editor of the IEEE TRANSACTIONS ON NANOTECHNOLOGY. He was a recipient of a number of awards, including the NSF CAREER Award, the NASA TGiR Award, the USC Junior Faculty Research Award, and the IEEE Nanotechnology Early Career Award.