Foreword

THIS IS the third issue of this TRANSACTIONS which has been devoted to high-resolution fabrication of electron devices. There has been considerable progress since the last such issue appeared in 1978. Perhaps, the most striking developments are those of techniques for fabricating functional structures with dimensions of less than 0.1 μm. In some cases, these techniques have been ingenious without involving highly developed materials or equipment while others have involved considerable sophistication in resist materials. An example of the latter is the multilevel resist process sequence described by Hu and her colleagues at Bell Laboratories in their paper entitled "High Resolution Techniques for the Fabrication of Small Area Josephson Tunnel Junctions."

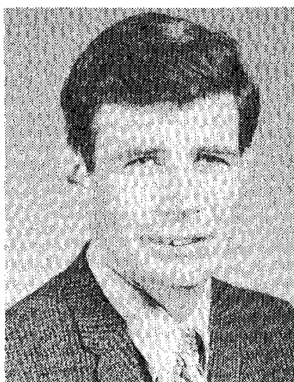
It would be nice to be able to claim that this issue contains representative papers on all aspects of high-resolution fabrication. However, reading the contents page will show that there are no papers devoted to ion-beam lithography, to X-ray lithography, or to the nonlithographic aspects of device fabrication, such as low-temperature processing of semiconductor circuits, which are not covered.

Nonetheless, the papers not only contain examples of the super high resolution work alluded to above but also show how both photolithography and electron-beam lithography have been maturing. The opening paper by A. N. Broers of IBM entitled "Resolution, Overlay, and Field Size for Lithography Systems" sets out the relationships between different lithographic parameters. In other papers, the considerable emphasis on computer simulation of both electron and photolithography indicate that repeatable control of critical dimensions, rather than minimum attainable feature size, is now regarded as the more dominant factor in patterning semiconductor circuits.

The papers on resists also point out that this subject has matured from a chemical science to a relevant technology for electron devices; it is also interesting to note that nonconventional resists, as exemplified by the paper entitled "Evaporated Silver Bromide as a Potential Photosensitive Material for the New Lithographies" by J. Lavine of the Ionomet Corporation, are receiving attention.

Thus while not embracing all aspects of High-Resolution Device Fabrication, these papers should provide good insight into most of the micropatterning techniques available to today's electron device engineer.

R. FABIAN W. PEASE
Guest Editor



Fabian Pease (M'75) received the B.A., M.A., and Ph.D. degrees from Cambridge University, Cambridge, England, and was awarded a Research Fellowship at Trinity College for work on high-resolution scanning-electron microscopy.

He then spent three years on the Electrical Engineering Faculty at the University of California, Berkeley, where he continued research in scanning-electron microscopy. During this time, he also served as a consultant on electron beam recording for IBM. In 1967 he joined Bell Laboratories, Holmdel, NJ, where he worked on digital encoding of television signals. He transferred to the Murray Hill, NJ, location 1971 and worked on electron and X-ray lithography. In 1978 he was appointed Professor of Electrical Engineering at Stanford University, Stanford, CA, where he has been pursuing research in electron-beam technology and in high-density integrated circuit technology.

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