Foreword

SOS Special Issue—SOS Technology

THE TECHNOLOGY of silicon on insulating substrates, specifically silicon on sapphire (SOS), dates back to the early days of practical MOS technology. The technology is also known by several other acronyms including SIS (silicon on insulating substrate) and ESFI (epitaxial silicon films on insulators). Extensive work on material properties and characterization techniques, processing techniques, device characteristics, novel devices, high-performance, low-power circuits and radiation hardening have been published. Extensive, although somewhat incomplete, bibliographies of work prior to 1975 are included in recent review articles [1]. Since 1975, three SOS Workshops have been sponsored by the IEEE Electron Devices Society. This Special Issue is based on papers presented at the third SOS Workshop held September 28-30, 1977, in Vail, CO. The papers in this Special Issue and the references included provide a reasonably comprehensive review of the work in SOS technology from 1975 to the present time. Interested followers of the latest developments in SOS technology are directed to the fourth SOS Workshop to be held in Vail, CO, October 4-6, 1978.

The first single-crystal SOS films were grown by Manasevit and Simpson of Rockwell International in 1963 by the H_2 reduction of $SiCl_4$ at high temperatures [2]. This was followed, a short time later, by similar work at RCA by Mueller and Robinson [3]. Workers at RCA and Rockwell with significant support from the Air Force and ARPA developed the SOS material over the next decade to its present relatively mature state as summarized in the first paper in this special issue by J. E. A. Maurits. This materials work is reviewed by Manasevit [4] in a 1974 survey article.

The principal advantage of SOS technology is the inherent dielectric isolation, both dc and ac. Further, the diffusion (or implantation) of source and drain electrodes entirely through the silicon to the sapphire substrate results in a vertical junction. This reduces electrode capacitance by more than an order of magnitude. In addition, the use of ion-implanted junctions with polysilicon gates and a low-temperature implant activation significantly reduces gate to drain overlap capacitance. The only remaining significant parasitic capacitance is that at metal to polysilicon crossovers. If C-MOS circuitry is used with this type of low parasitic capacitance structure, very-low-power, high-performance circuitry results.

The last two papers in this Special Issue show the potential for 1-GHz switching and linear amplification stages. Prescalers and counters made with 2-μm C-MOS/SOS operating at 1 GHz seem within reach already. Further reduction of gate length to the submicrometer region promises to make gigahertz silicon IC technology a very real possibility in the 1980's.

With the emergence of VLSI (see the last two papers in this Special Issue), SOS has several additional features which enhance its attractiveness:

1) Present chip power dissipation is limited to the range of 0.5 to 1.0 W with present packaging and cooling techniques. For most high-performance logic, at least 50 to 100 μA/gate are required. Thus practical chip sizes are limited to 10 000-20 000 gates per chip. Because only 10 percent of the nodes in an active circuit are toggeling at one time, C-MOS/SOS technology is capable of achieving densities of greater than 100 000 gates/chip. Standby power is less than 1 μW/gate so that standby power of 100 mW/gate is expected for chips with 100 000 gates.

2) The drain depletion region is controlled by the gate electrode and the sapphire dielectric. This results in a modified short-channel effect and higher drain breakdown voltage. (See last paper in this issue.)

3) Shallow contact effects are reduced or eliminated since the junctions extend all the way to the sapphire substrate and no silicon substrate exists to cause spiking or shorting below the junction.

4) The inert substrate between devices on silicon islands results in a lower effective density of photolithographically induced defects [5]. This offers the potential for a high-yield six-mask process applicable to high-density VLSI technology.

5) The dielectric isolation allows for very-high-gain linear amplification and the combination on the same chip of linear and digital electronics.

6) The SOS structure offers extremely high tolerance to hostile radiation environments at high- and low-temperature extremes. (See B. L. Buchanan review in Radiation Effects section of this Special Issue.)

Although these advantages of SOS seem impressive, a number of shortcomings have impeded the progress of SOS technology over the years. These include:

1) The cost of SOS substrates is 4 to 5 times that of bulk silicon.

2) The material quality of SOS films is significantly poorer than single-crystal silicon used in present-day IC fabrication. This results in low minority carrier lifetime ($<10^{-9}$ s) and—in comparison to monolithic silicon—higher surface state density, higher diode leakage, and reduced mobility.

3) The yield of SOS circuits has been limited by wafer breakage, reduced dielectric integrity, and metal step coverage at island edges.

0018-9383/78/0800-0857$00.75

4) The SOS substrate tends to float due to high-resistance body contact (or lack of body contact). This results in the so-called "kink" effect [6].

5) For VLSI applications, SOS films in the 2000- to 4000-Å thickness range are desirable. Present films in this thickness range are of poor quality. This problem remains as one of the significant challenges for SOS VLSI.

However, solutions to all these problems, except 5), have emerged in the last three years. The cost of Czochralski material continues to drop as volume builds up. New sapphire ribbon growth techniques [7], if successful, promise to further reduce the cost penalty for SOS. Material quality is sufficient for static digital logic and linear circuitry if low-temperature processing is utilized. The detrimental effects at SOS island edges have been greatly minimized by the use of a grown oxide between islands (isoplanar approach) [5].

Support to this latter contention on the maturing state of SOS technology is derived from the recent flurry of activity at many major IC manufacturers. This Special Issue is very timely in presenting a capsule status report on SOS at a period of time when SOS is beginning to emerge as a widely accepted technology and promises to fulfull the expectations that so many of the active workers is SOS have been advocating for the last 10 years.

References

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Guest Editor

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