Erratic Erase in Flash Memories—Part II: Dependence on Operating Conditions

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***Abstract*—This paper presents experimental results about the erratic erase phenomena occurring in Flash Memories with the aim of providing a deeper insight into the physical nature of the phenomenon and to deepen the comprehension of charge trapping/detrapping dynamics in tunnel oxides during Fowler-Nordheim erase. The results obtained under different operating conditions as Program/Erase cycling, Ultra Violet light exposure, thermal stress and the analysis of the erratic erase behavior varying the erasing conditions and the tunnel oxide thickness, suggested also possible methods that can be used in order to reduce the erratic erase phenomena.**

***Index Terms*—Erasing operation, Flash memories, integrated circuit reliability, semiconductor memories.**

I. Introduction

ERRATIC erase, characterized by a random variation of the erased threshold voltage of a cell during cycling, represents a major concern of Flash Memory reliability. Erratic erase has been attributed [1], [2] to clusters of three or more charges in the oxide close to the floating gate interface and producing a reduction of the tunneling barrier height for electrons that are injected in their vicinity, thus enhancing the erasing dynamics of the considered cell. As a consequence, after erase, the threshold of the cell would have a lower value as compared with the normal case where no clusters are present. The presence/absence of positive clusters of charge may be related to trapping/detrapping of holes that may be generated by impact ionization in the anode (silicon substrate) of high energy electrons emitted from the cathode (floating gate), i.e., with the so called Anode Hole Injection (AHI) mechanism [3]. In general, hole trapping will result in negative erratic threshold shifts while hole-detrapping will result in positive shifts.

In a previous work [4], some basic experimental results and a statistical characterization of the erratic behavior have been presented. In this paper we present a large set of experimental results with the aim of providing a deeper insight into the physical nature of the phenomenon and to deepen the comprehension of charge trapping/detrapping dynamics in tunnel oxides during Fowler Nordheim (FN) erase. This has been done investigating the dependence of the erratic erase on several conditions as Program/Erase cycling, Ultraviolet (UV) light exposure, thermal stress, and tunnel oxide thickness.

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Finally, the analysis of the erratic erase behavior varying the erasing conditions suggested also possible methods that can be used in order to reduce the erratic erase phenomena.

II. Experimental Setup

All measurements have been performed by means of a dedicated automated test equipment [5] on single sectors of 512 kbits NOR-type Flash test chips. The tunnel oxide thickness was 10.2 nm and ≈7 nm for the data of Section IV.

Where not differently stated, the erase operation has been performed over the channel ($V_{SB} = 0\,\mathrm{V}$) via FN tunnel applying a sequence [6]–[8] of $N = 7$ rectangular pulses with the control gate and the bulk voltages at $V_G = -8$ V and $V_B = 6.12$ V, respectively.

The Program operation has been performed via Channel Hot Electron (CHE) applying 8 V to the control gate and 4.5 V to the drain for 5 μs.

The threshold voltage has been measured as the control gate voltage at which the cell drains a predefined current.

All data have been collected measuring the erased threshold voltage V_{T_E} of each cell for a certain number of cycles. Erratic behaviors have been marked whenever the V_{T_E} value for a cell exhibited a cycle-to-cycle absolute variation larger than 250 mV. During any experiment, a cell has been marked as erratic when exhibiting its first erratic behavior. Different experimental conditions have been used when analyzing the effect of oxide thickness, as shown in Section IV.

III. Dependence on Operating Conditions

A. Oxide Aging Effect

Fig. 1 shows the number of cells marked as erratic during successive tests of 1000 cycles on the same memory sector. This number is a decreasing function of the amount of cycles applied to the cells, thus showing a dependence of the erratic behavior on oxide aging during cycling. This result has a definite impact on all the further experiments shown in this paper, since a fair data comparison would always require measurements on virgin sectors. In the rest of the paper we will limit the use of virgin sectors to the mandatory cases, while in other experiments involving successive tests of 1000 cycles we will account for the oxide aging effect shown in Fig. 1.

B. Ultraviolet Light Exposure

UV-erase has been experimentally found to have a significant impact on the erratic dynamics. After 10 000 cycles an entire sector of cells was programmed and then UV-erased (253.7 nm)

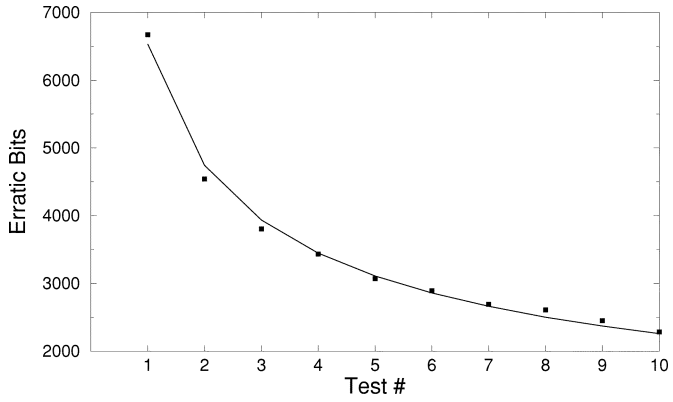

Fig. 1. Number of cells marked as erratic during successive tests of 1000 cycles on the same memory sector.

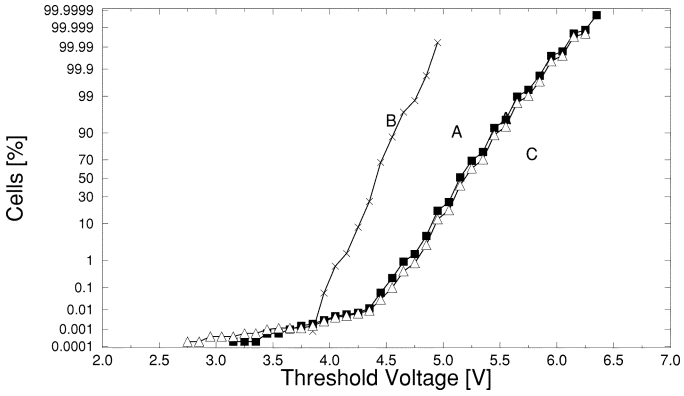

Fig. 2. Distributions of erased threshold voltages of an entire sector. (A) After 10 000 cycles. (B) After a program operation and the UV light exposure for 1 h (253.7 nm). (C) After a further program/erase cycle.

for 1 h. The erased distribution after 10 000 cycles (A) and after a program operation followed by UV erase (B) are shown in Fig. 2. After a further program/erase cycle (C), the numbers of erratic events and threshold shift polarities produced during this final cycle have been compared to the values measured during cycling before UV. A huge increase of erratic events has been found in C (192 events with respect to ≈5 events/cycle during cycling before UV) together with an evident prevalence of positive shifts (157) with respect to negative shifts (35). The increase of negative shifts can be appreciated by looking at the tail of the C distribution in Fig. 2 where some new tail bits clearly exhibit low thresholds. On the contrary, since the threshold voltages of erratic bits exhibiting a positive shift after are drowned in the C distribution, their average effect on C distribution may be masked by the total amount of cells $(\approx 500\ \mathrm{K})$ that does not exhibit erratic events: only a small and negligible positive shift can be seen by comparing C and A distributions.

The large number of positive shifts may be attributed to holes trapped in clusters of positive charge near the floating gate that escape their trap sites during UV exposure. Cells where this phenomenon takes place may become "normal" cells. So, during the first FN erasing following the UV exposure, their normal behavior gives rise to higher thresholds with respect to the pre-UV condition.

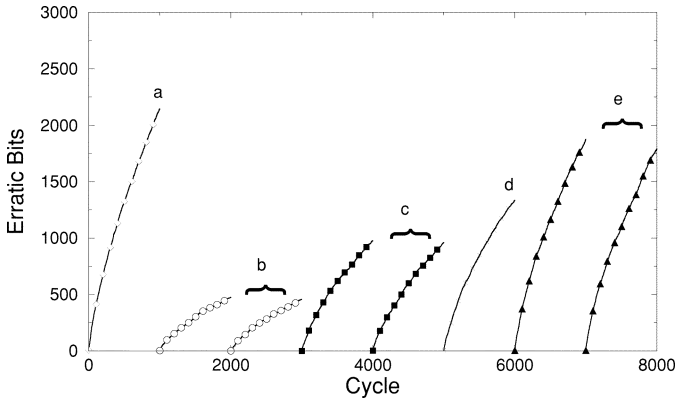

Fig. 3. Cumulative number of erratic bits during successive 1000-cycle tests on the same memory sector using the pulse parameters of Table I.

TABLE I
DEPENDENCE ON N AND V_B

Test	N	Δt [μs]	V_B [V]
a	3	100	8.5
b	4500	100	4.5
c	80	100	6.5
d	16	100	7.5
e	6	48	8.7

On the other hand, hole detrapping during UV exposure leaves empty trap sites that can be easily repopulated. Hence, during the first FN erasing following the UV exposure, many holes may be trapped giving rise also to a larger number of negative shifts with respect to the pre-UV condition.

C. Erasing Pulse Parameters

In this section it will be evidenced how erasing scheme parameters have a strong impact on the erratic phenomenon.

In order to allow a simple evaluation of the weight of each erasing parameter on the erratic erase phenomenon we will consider the most simple erasing scheme where a sequence of N equal, rectangular pulses with a duration Δt and separation τ are applied. The pulses where characterized by a constant $V_G = -8$ V while V_B has been varied during different experiments.

Fig. 3 shows the number of bits marked as erratic during successive 1000-cycle tests on the same memory sector. The parameters chosen for the erasing pulses during each test (reported in Table I) guaranteed the same average erased threshold voltage.

The test sequence was selected in order to observe an increase of the number of erratic bits that overrules the oxide aging effect (see Section III-A). In this way we are sure that the observed increase using c, d, and e parameters is certainly due to the change of the erasing scheme. On the other hand, the decrease in test b with respect to test a is too high as it could be with respect to the oxide aging effect (see points 9–10 of Fig. 1) and therefore it is a direct consequence of the erasing scheme used in b.

From the results of Fig. 3 it is possible concluding that the use of a high initial electric field and/or a low number of pulses produces a significant enhancement of erratic failures.

TABLE II
DEPENDENCE ON Δt AND τ

Test	N	Δt [ms]	τ [ms]	Erratic Bits	Err. Ev. per cycle
1	7	10	10	4781	19.7
2	7	10	10	3276	13.5
3	7	10	30	2665	10.9
4	7	10	1	2435	10.9
5	7	20	1	2485	11.1
6	7	30	1	2407	11.0
7	1	707	n.a.	2749	12.82
8	7	100	1	2481	11.24

TABLE III
DEPENDENCE ON V_B

Test	V_B [V]	V_T [V]	Erratic Bits	Err. Ev. per cycle
1	6.12	3.46	2008	8.99
2	4.00	5.41	906	3.79
3	5.00	4.49	1285	5.40
4	6.12	3.49	1909	7.89

The results of the analysis of the erratic bit statistic varying Δt and τ while keeping V_B constant at 6.12 V are reported in Table II.

Within the first three tests (characterized by the same values of N and Δt) the number of erratic bits decreases, following the expected dependence on oxide aging. For tests $4 \div 6$ the number of erratic bits is almost constant, showing that an increase in Δt just compensate the aging effect. With test 7 (one single long pulse) a significant increase of the erratic bit number has been found, while the successive test (characterized by a longer Δt with respect to test $4 \div 6$) produces almost the same results as test $4 \div 6$.

Summarizing the results of Table II we conclude that, while τ and Δt seem not having a significant influence on the erratic behavior, test 7 confirms a strong dependence on the number of erasing pulses.

The dependence on V_B has also been evaluated by successively erasing the considered sector with the same number of pulses and pulse duration ($N = 7$, $\Delta t = 100$ ms) but varying V_B (thus resulting in different erased threshold voltage distributions whose average value is also indicated by V_T column). As shown by data in Table III, there is a strong correlation between V_B and the erratic phenomenon. Low values of V_B are correlated with low values of both the erratic bit number and the average number of erratic events per cycle.

To investigate the influence of the pulse number on erratic erase a further analysis has been performed on three virgin sectors. V_B was always kept at 6.12 V while Δt, whose effect on erratic behavior has shown to be negligible, has been changed in order to reach the same average erased threshold after erase for each sector (see Table IV). The evolutions of the number of erratic bits for the three experiments are reported in Fig. 4.

As shown, the number of erratic bits is a strong function of the total number of pulses applied during erasing.

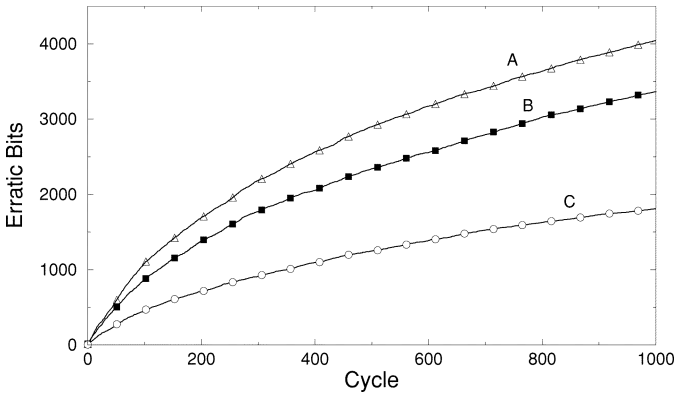

Fig. 4. Cumulative number of erratic bits as a function of cycle number for virgin sectors erased using the parameters of Table IV.

TABLE IV
DEPENDENCE ON N

Sample	N	Δt [ms]	V_B [V]
A	7	10	6.12
B	80	1	6.12
C	1000	0.1	6.12

This result can be explained by looking at the entire erasing curve of an erratic cell (i.e., the evolution of the threshold voltage as a function of the number of erasing pulses). It has been already evidenced the possibility of having two equal and opposite erratic shifts during the same erasing operation [9]. In this case, no erratic shifts are observed at the end of the erasing operation and, the larger is the number of erasing pulses, the larger is the probability that during the same erasing operation a charge cluster may be subjected to both trapping and detrapping events whose effects neutralize mutually.

As a general comment concluding this section, it can be stated that the use of a large number of erasing pulses and a low value of the electric field during erasing will improve Flash memory reliability reducing the erratic erase phenomena.

D. Thermal Stress Effect

The influence of a thermal stress has also been evaluated by comparing the number of erratic bits marked during two 1000-cycle tests performed before and after a 12 h bake at 250°C. As shown by Fig. 5, after the bake, erratic erase failures exhibit a significant increase.

The effect of a thermal bake has been further analyzed by the following experiment: during a memory sector cycling, after the 1000th cycle and after the 4000th cycle a 12 h and a 9 h bake at 250°C were performed, respectively. As it can be seen in Fig. 6, where the moving average of erratic events marked at the end of each cycle has been plotted, after each bake the number of erratic events per cycle exhibits a significant increase.

The thermal stress produces another important result as shown in Fig. 7 where the cumulative difference between positive and negative shifts at each cycle is reported: positive shifts become dominant in regions 2 and 3.

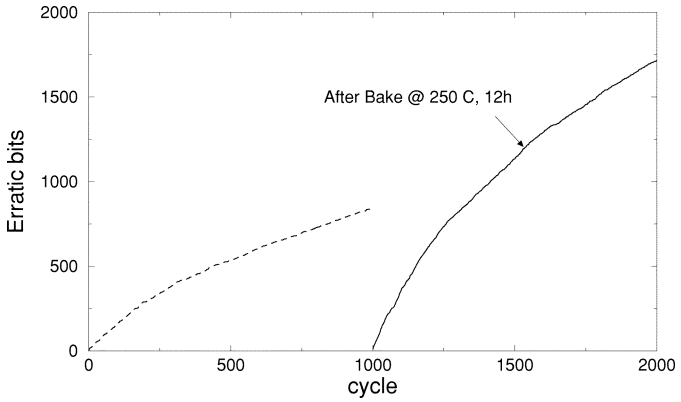

Fig. 5. Cumulative number of erratic bits during 1000-cycle tests performed before (dashed line) and after (solid line) a 12 h bake at 250°C.

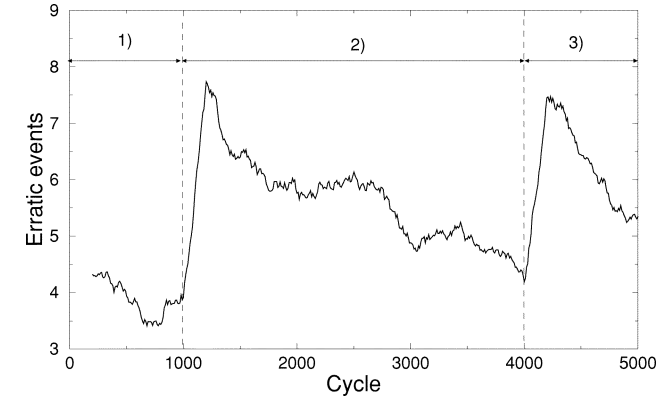

Fig. 6. Moving average (over the previous 200 samples) of erratic events per cycle. The dashed lines indicate where the 12 h and the 9 h bakes at 250°C were performed. The moving average has been here preferred with respect to the actual number of events per cycle to mask noise effects.

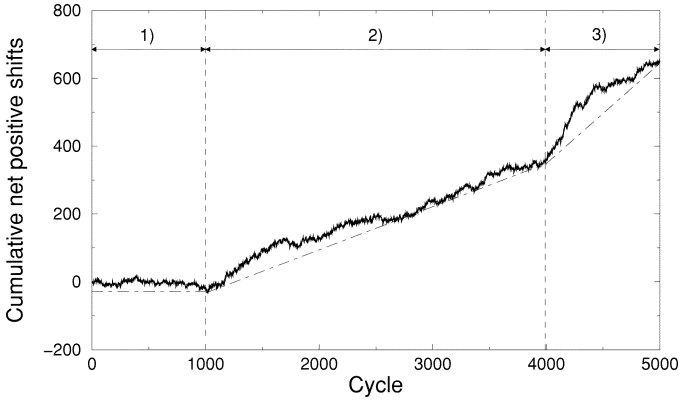

Fig. 7. Cumulative net positive shifts, i.e., the cumulative sum of the difference between positive and negative shifts measured at each cycle. The dashed lines indicate where the 12 h and the 9 h bakes at 250°C were performed.

The charge/cluster model [2] attributes positive shifts to detrapping/neutralization of the positive charge clusters while negative shifts are related to hole trapping. So, the difference between positive and negative shifts at each cycle represents the relative behavior of hole trapping/detrapping dynamics.

In region 1 (from cycle 1 to 1000, performed before the bake), there is equilibrium between positive and negative shifts dynamics being the curve almost constant and oxide aging effects are negligible. After the first bake (region 2), the detrapping dynamics results larger than the trapping dynamics and positive shifts occurrence increases with respect to negative shifts. The second bake (region 3) produces a further increment of the detrapping dynamics, i.e., of the occurrence of positive shifts over the negative shifts.

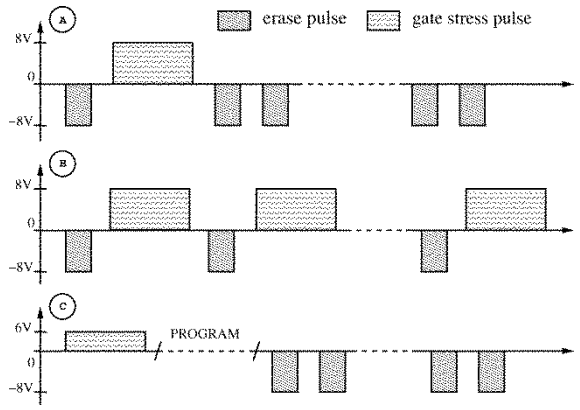

Fig. 8. Sketch of the applied gate voltage for the three gate stress schemes.

These measurements reveal that the ratio between trapping/detrapping dynamics depends significantly on the bake time. These results may be explained qualitatively by an increase of the hole detrapping probability. Nevertheless, it remains still obscure how temperature may influence such an effect.

E. Gate Stress Effect

It has been shown [10] that the use of a gate stress pulse after erase may have a detrapping/neutralization effect on holes trapped in the oxide and, as a consequence, it may lead to an increase of memory endurance.

Since erratic bits are related to holes trapped in the oxide, we checked for a possible correlation between gate stress and the erratic phenomenon.

To this purpose we used three gate stress/erase voltage schemes (see Fig. 8): scheme A, where a gate stress pulse was applied just after the first erasing pulse; scheme B, where a gate stress pulse was applied to the cell after each erasing pulse; and scheme C where the gate stress was performed before programming. Gate stresses of scheme A and B were performed with $V_G = 8.5$ V and $V_B = -8.5$ V or $V_B = -5$ V for 50 ms. Gate stress of scheme C was performed with $V_G = 6$ V, $V_B = -6$ V for 1 s.

The effect of a gate stress on the erratic erase can be evaluated from the results of Fig. 9, where a memory sector was successively cycled for 1000-cycle tests under different voltage schemes.

Fig. 9 clearly shows that scheme A reduces the probability of erratic erase with respect to normal erasing conditions. Infact, the cumulative number of erratic bits measured without gate stress (cycles 1001–2000 in Fig. 9) does not decrease with respect to cycles 1–1000 as expected from the oxide aging effect (see Section III-A). Scheme B (cycles 2001–3000) does not produce significant difference with respect to scheme A.

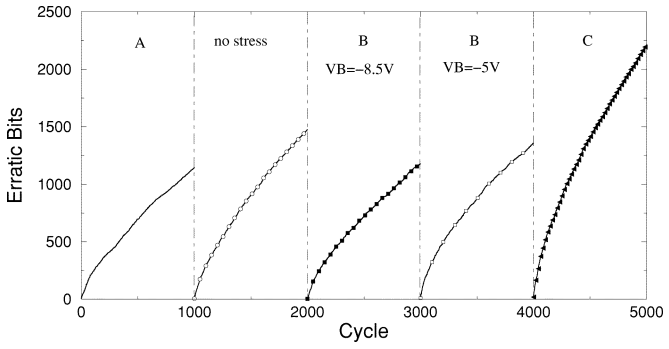

Fig. 9. Number of cells marked as erratic during successive 1000-cycles tests on the same memory sector under different gate stress schemes. In sequence: scheme A (cycles 1–1000); no gate stress (cycles 1001–2000); scheme B with $V_B = -8.5$ V (cycles 2001–3000); scheme B with $V_B = -5$ V (cycles 3001–4000); scheme C (cycles 4001–5000).

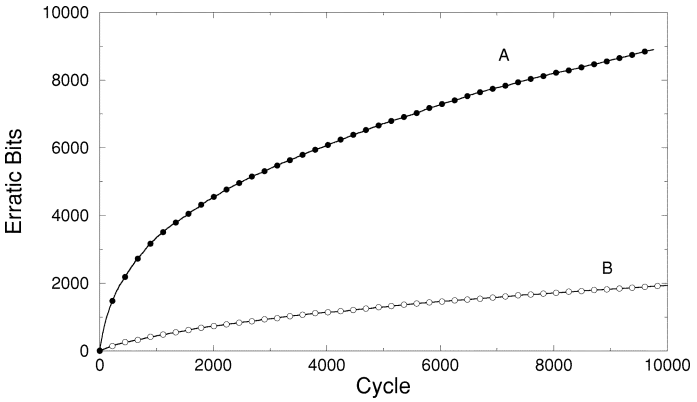

Fig. 10. Cumulative number of erratic cells for sample A (solid symbols) and B (empty symbols).

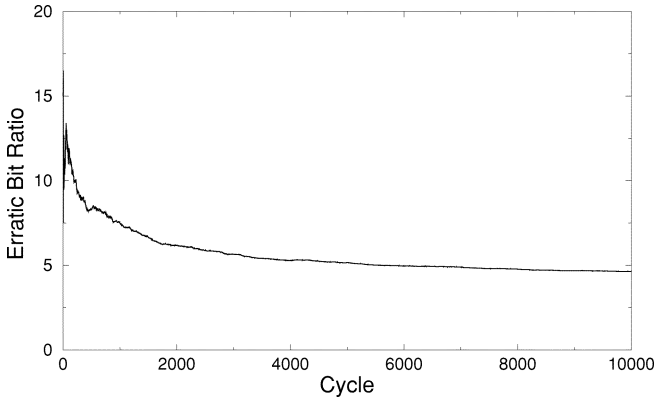

Fig. 11. Ratio of the number of erratic bits of sample A with respect to that of sample B of Fig. 10.

Those bits whose erasing dynamics increases abnormally due to holes trapped during the previous erasing pulse may become 'normal' again after a gate stress pulse, exhibiting a normal FN erasing dynamics for the rest of the erasing operation. On the other hand, since for both schemes the amplitude of the erasing pulses is constant, the largest contribution to floating-gate charge removal is produced by the first erasing pulse [8]. In the same way, due to the AHI mechanism, the larger number of hot holes is created and trapped in the oxide just at the beginning of erasing. In this situation, a gate stress pulse applied after the first erasing pulse is more effective in the removal of trapped holes, thus restoring any anomalous FN erasing dynamics before the end of the considered erasing operation. For this reason, scheme A and scheme B give similar results.

Another indication comes from scheme B with a lower V_G during gate stress (cycles $3001 \div 4000$): the number of bits marked as erratic is larger with respect to scheme B with a higher stress voltage. The smaller is the gate stress voltage, the smaller is the removal of trapped holes and the smaller is the number of cells whose FN erasing dynamics can be restored before the end of erasing.

Contrary to what happens with schemes A and B, the erratic erase probability increases when the gate stress pulse is performed before the erasing operation (scheme C). Both increases of positive and negative shifts have been found, with a prevalence of positive ones.

The increment of positive shifts may be due to the additional removal of part of the clusters of oxide-trapped charge induced by the gate stress performed before the erasing operation. At the same time, the increment of the negative shifts may be due to the trap sites left empty by the gate stress that are repopulated during the following erasing operation.

IV. Dependence on Tunnel Oxide Thickness

Using CCES, two cycling experiments have than been performed in order to find all erratic shifts within the first 10 000 cycles for two virgin samples that differ only in their tunnel oxide thickness: 10.2 and 7 nm for samples A and B, respectively.

During erasing the cell control gates were biased by pulses with a constant amplitude (-8 V for sample A and -3 V for sample B), while the common bulk was driven by a sequence of 20 pulses with increasing amplitude $\Delta V_B = 0.3$ V starting from V_B^0 (1.5 V for sample A and 2 V for sample B). The duration of each erasing pulse was $\Delta t = 10$ ms.

Program/erase operating conditions have been chosen so that comparables average electric fields during erasing [8] and similar program/erase threshold windows for both samples were guaranteed. In particular, during erasing, the average electric fields were 10.3 and 10.8 MV/cm for samples A and B, respectively.

The most important result extracted from cycling experiment performed on the two samples is presented in Fig. 10 that compares the number of erratic bits occurred during cycling for both sample A and sample B.

Sample A exhibits a larger number of erratic bits and, for both samples, the number of erratic bits does not seem to saturate. Nevertheless their ratio reaches a constant value as shown in Fig. 11.

From Fig. 10 it is evident that erratic erase is a strong function of the oxide thickness showing that thinner oxides are less prone to erratic erase phenomena.

The result of Fig. 11 and the general dependence on oxide thickness may be explained assuming that the positive clusters of charge may origin from AHI [3]: during erasing the FN electron current density J_n creates hole/electron pairs in the anode by impact ionization. Part of the generated holes tunnel back to

the floating gate and are trapped in the oxide. We therefore suggest that the higher erratic bit failure distribution of sample A may be a consequence of the AHI current that increases with the tunnel oxide thickness.

During erasing, with the considered tunnel oxide thickness and electric fields, from [3] and [11] it is possible to estimate that the fraction of hole-to-electron current density J_p/J_n is $\approx 1 \cdot 10^{-3}$ for sample A and $\approx 2 \cdot 10^{-4}$ for sample B. Since ΔV_B and Δt are the same for both samples, we can also assume [8] that J_n is almost the same for both samples. Therefore the hot-hole current increase of sample A with respect to sample B may be expressed as

$$\frac{\left(\frac{J_p}{J_n}\right)_{\text{sample } A}}{\left(\frac{J_p}{J_n}\right)_{\text{sample } B}} \approx 5. \tag{1}$$

This increase in the hole-current density may be related to a proportional increase of the hole trapping probability and therefore to an increase of the number of erratic bits during cycling.

The experimental result of Fig. 11 is in agreement with the hypothesis of a correlation between anode hole current and erratic bits failure. The ratio of the erratic bit failure distribution of sample A with respect to that of sample B reaches a constant value that is close to the hole current ratio of (1).

V. Conclusion

Experimental results revealed that the erratic erase significantly depends on oxide aging, and decreases during cycling. Therefore, by repeating of the same test with the same erasing conditions on the same array will result in a lower number of erratic bits/events.

The erasing parameters of a standard erasing scheme have been varied in order to find all those parameters that may play a significant role in the erratic phenomena. In particular the erratic erase may be significantly reduced using a sequence of pulses instead of a single pulse during erasing and using low values for the bulk voltage.

Thermal bake has also been carried out to investigate the thermal properties of the erratic phenomena. We found that thermal bake has a significant influence on the erratic erase occurrence. In particular, after each bake, it is possible to observe a significant enhancement of erratic erase occurrence during cycling. We also observed an increase of the dynamics of positive shifts after with a significant dependence on bake duration.

A set of gate stress experiments also reveals that the number of positive erratic shifts may increase if a gate stress pulse is applied before erasing while, performing the gate stress during erasing, both positive and negative erratic events will decrease. Moreover, it has been observed that the reduction is more effective using higher values of the gate stress electric field and that only one gate stress pulse after the first erasing pulse may be sufficient.

Measurements and statistics on erratic behaviors of Flash memories featuring different oxide thickness reveal that, under the same operating conditions, thinner oxides are more robust against erratic erase.

All the measurements on the erratic phenomena seem to support the charge/cluster model [2]. In fact, thermal bake, gate stress, and UV exposure neutralize part of the charge trapped in the tunnel oxide leaving new empty trapping sites that may be occupied by holes injected in the following erasing operations. Experimental comparisons of data obtained varying oxide thickness and bulk voltage give another useful indication for the physical modeling of the erratic phenomena being the dependence of erratic bit failure distribution on oxide thickness and on bulk voltage consistent with an anode hole injection model [3].

Acknowledgment

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References

[1] T. C. Ong, A. Fazio, N. Mielke, S. Pan, N. Righos, G. Atwood, and S. Lai, "Erratic erase in ETOX™ flash memory array," in *VLSI Symp. Tech.*, 1993, pp. 83–84.

[2] C. Dunn, C. Kaya, T. Lewis, T. Strauss, J. Schreck, P. Hefley, M. Middendorf, and T. San, "Flash EPROM disturb mechanisms," in *Proc. Int. Rel. Phys. Symp.*, 1994, pp. 299–299.

[3] K. Kobayashi, A. Teramoto, M. Hirayama, and Y. Fujita, "Model for the substrate hole current based on thermoionic hole emission from the anode during Fowler-Nordheim electron tunneling in n-channel metal-oxide-semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 77, pp. 3277–3282, Apr. 1994.

[4] A. Chimenton and P. Olivo, "Erratic erase in Flash memories—Part I: Basic experimental and statistical characterization," IEEE Trans. Electron Devices, vol. 50, pp. 1009–1014, Apr. 2003, to be published.

[5] P. Pellati and P. Olivo, "Automated test equipment for research on nonvolatile memories," *IEEE Trans. Instrum. Meas.*, vol. 50, pp. 1162–1166, Oct. 2001.

[6] K. Yoshikawa *et al.*, "Comparison of current flash EEPROM erasing methods: Stability and how to control," in *IEDM Tech. Dig.*, 1992, p. 595.

[7] R. Bez, D. Cantarelli, L. Moioli, G. Ortolani, G. Seravalli, C. Villa, and M. Dallabora, "A new erasing method for a single-voltage long-endurance Flash memories," *IEEE Electron Device Lett.*, vol. 19, pp. 37–39, Feb. 1998.

[8] A. Chimenton, P. Pellati, and P. Olivo, "Constant charge erasing scheme for flash memories," *IEEE Trans. Electron Devices*, vol. 49, pp. 613–618, Apr. 2002.

[9] ——, "Analysis of erratic bits in flash memories," *IEEE Trans. Device Mater. Rel.*, vol. 1, pp. 179–184, Dec. 2001.

[10] T. Endoh, H. Iizuka, S. Aritome, R. Shirota, and F. Masuoka, "New write/erase operation tecnology for flash EEPROM cells to improve the read disturb characteristics," in *IEDM Tech. Dig.*, 1992, pp. 603–606.

[11] F. Nebel and M. Jourdain, "On the correlation between interface defects, positive oxide charge and hole fluence throughout the oxide," *J. Non-Cryst. Solids*, vol. 245, pp. 67–72, 1999.

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