

Special Issue on PCB Level Signal Integrity, Power Integrity, and EMC

THE RAPID growth and convergence of digital computing and wireless communications have been driving semiconductor technology to continue its evolution following Moore's law in today's nanometer regime. Modern electronic systems integrate more complex components and devices, which results in a very complex electromagnetic field environment. Electromagnetic compatibility (EMC) has become one of the major issues in printed circuit board (PCB) and integrated circuit (IC) design.

High frequency channel loss, reflection, and crosstalk are causing degradation of the receiver eye opening, jitter performance, and bit error rate. In addition, improper PCB design can lead to noncompliance with EMC regulations. The growing popularity of mixed integration on the same PCB of noise sensitive radio frequency and sensor chips with noisy digital chips has created significant PCB design challenges to suppress high-frequency electromagnetic interference. High-frequency electromagnetic interference can yield lower receiver sensitivity and performance degradation. In order to overcome these difficulties and achieve compatibility, there have been major advances in areas of PCB level modeling, design, and measurement with respect to signal integrity, power integrity, and EMC.

This special issue is published to highlight the recent significant advancements and innovations related to PCB signal in-

tegrity (SI), power integrity (PI), electromagnetic emission and susceptibility modeling, design, and measurement technologies. The issue has received an overwhelming response from the PCB EMC community, and 24 high quality papers are selected for publication in this issue. We express our sincere thanks to all the respected authors, ex-Chief Editor, Dr. P. Wilson, and current Chief Editor, Prof. H. Garbe, for their very active support and prompt response. Without their support this special issue would never have been published. We are sure that the readers will find interest in this special issue, and we hope it will benefit the EMC industry and academic community.

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Joungho Kim received the B.S. and M.S. degrees from Seoul National University, Seoul, Korea, in 1984 and 1986, respectively, and the Ph.D. degree from the University of Michigan, Ann Arbor, in 1993, all in electrical engineering.

In 1994, he joined Memory Division of Samsung Electronics, where he was involved in Gbit-scale DRAM design. In 1996, he joined the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, where he is currently a Professor in the Electrical Engineering and Computer Science Department. Since joining KAIST, his research has been focused on modeling, design, and measurement methodologies of 3-D hierarchical semiconductor systems including multistack high-speed chip, 3-D package, interconnection, and multilayer printed circuit board (PCB). He has successfully demonstrated low noise and high performance designs of more than ten system-in-packages (SiPs) for wireless communication applications such as ZigBee, terrestrial digital multimedia broadcasting (T-DMB), near field communication (NFC), and ultra wide band (UWB). He was on a sabbatical leave during an academic year from 2001 to 2002

at Silicon Image Inc., Sunnyvale CA, where he was responsible for low noise package designs for serial advanced technology attachment (SATA), fiber-optic connectors (FC), high-definition multimedia interface connectors (HDMI), and panel link SerDes devices. Currently, he is also the Director of Satellite Research Laboratory, Hyundai Motors, Inc., Seoul, Korea, where he has been engaged in research on electromagnetic interference/electromagnetic compatibility modeling of automotive radio frequency, power electronic, and cabling systems. His current research interests include chip-package codesign and simulation for signal integrity, power integrity, ground integrity, timing integrity, and radiated emission in 3-D integrated circuits, 3-D semiconductor packages, and SiP. He is the author and coauthor of more than 230 technical papers published at refereed journals and conference proceedings in modeling, design, and measurement of 3-D IC, package, and SiP. He has delivered more than 105 invited talks and tutorials at the academia and the related industries.

Dr. Kim was the recipient of the Outstanding Academic Achievement Faculty Award of KAIST in 2006, and the Best Faculty Research Award of KAIST in 2008. He is the Symposium Chair of IEEE EDAPS 2008 Symposium. He is an Associated Editor of the IEEE TRANSACTIONS OF ELECTROMAGNETIC COMPATIBILITY. He also serves as the Chapter Chair of IEEE CPMT Daejeon Chapter.



Erping Li (S'91–M'92–SM'01–F'08) received the Ph.D. degree in electrical engineering from Sheffield Hallam University, Sheffield, U.K, in 1992.

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Dr. Li is a Fellow of Electromagnetics Academy, USA. He was the recipient of the 2006 IEEE EMC Technical Achievement Award, the 2007 Singapore IES Prestigious Engineering Achievement Award, and the prestigious Changjiang (Yangtze) Chair Professorship Award from the Ministry of Education in China in 2007. He is an elected IEEE EMC Distinguished Lecturer for 2007 to 2008. He served as an Associate Editor for the IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS from 2006 to 2008 and currently serves as an Associate Editor for IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY. He has been a Technical Chair, Session Chair for many international conferences. He was the President for the International Zurich Symposium on EMC held in 2006 and 2008 in Singapore, the General Chair for the 2008 Asia-Pacific EMC Symposium, and the Chairman of the IEEE EMC Singapore Chapter for 2005–2006. He has been an Invited Speaker at various international conferences and forums.